

# 8

## MEMS Packaging And Assembly

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## **Executive Summary**

There are many references by MEMS experts as to the high percentage of the product cost attributed to the “Back end” (i.e., package and test). This percentage has been cited as high as 70% of the total cost. Packaging has not until recently received the research and development attention it deserves as a key enabler for microsystems commercialization. Packaging has often been referred to as the “Achilles Heel of MEMS Manufacturing” and a key “Bottleneck” in the process of MEMS commercialization.

A significant amount of attention is now being directed at packaging concerns. Packaging was an afterthought for most MEMS designers and manufacturers only a few years ago. Now it is part of the initial design process as mentioned by many notables such as Dr. Steven Senturia (see the Design, Simulation, and Modeling chapter for further insight). It is this second question that will dominate packaging and assembly over the next 5 years in order to make the majority of MEMS devices cost-effective and more ubiquitous in the marketplace. Therefore, a chapter in this MST Roadmap has been dedicated to the challenges of packaging.

Assembly of MEMS devices utilizes many engineering and design tools and supporting infrastructure for microsystems. There is a trend for MEMS specific packaging and assembly tools from EVG, Karl Suss, MA3 Solutions and many others, although Cost of Ownership in relation to the often relative small production volumes can be a problem. But, to date, many MEMS devices are developed using equipment not specifically MEMS-oriented, but more likely standard semiconductor industry equipment that has been modified somewhat (“Force-fit Prototyping” see the Introduction chapter). As discussed in both the IC and Non-IC related chapters, there are many application specific processes in MEMS. Nowhere is this more

apparent than in MEMS packaging. More often than not, this application specific approach leads to a trial-and-error approach to packaging design and implementation. However there is a growing attention to more generic approaches of which waferscale packaging and modification of standard IC packaging concepts to enable MEMS packaging are the most striking examples.

There is a trend toward the “Product Family” concept in microsystems. This occurs when the same core MEMS device is utilized in several applications causing the manufacturer to package the device in several different ways, depending on the environment where the device will finally be used. For example, *in vivo*, bioMEMS devices have to be encapsulated so that they are truly non-invasive. MEMS devices used in engine performance sensing must be temperature resistant, while other MEMS devices used in space applications will have to be radiation hardened. Thus, since there are so many different types of MEMS devices being developed for use in nearly every conceivable market, there are at least double the amounts of packaging methods that have to be considered.

Often, the MEMS industry is likened to the semiconductor industry in its nascent days. At that time, the semiconductor industry faced many of the same issues with packaging ICs because the expensive packaging was often considered an afterthought. Over time, the semiconductor industry separated into two completely different fields with very little overlap: front-end and back-end (packaging). Lately the borderline is becoming vague with the introduction of waferbonding (a waferscale packaging technology) and the decreasing features sizes in back end processing. It is quite possible that the MEMS industry can learn lessons from their semiconductor counterparts and design-in manufacturability and packaging concerns starting with the early prototype concepts.

This chapter focuses on the recent developments in MEMS packaging, as well as discusses the future of this sub-industry. One of the more promising approaches to MEMS packaging appears to be the “Supply Chain Method” and this process is discussed.

## 1 Introduction and Background

Although many activities have been started, to improve the situation, packaging still can be a major obstacle to the commercialization of MEMS devices. Other than the few fully commercialized device types (e.g., air bag triggers, ink-jet print-heads, pressure sensors, and a few medical devices), packaging constitutes the single largest element of cost and a major limitation to the miniaturization potential. This chapter will address both the design and materials aspects and the methods and procedures used.

Robust Packaging is at once an obstacle and an opportunity in the Microsystems and Top down Nanosystems arena. We explain this point by point in the next several paragraphs and throughout the chapter. For instance there are:

1) No standards: Major limitations include the lack of standards and standardized methodologies. This is due in part to a common assumption that more conventional methods and standards used for integrated circuits are “Sufficient,” in part to the need to adapt these methods and standards to develop the required infrastructure for the commercialization of microsystems, and in part to the greater roles, degree of integration, and interfacing of microsystems with their environments.

2) Lack of trained personnel (and lack of MEMS assembly curriculum): Packaging has been a critical but less glamorous and less valued aspect of microsystems development. Much of the current limitation is also attributed to the trade off between company trade secrets and the need for development of the microsystems industry. Packaging relies on systems engineering, and is severely under populated. This skills gap occurs not only for all trained technological

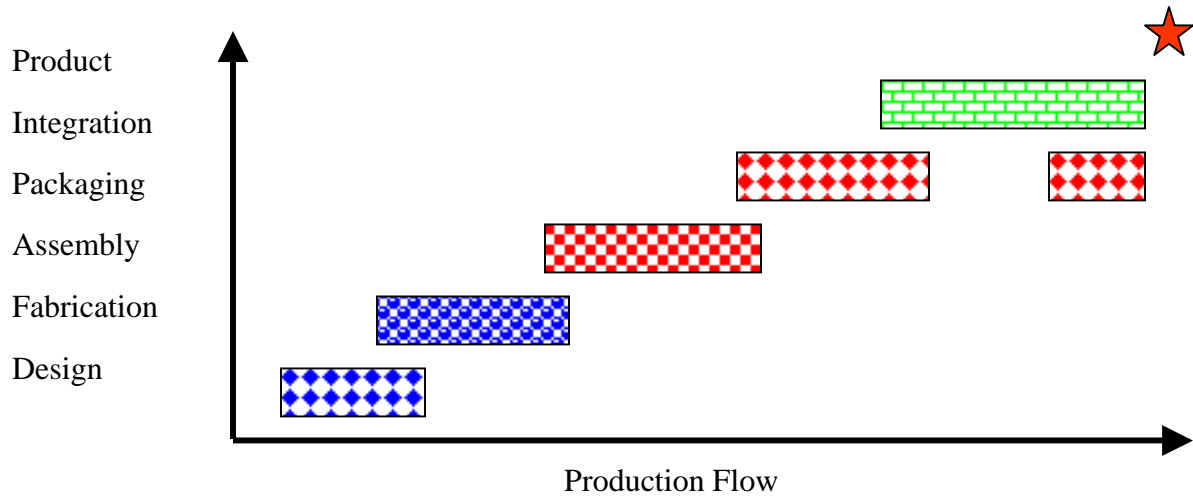
professionals but also for the manager's needed for trained professional personnel in management levels.

This skills gap is being actively met by academia. There is an increasing interest in universities trying to meet this need. The number of universities that now offer curriculums in this area has increased from less than 10 to nearly 50 worldwide in the last 15 years. Schools such as Arkansas, Stanford, University of California Berkeley, Lehigh, Oregon State, Cornell and Albany State, Georgia Institute of Technology in North America, KAIST, City Univ. of Hong Kong, Osaka in the Far East and Fraunhofer IZM, Technical University Berlin, Loughborough University (UK) and Helsinki in Europe have all taken up the challenge.

The two limitations above are compounded by many others including but not limited to:

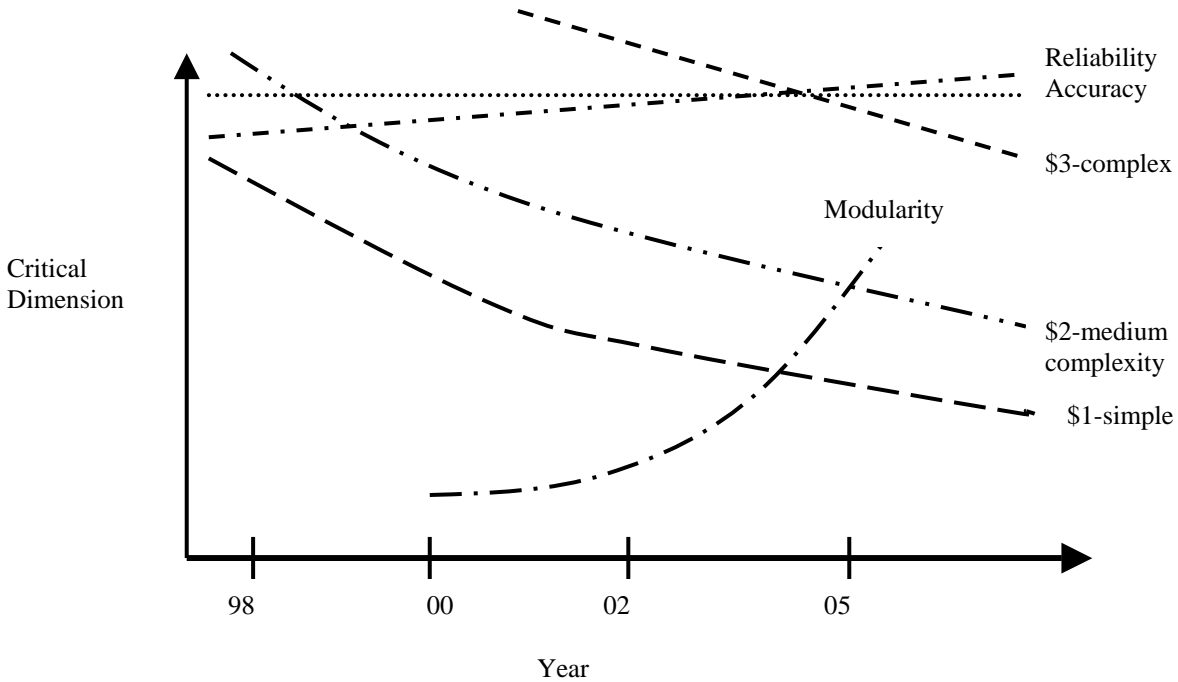
- Being a small customer for several materials, equipment, etc.
- Lack of modeling: materials properties for package materials, package modeling tools, validation of models
- Measurement techniques for materials parametrics (e.g., incoming/outgoing inspection, control charts, etc.)
- Lot-to-lot variability of materials properties
- Coupling of packaging modeling with reliability (and media compatibility) modeling

Packaging includes the materials and design used to encapsulate, protect and interface the MEMS device. It also includes the assembly methods and procedures used to prepare the device for its intended application. Otherwise similar devices may be applied in vastly different environments. As with any measurement device, dynamic range is a critical parameter. For example, a piezoelectric pressure device may be used to measure cryogenics or plasmas- extremely different environments.



**Figure 1. Production Flow Schema for Microsystems**

A general schema for production flow of microsystems is shown in Figure 1. We illustrate the evolutionary role of packaging and assembly as the level of complexity and integration has been advanced. Packaging and assembly options are determined in the design stage and often begin at the wafer level, and continue into the integration stage. Critical factors include cost, reliability, and accuracy. Modularity is an important trend. Trends are shown in Figure 2.



**Figure 2. Trends in Critical Dimensions**

A four level approach is used to describe current thinking, analogous to methods used for integrated circuits, as described in Table 1. This chapter addresses the first three of these levels for MEMS/MST. The system level is considered more conventional and application-specific, thus outside the scope of the road mapping effort.

<b>Integrated Circuit</b>	<b>MEMS</b>
Chip/Module	Die
Card	Device
Board	Subsystem
System	System

**Table 1. A Four Level Approach to Packaging**

Accuracy must be comparable to existing macroproducts, and is essentially a flat line. Reliability must be high, and has shown slow and steady improvement with added operating experience. The important trends shown are for cost (as a percentage of product prices) and

modularity. Costs for “Simple” devices (“\$1”) and those of medium complexity (“\$2”) have shown comparable decreases. Costs for complex devices (“\$3”) have shown more dramatic decreases in part due to the increasing trend in modularity.

Packaging is used to protect and enable the system. Because MEMS is used often in sensor or actuator products, it must interact with the environment, which may be in direct conflict with the desire to isolate the electronics for improved reliability performance. For some very simple devices, performance requirements allow a high degree of isolation from the environment (e.g., stints and accelerometers). Other more complex devices (e.g., chemical and biological analysis systems, particularly in vivo systems) present extremely complex packaging requirements. Packaging serves several important roles, including:

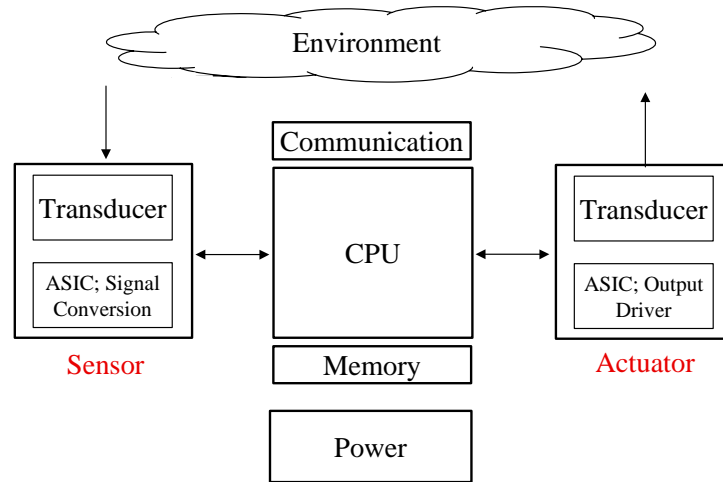
- The provision of feed-troughs for electrical, fluidic or optical interfaces. Examples include optical sensor or switches, fluid / gas pressure sensors etc.
- Environmental management including, hermiticity /outgassing/controlled atmosphere and vacuum. As an example, resonating structures, such as gyroscopes, require control of pressure to <10 mbar. In addition, potential corrosion, condensation of water, change of the beam weight due to impurity adhesion all affect the resultant lifetime of the product.
- Control of the stresses/thermal expansions. Even with the more robust semiconductor chips this is a cause for concern. The highly sensitive MST/MEMS devices necessitate even more stringent control of mechanical properties.
- Management of thermal properties to minimize absorption and/or emission.
- Management of the RF/magnetic/electrical or optical interference and/or radiation properties.

- Maximized reliability/lifetime, where packages must ensure that automotive products, for example, have guaranteed lifetimes of over 12 years.
- Minimized costs and resultant product price. The MST/MEMS component usually is one constituent of a larger module / (sub)system. The cost element of this component is therefore important and must be minimized, particularly if alternative solutions / technologies can be readily implemented instead.

At the same time it must address multi-domain technologies like:

- Structural (including tension, shear, compression and deflection)
- Mechanical (including shock and vibration)
- Electrical (includes static, voltage, current for power and signal)
- Optical (intended wavelengths, field of view)
- Thermal (operating and storage temperatures, thermal shock)
- Chemical (design for intended environment, protect against others)
- Radiation (including EMC/EMI, RFI and nuclear sources).

Microsystems consist generally of MEMS devices, signal conditioning and packaging. Microsystems may provide sensing, actuation, energy conversion, or combinations of these functions. Input/output parameters may include electrical, optical, mechanical, and/or fluids (pneumatic, hydraulic or other fluids). They must be provided with power, except in the case of passive devices, and many require communications with the “Outside World.” Some types simply provide structural strength in critical roles, such as a stint used to reinforce a weakened artery wall. Others provide increasingly complex functions and logical sets of functions. This gives rise to taxonomy to classify devices according to their abilities to “Sense, Think, Act, Communicate, and (get) Self-Power.” (see figure 3) This is described in Table 2, and is described more fully in this works introduction found in Chapter 1.



**Figure 3. Overview of device functions**

Type	Sense	Think	Act	Communicate	Power	Example
1						Stint
2	✓					Temperature
3	✓				✓	Regulator
4	✓			✓	✓	Remote Monitor
5	✓	✓		✓	✓	Alarm
6	✓	✓	✓		✓	Drug Dispenser
7	✓	✓	✓	✓	✓	Lab on Chip

**Table 2. Taxonomy of MEMS/Microsystems**

The types vary in complexity and the required degree of integration from Type 1, which provides structural strength only (e.g., to reinforce a weakened section of artery wall), through the “Lab on a Chip” used to collect and analyze samples and to report results. Current versions of “Lab on a Chip” are principally used in-vitro, but in-vivo products are also being developed. The self-sufficiency required for this latter application adds significantly to the complexity and reliability requirements.

## 2 Die Level

Four steps are commonly performed at the die level as: passivation, isolation, bonding, and sawing (for detailed descriptions of these terms please see the glossary). These are intended to provide protection in handling and in use. Conventional separation of the die from the wafer involves sawing with a high-speed diamond blade while spraying the wafer surface with high-purity water. This method developed for integrated circuits was effective because the critical components on the die are protected from silicon dust and water by surface coatings. MEMS have more complex structures, cavities, moving parts, and a more complex 3D geometry that are easily damaged or destroyed by water, dust, or both. Protection from these must be decided in the design stage. Knowledge of the intended application environment (parameters to be sensed as well as environmental threats) supports the choice of methods and materials.

The use of cavities in silicon die is common practice. A base die and a “Cap” die are used. The MEMS device is bonded to the base die, and the cap is then bonded over the device to form a sealed cavity. The internal atmosphere may be a vacuum or an inert gas, depending on the application. Interface with the “Outside World” is then accomplished using electrical, optic and/or fluid channels through the encapsulated structure. An alternative to bonding the cap to the substrate is the application of a gel coating. Other alternatives include the choice of ceramic or metal cans. Plastic encapsulated microdevice structures (“PEMS”) are less common in MEMS applications due to their limited strength, particularly under temperature extremes, lack of shielding, poor conductivity, and radiation embrittlement.

Passivation includes the use of a protective layer, a coating or an overlay. Protective layers of 2 – 3 microns of organic materials are effective except that they stiffen with age. Die-level passivation materials are most often inorganic: PECVD silicon nitride/oxynitride, silicon

dioxide, PSG, etc. (sometimes polyimide). Coatings, typically a silicon-based gel product, dry and harden, also limiting effective life in many applications. Overlays, generally made of plastics, are more effective in many applications but are more expensive to use and often take more space.

Ideally, isolation provides the required exposure to the intended environment while masking or shielding all unintended environmental characteristics. These may include protection against mechanical, thermal, chemical, and radiation environments where these are not parameters to be measured by the device.

Bonding methods include anodic, solder, epoxies, fusion, glass-frit, and silicon-based compounds. Anodic bonding is commonly used to bond silicon to glass. It provides a reliable bond and may be used to form a hermetic seal. Eutectic solder bonds also provide reliable bonds and may be used for hermetic sealing. These compounds often require treatment of the MEMS device with a very thin (atoms thick) layer of a noble coating to prevent damage or destruction from the soldering process. The higher temperatures required in this process leads to a tradeoff between the allowed temperature and the type of solder used. Epoxy bonding is popular where materials can tolerate the resins and adhesives used, and generally requires much lower temperatures. The downside to these is the loss of strength with aging and the potential for caustic damage to the materials themselves both in manufacture and in use. Silicon-based adhesives (e.g., RTV, Silastic, etc.) are simpler to use, do not require elevated temperatures in curing, and provide protection from shock and vibration, and have cost advantages. The downside to these is that they have no strength in tension and are subject to environmental aging.

### 3 Bonding and Packaging

In many applications sealed cavity or protection against excessive movement is required. In these applications it is important that the bond is mechanically strong and the seal is maintained. Ranges of techniques that are available are listed in Table 3. These techniques are further illustrated in Figure 3. Bonding can occur at both the wafer and die level (flip chip etc.).

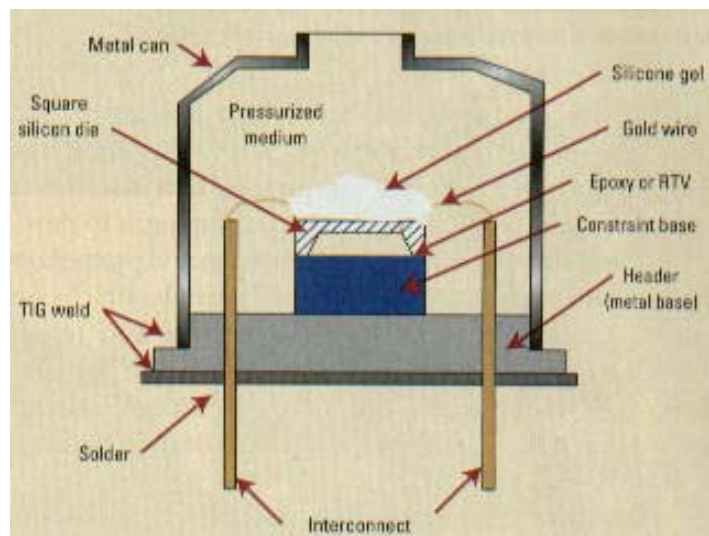
If bonding is to be performed at the end of the processing, the permitted temperature is extremely limited due to the presence of aluminum. For many years, this was a problem for fusion bonding which used temperatures above 1000<sup>0</sup>C. However, more recent developments have brought the bonding temperature down to below 400<sup>0</sup>C, and thus compatible with aluminum. Aluminum is available in many forms having different mechanical properties. Caution is needed in the manufacturing process to prevent loss of these properties by changing the form of the aluminum. For example, aluminum 6061 – T6, a common form used for its structural strength, processed at these temperatures reverts to a form with ~ 20% of its previously rated strength in tension and in shear.

Bonding method	Substrate	Intermediate layer	Temperature [ <sup>0</sup> C]	Reference
Gluing	Si-Si, Glass-Si, Glass-glass	Spin-on adhesives	Room temp	
Low temp. glass bonding	Si-Si	Boron glass	450	[1.22]
Eutectic bonding	Si-Si	Au	370	[1.23,1.24, 1.25]
Fusion bonding	Si-Si	-	>150	[1.26, 1.27]
Anodic bonding	Glass-Si Si-Si Glass-glass	- Oxide -	>250 >850 <400	[1.23,1.28, 1.29, 1.30, 1.31]

**Table 3. Some Examples of Bonding Techniques**

## 4 Device Level

The device level is normally comprised of the MEMS device, power, signal conditioning and compensation, supplemented with mechanical and electrical interfaces to the system. This is an area where modular design is promoting increased performance while reducing size and costs. MEMS interfaces are more complex and comprehensive than microelectronics, and the lack of standardization and standard products has impeded commercialization. Figure 4 shows an example of “Conventional” packaging in a metal can. “Signal” interfaces include electrical, optical and/or fluidic inputs, pressure sensor ports and other physical and energy domain ports as (“Control”), and outputs as (“Data”). Power inputs are either electrical or fluidic, and thermal protection requirements are similar to microelectronic product requirements. Each of these commonly requires compensation for its environment to reliably perform within the device’s operating range.



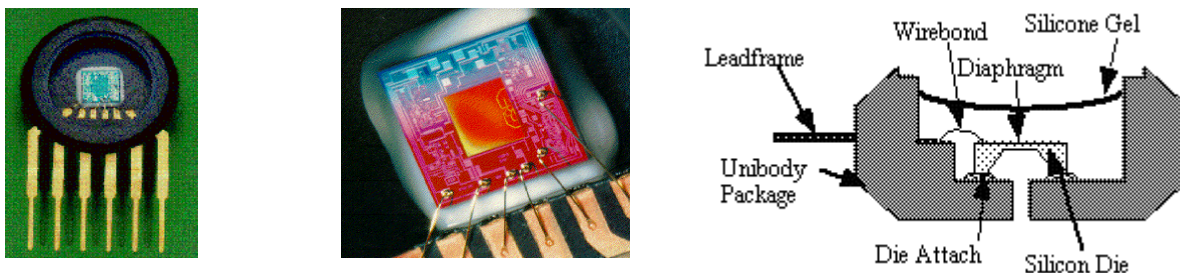
**Figure 4. Conventional Packaging Approach (courtesy Sandia National Laboratories)**

Bonding includes structural, mechanical, hydraulic/pneumatic and wiring attachments to be reliable throughout the specified environmental range; even “Specified Environmental Range”

has not been commonly defined by application. Bonding methods include epoxies and other adhesives, thermal fusion, vapor deposition (physical or chemical), ultrasonic thermosonic, and thermocompression methods.

## 5 Reliability and Media Compatibility

There are considerable opportunities for low-cost MEMS sensors that can withstand long-term exposure in the environments listed above. This ability of a sensor to perform its specified electromechanical function over an intended lifetime in the chemical, electrical, mechanical, and thermal environments is called media compatibility. It is evident that MEMS devices could not operate in the environments listed above without some form of passivation or protection. In most of those environments, the metallic regions of a sensor would quickly corrode resulting in catastrophic failures and in less drastic cases in electrical output alteration. For example, a packaged, bulk micromachined, piezo-resistive pressure sensor has the following metallic regions prone to corrosion: Al lines under passivation, Al bond pads, Au wires, and Au-plated lead frame.



**Figure 5. Photograph of the Motorola Pressure Sensor in “Unibody” Package (left), a Closer View of the Pressure Sensor Die (middle) and Schematic Cross-section of the Motorola Bulk Micro-machined Pressure Sensor in “Unibody” Package (right). (Courtesy Dave Monk, Motorola)**

## **5.1 Thermo-Mechanical Effects**

### **5.1.1 Mechanical consideration**

There are many mechanical considerations for evaluating the design of a MEMS or semiconductor device. Mechanical considerations for MEMS packages fall into one or more of the following four categories: minimization of residual stresses induced during the fabrication of the package; minimization of stresses induced by external loads; reduction of stresses caused by time dependent deformation mechanisms; and prevention of mechanical failure of the package during service. The last issue is of concern for all varieties of semiconductor devices, and considerable effort has been devoted to the optimization of the package designs and packaging materials to alleviate these problems. However, for the assembly of stress sensitive devices, such as pressure sensors, piezoresistive force sensors, or capacitive accelerometers, the first three considerations frequently drive the design of the sensor package.

The reduction of package-induced stresses to the level that will not affect the output is of utmost importance for the performance of MEMS sensors. The task is especially difficult for devices that are designed to measure “Sense” the change in force or displacement (piezoresistive or capacitive pressure sensor), or in the case of the devices that are by design made to be displacement sensitive, such as some of the capacitive inertial sensors.

The MEMS sensors are usually designed to detect extremely small changes of stress or displacement. The high sensitivity of these devices is a much-desired property. To a package designer, however, the high sensitivity imposes very serious requirements regarding the stress isolation of the die. This is why packaging MEMS sensors is a very challenging task: the deformation level usually allowed in most semiconductor packages has to be significantly reduced, below an already very fine resolution of the sensing element. Moreover, it is often not

enough to provide isolation of the die from the deformations caused by changes in temperature and outside forces. The die must also be protected from the changes in mechanical equilibrium due to the time dependent deformation mechanisms that can take place within the package in the absence of the change in outside stimuli. These time-dependent deformations, although very small, may affect the sensor response by causing a shift in offset and/or sensitivity, and, therefore, may compromise the sensor performance and reliability.

### **5.1.2 Vibration**

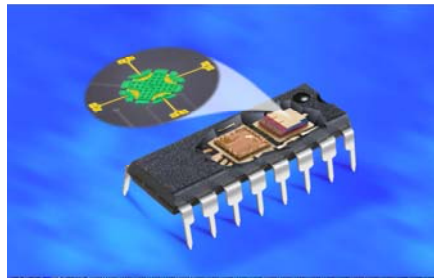
The sensor package must provide efficient transmission of the inertial forces to the sensing device. In the case of an inertial sensor, acceleration transmission must be provided for the full range of operating frequencies. The operating frequency range for an accelerometer is proportional to the fundamental natural frequency of the sensing structure. It is, therefore, important to avoid the resonance effect. Consequently, the fundamental frequency of the package and the whole system represented by the package attached to the printed circuit board should lie outside the intended operating frequency range of the system. This requirement might direct the selection of packaging materials and specifics of package geometry (such as leads length and dimensions). In the case of surface mount packages, the properties and thickness of solder require due consideration.

### **5.1.3 Stress change**

Minimization of the residual stresses in the package and device is an important requirement, and so is the adequate isolation from the outside effects. Reduction of the residual stresses is usually accomplished by adequate material selection and certain processing requirements. The magnitude of these stresses is not of a big concern because the parts are

trimmed after manufacturing and offset and sensitivity is adjusted relative to the stress state. The real problem is a change of stress.

The effect of stress change on the electrical output of a MEMS device is explained here using the example of a Motorola medium g z-axis accelerometer (Figure 6.).

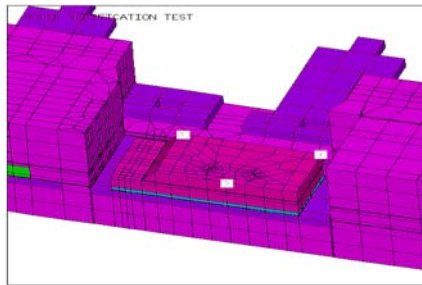


**Figure 6. Motorola Medium g z-axis Accelerometer (Courtesy Dave Monk, Motorola).**

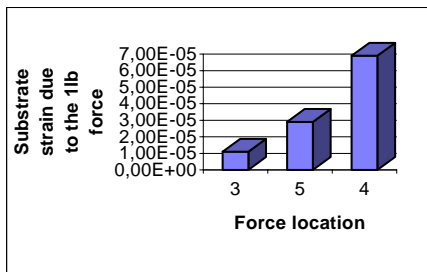
An experiment was conducted to simulate the effect of a stress change, exerted from the package to the sensing die, on electrical output. The 11lb force was applied in a vertical direction at three different locations on the sensing die. The applied load caused deformations of the die, which in turn, resulted in the displacements of sensing trampoline structure and a consequent change in capacitance. In all three cases, the voltage offset was recorded. The same experiment was carried out numerically (Figure 7a). The output of a mechanical analysis shows strains on the substrate where the sensing element was anchored (Figure 7b). The trend of the computed strain is almost identical to the trend of the measured offset (Figure 7c). The changes in the mechanical equilibrium of the package are transferred to the die. These examples illustrate that these changes will be detected by the sensing element and cause a shift in electrical output.

Different counter-measures are usually taken to reduce the stress. These counter-measures are often focused on changes in geometry of the package as well as on the use of alternative package materials. Geometrical considerations primarily include the die placement.

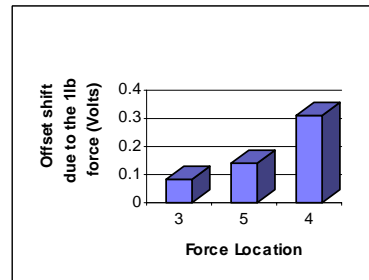
It is generally beneficial that the die is placed closer to the package neutral axis and/or closer to the axis of symmetry. Also, for post molded plastic package usage it would be ideal for a MEMS die to be embedded in a thermoset material and in that way constantly exposed to an almost hydrostatic stress state. However, this is not feasible from the processing standpoint. Because of that, the lead frame flag and die attach are used for placing the die at the desired location.



**Figure 7 (a)**



**Figure 7 b**



**Figure 7c**

**Figure 7. Result of a 1 lb Force Applied at Different Locations on the Sensing Die. (a) The Finite Element Model (the die coat and a portion of the mold compound were removed as it was done in the experiment) (b) Substrate Strain (numerical result); (c) Offset Shift (test result) Elements Introduce Bending in the System. Sometimes Chip Coatings used to Alleviate the Bending Introduce Additional Unknowns into the System.**

Protection from the time dependent deformation mechanisms is a very delicate task. The change in mechanical equilibrium in the package in the absence of outside forces can be caused by different mechanisms. The two most common ones are: creep of materials, and delamination

(or separation) of interfaces. These mechanisms and their evolution are a function of many different parameters. The extent of the creep effects is a result of material properties, residual stresses, and temperature. Delamination and separation of interfaces are complex processes influenced by the residual stresses, temperature, and chemical preparation of interfaces, humidity, and the environment.

Materials with visco-elastic properties are often used in MEMS packaging. Because of their low stiffness these materials enable isolation for the die from the comparatively stiff mold compound and lead frame, but can often undergo creep (relaxation) over time. Creep of package materials can cause drift in electrical output, which means a failure for a MEMS device. For sensors that provide safety functions such as airbag sensors in vehicles, this is unacceptable. Relaxation is a function of many parameters, intrinsic to material as well as extrinsic (temperature and stress). It is a property difficult to characterize and adequately model. Consequently, different remedies have to be utilized to overcome this problem. For example, the problem of device shift due to die coat creep, in the case of the Motorola medium g accelerometer, was resolved in the following way. During processing of the post molded plastic package, a gap is created between the die coat and the mold compound. The gap size varies with temperature. The gap is designed to remain open over the operating temperature range of the device. At a given temperature the gap size is a function of the coefficients of thermal expansions of the materials in the package as well as of the length of the die and the thickness of the die coat. The modeling results of the processing steps involved are illustrated in Figure 8.

#### **5.1.4 Material selection**

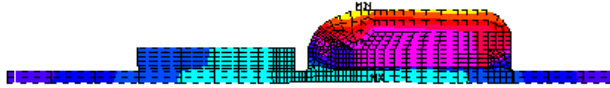
A very important part of the package development is the selection of materials. Thermomechanical parameters that are of the highest importance are: coefficient of thermal

expansion (CTE), elastic moduli, glass transition temperature, filler content, and relaxation properties. Since the temperature change is an outside stimulus important for MEMS packaging, the stress reduction is usually accomplished by selecting materials with similar CTE's.

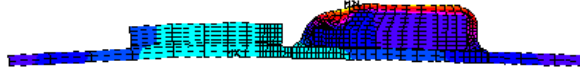
**Step 1: The Die Attach Process**



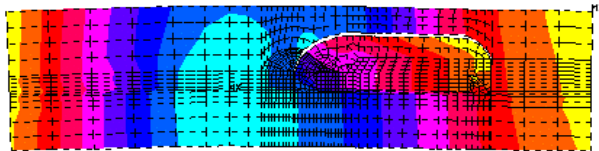
**Step 2: Dispensing and Curing of the Die Coat: T = 150C**



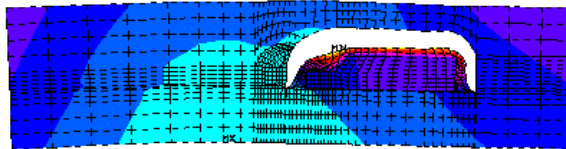
**Step 3: Cooling Back to Room Temperature: T= 25C**



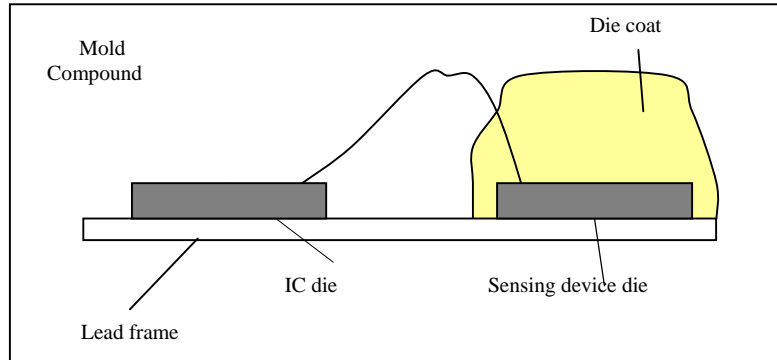
**Step 4: Curing of Mold Compound: T = 160C**



**Step 5: Finished Product: T = 25C**



**Figure 8. Process Steps. Deformed Configurations of the Part at Different Stages of the Manufacturing Process. (Modelling results: colors represent vertical displacements; displacements are exaggerated for clarity).**



**Figure 9. A Two-chip Post Molded Plastic MEMS Package.**

For materials that undergo a phase change, a glass transition temperature can be a very important parameter to consider. A sudden change in phase (i.e., material stiffness) can compromise both the performance and the reliability of the package. For example, in a two chip plastic package inter-chip wires are partly covered by the die coat while the remainder of the wire is in the mold compound. A sudden change in the die coat state from rubber to glass (these are the formal names for the polymeric phases) can cause breakage of the inter-chip wires at the mold compound-die coat interface. For this reason, the selected die coat material should have the glass transition temperature that falls outside the device operating temperature range as was successfully reported.

### 5.1.5 Methods

Design processes for MEMS packages incorporate standard tools and methods used in the design of IC packages. Experimental, numerical, and analytical methods are utilized, depending on type and complexity of the problem. It should be noted that MEMS packaging faces similar problems as standard electronic packaging. The most noticeable one is the absence of theoretical models that would provide better understanding and more comprehensive modeling treatment of certain phenomena. Experimental techniques on the other hand are largely in use. Their

prevalence is a result of several factors: (1) in the electronic packaging field, it is convenient to conduct tests since they can be done on the real size samples; (2) doing destructive tests is fairly cheap, since the electronic parts are inexpensive; and (3) obtaining experimental results is much faster than developing theoretical models. Although useful, experimental results are of a limiting value. Development of theoretical models is a necessity for both a meaningful advance in the electronic packaging field and improvements in cycle time. This is particularly true in the case of MEMS packaging with its specific and delicate requirements for higher precision and lower uncertainty level in package performance.

## **5.2 Chemical Environment**

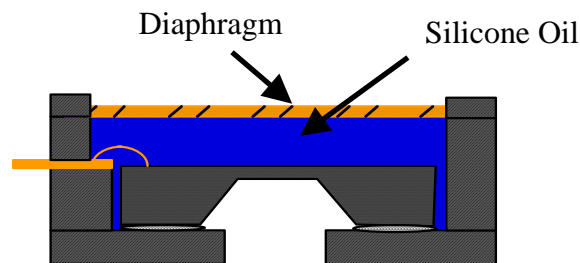
### **5.2.1 Applications**

The ability of the MEMS devices to operate in potentially corrosive environments will be of critical importance in the introduction of these devices into new markets. For example, the most common MEMS sensor is the piezoresistive pressure sensor. The use of this type of sensor along with the flow or chemical sensors could dramatically increase in the automotive, industrial, and medical markets. Traditionally, silicon pressure sensors have been specified for dry, non-corrosive gas environments. However, automotive “Under-the-hood” applications, for example, require the operation in different fluids in the temperature range from  $-50^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ . In addition, some automotive specifications call for an exposure to salt water and/or strong acids. A typical automotive specification includes a mixture of iso-octane and toluene (Fuel C or carburant) often with ethanol or methanol and corrosive water added to it; engine oil, transmission oil, engine protection additives, gasoline, windshield washing fluid, battery acid ( $\text{H}_2\text{SO}_4$ ) vapors, diluted  $\text{HNO}_3$ , etc. White-goods applications most often require exposure to alkaline aqueous solutions (e.g., washing machine). A sensor exposure to pH of 11 solution of

NaOH/NaHCO<sub>3</sub> is an example of an industrial application in water pumps. Medical applications often call for exposure to bodily fluids.

The corrosion mechanism on an unprotected device can be general corrosion induced by bias voltage, galvanic corrosion silicon etching, die attach failure, interconnect failure, and housing material failure. The bias voltage typically used is 5 V and this will enable very high corrosion rates in most of the environments listed above.

There has been a significant body of primarily patent literature on the media compatible sensor design. In the early days of MEMS sensors, media compatibility solutions were sought that were analogous with the traditional IC industry. In a typical IC encapsulation, a thermosetting polymer, such as an epoxy, is applied by overmolding on a fully assembled device onto a lead frame. This kind of protection is relatively simple to apply and it provides reliable protection from corrosive chemicals. However, in the case of pressure sensors, the encapsulation material must allow a direct contact with the environment. For example, the transmission of the pressure signal to the diaphragm and the over-molding process cannot be used. This uniqueness of MEMS devices had led to a plethora of specific methods for achieving media compatibility. The most successful media compatible solutions for MEMS pressure sensors include use of a stainless steel diaphragm and a silicone oil pressure transmission fluid to isolate the silicon (Figure 10).



**Figure 10. Schematic Diagram of the Stainless Steel Diaphragm for Piezoresistive, Bulk Micro- machined Pressure Sensors.**

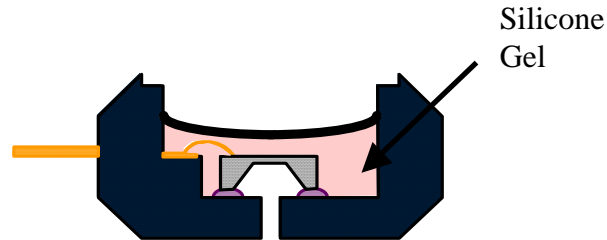
The critical disadvantages using this approach are high cost, increase in the final package size, and limited temperature range. Other diaphragms, such as polymeric diaphragms, have also been used to isolate the sensor from the corrosive media. Several other somewhat elaborate packaging means have been cited in the patent literature. Another technique for developing a media compatible pressure sensor is to use silicon through either a backside exposure (e.g., pressure sensor) or through use of a “Cap” wafer, which would selectively protect metallic areas of the device.

### **5.2.2 Barrier coatings**

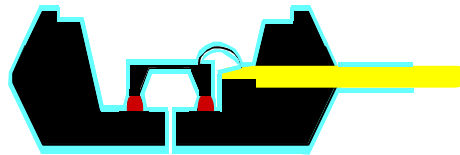
The simplest way to provide protection for a MEMS sensor in a corrosive environment is to use “Barrier Coatings.” Numerous possibilities exist for the selection of the right barrier coating for the particular application, but the most common ones are silicone gels and conformal coatings. Silicone gels are one- or two-part siloxanes that are used to fill the packaging cavity and protect the silicon die and metallic parts of the assembly from the corrosive environment. One part usually comprises a base polymer and a catalyst and the second part contains a crosslinker. When mixed together the gel components cure under a specified regime. These gels are dispensed in thick coatings (on the order of millimeters) and can be dispensed to completely fill the sensor package cavity or they can also be selectively dispensed to critical areas (Figure 11). They have, in most cases, very low modulus, and because of that, have very little effect on the device’s electrical performance. Several vendors provide these materials, each with a slightly different formulation.

Thin, conformal coatings, such as Parylene C, SiC or  $\text{SiN}_x\text{H}_x$ , have found a widespread use for protection of electronic devices from humidity (Figure 12). These coatings are usually deposited in a chemical vapor deposition process in thicknesses on the order of several microns.

Even in these thicknesses the materials can affect the device performance because of their relatively high modulus. The advantage of using Parylene was found in its thickness uniformity and repeatability, the features that allow output adjustment based on modeling.



**Figure 11. A Schematic Diagram of the Motorola Pressure Sensor in “Unibody” Package. The Device is protected with Silicone Gel.**

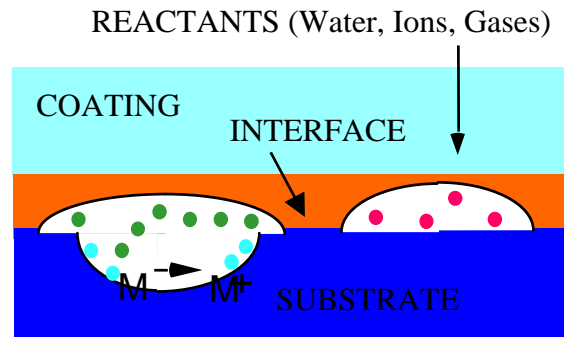


**Figure 12. A Schematic Diagram of the Motorola Pressure Sensor in “Unibody” Package. The Device is protected with a Conformal Coating such as Parylene C.**

### 5.2.3 Failure mechanism

Despite their advantages, barrier coatings do not provide ideal protection in many environments. The most common failure mechanism is corrosion under the coating. The main steps in the overall process are the reactant (water, ions, gases) transport or diffusion through the coating; charge transfer at the interface in an electrochemical reaction; delamination of the coating at the cathodic site; and finally, general corrosion or dissolution of metal at the anodic site (Figure 13). Any defects in the coating accelerate this process, but the diffusion of oxygen, water, and ions is essential for this process to occur. This diffusion of the reaction components can occur through the bulk material or through the coating interface with the device as a result of insufficient adhesion strength.

Despite numerous efforts over the years, the realization of media compatibility for MEMS sensors remains elusive or hitched to very specific applications without widespread importance. One of the reasons for this is the lack of reliable testing techniques for rapid screening of coating candidates and processes and early detection of corrosion failures under barrier coatings. In many cases, the reasons for device failure are very difficult to analyze as they stay unresolved and preclude any process improvements. Very few analytical techniques exist for quantifying the media compatibility of a given device. Some of these methods have been derived from basic electrochemical techniques and used to test the reliability of pressure sensor devices. The development of the reliability engineering techniques specifically for MEMS sensors will be one of the key conditions for the further advancements or breakthroughs in media compatibility solutions.



**Figure 13. A Schematic Diagram of the Failure Mechanism under the Coating Showing the Electrochemical Anodic (metal dissolution) and Cathodic Sites.**

### 5.3 Wafer Level Packaging

In the fabrication of sensors using MEMS technology, efforts have been made to alleviate some of the packaging challenges in the device design and fabrication process itself. In this section, some of the methods and fabrication processes developed to address the challenges for MEMS based devices will be described.

A MEMS device, such as an inertial sensor, has to be protected from the environment not only during the entire process of fabrication, but also in the application environment. Because the sensors, in many cases, respond dynamically to the sensing environment, they are suspended from the substrate and are capable of motion, vertically or laterally. Therefore, at the wafer level, after the completion of the processing, these devices are susceptible to the effects of the subsequent processes of sawing and assembly. There are a number of techniques that have been developed to address this issue.

The issue of protecting the suspended sensor from the saw and assembly operations is typically addressed by a combination of design and process. The specific method followed depends on the technology used to fabricate the sensor. In some processes, the sensor, after being released from the substrate, is again immersed in a readily etched polymer such as photoresist. The wafers with the dried resist are sawed and the device is placed in a package. The photoresist is then removed in oxygen plasma and the device is finally released. Next, the sensor package is covered with a hermetic lid made of metal or ceramic. This method, while being functional, is susceptible to particulate contamination. In addition, the problem of stiction, where adhesion forces are developed during the release process, can also cause catastrophic failure. This problem is addressed in design by using stiff suspensions systems or in processing by using low surface tension films such as self-assembled monolayers or teflon-like polymers.

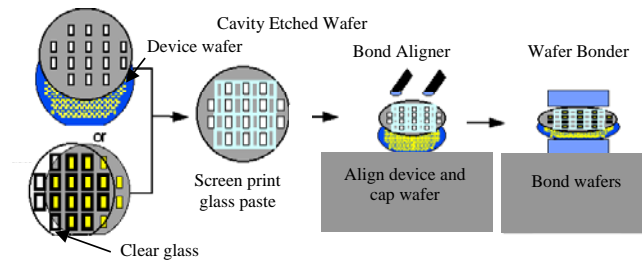
In a number of processes, the released sensor is protected by a cap or cover. This cap is formed at the wafer level using either a planar integrated fabrication process or by an additional wafer made of silicon, glass, or quartz. Some of the requirements for a cap structure are a highly hermetic seal, convenient lead transfer, low cost, manufacturability, and small footprint. The planar cap is formed by using deposited layers such as polysilicon, silicon nitride, etc. In this

case, an additional layer of sacrificial material is deposited on top of the sensor structure followed by the structural material of the cap. As a specific example, an additional sacrificial layer (e.g., phosphosilicate glass) is deposited on top of the sensor structure, which is a surface micromachined resonator. The integrated cap structure is then formed using LPCVD silicon nitride anchored to the substrate. Silicon-rich silicon nitride is typically used since it has low tensile stress and is capable of being deposited to a thickness of 1 micrometer without cracking.

In addition, LPCVD polysilicon can also be used to form the integrated cap. However, additional etch holes used to enable the removal of the entire sacrificial layer must be incorporated in the cap layer. Once the device is released by the sacrificial layer etch, the etch holes or ports must be sealed. Therefore, the etch ports are placed at the periphery of the cap or shell. The maximum distance that can be released using the sacrificial etch process, based on selectivity of the etch chemical to structural and isolation layers, will determine the size of the device. In addition, the effect of ambient pressure on the protective cap also needs to be considered.

A silicon wafer that is bonded to the device wafer is another method used to form the cap structure. A number of methods for bonding the cap wafer have been developed: anodic bond, compression bond, metal eutectic bond, and glass frit bond. In the development of the Motorola z-axis accelerometer, a silicon cap is bonded using a glass frit process. The frit glass wafer bonding technique involves bonding of a micromachined silicon device wafer to a bulk micromachined silicon cap wafer. The cap wafer is produced by patterning and wet etching the silicon substrate to create cavities on the wafer. The cavities allow access to metal bond pads for probe testing. An adhesion layer is used to establish permanent bond between the two wafers and to act as a spacer. A schematic representation of the capping process is shown in Figure 14.

The use of silicon for the cap wafer minimizes the difference between the thermal coefficients of expansion (CTE). It is also important that the CTE of the frit glass closely matches that of the silicon. The frit glass contains a base glass, a refractory filler, and a “Vehicle.” The filler is added to decrease the base glass CTE. It also enhances the mechanical strength and resistivity to crack propagation in the final glass bond. The “Vehicle” provides fluidity and gives strength to the pre-fired glass body. A screen-printing process is used for glass paste application. The wafer is allowed to dry and then glazed at a high temperature to burn off the organic binder and sinter the glass. The cap wafer is then aligned to the device wafer and bonded by applying thermocompression to form a hermetic seal. The two wafers are bonded at temperatures greater than 500°C and under an appropriate bond pressure. When the bond process is completed, the composite wafer is ready for probe. The wafers are then diced through the open cavity where the bond pads are exposed using a saw and assembled using the bonded wafer as the package.



**Figure 14. Schematic of the Glass Frit Silicon Cap Wafer Bond Process.**

## 6 Systems Level P&A

Packaging and assembly at the systems level converges with that required for microelectronics devices for many types of products. Primary differences lie in the number, complexity, and types of interfaces with the application environment and in the size and constraints on handling fixtures and equipment. These are essential elements of the infrastructure that must be borrowed or adapted from the microelectronics industry or developed specifically for Microsystems. MST users must define the environment as well as other conditions required for device utility in order for a systems approach to be taken and then the designers, manufacturers and packagers of a Micro or top down Nano device must work together to provide solutions rather than components.

Modeling and simulation are important tools used to supplement traditional finite element analyses. Tolerances are significant at these scales, and orientation problems may arise. Gravity, the major force in macrosystems, has much less effect at these scales and other forces must be understood and accounted for in the assembly and packaging process.

There is a wide range of application-dependent constraints. These range from hermetically sealed “Simple” devices, such as accelerometers used for air bag triggers, to industrial process sensors that may be exposed to severe thermal, shock, vibration, and radiation environments, to deep space applications with wide variations in temperature, pressure, mechanical, and radiation environments, to in-vivo devices that must survive conditions within the body. In the first case, packaging is simple and is well handled using inexpensive batch processes. In the more complex cases cited, the product function is dependent on controlled exposure to the environment it must sense and interact with while requiring protection from many

aspects of the environment that can readily defeat such functionality. Another important aspect is the period of performance. Some products are required to perform only once and are then disposed of (e.g., some medical diagnostics). Others are required to survive and perform reliably for many years (e.g., many space-based applications, industrial controls, etc.). These factors and reliability requirements challenge the state of the art. Meeting these at a competitive cost has truly delayed commercialization for many applications.

Increased integration at the wafer level has great advantages where production volumes support the nonrecurring engineering costs.

## **7 Standardization of Interfaces**

Key issues include standardization of all interfaces. These include all of the “I/O” described above. MST device users are steadily demanding more standards for their utilization of top down Nano or Microsystems solutions (see chapter 13 for further discussion on standards). Of note are the efforts of the Semi organization in this area. (see [www.semi.org](http://www.semi.org))

Power and signals connectivity with the “Outside World” generally follows standards established for the IC industry, and will probably continue to be adequate for most common applications. Power connections follow copper, aluminum or gold wiring to standardized connector pairs suitable to the rated loads and the application environment. Signals connectivity may follow similarly or may rely on fiber optics for wireless methods; certainly, the latter is more appropriate for many emergent applications, particularly for in-vivo applications. This raises the issues of electromagnetic compatibility (EMC), electromagnetic interference (EMI), and radio frequency interference (RFI) in the design and implementation of microsystems that require

communications as a key feature. As with all microelectronics devices, proper grounding is also required to prevent the catastrophic effects of static charge buildup and transients.

Fluids I/O also require the development of standardized connectors. These are not generally emerging from the IC world, except for some larger chips that use coolant plumbing. Recall that the list of fluids included gasses and liquids, and that applications must consider fluid type, pressure, temperature, flow and chemical toxicity and/or causticity of the materials. Many applications will require fine filtering with self-cleaning features to prevent improper functioning or early failures. Flow channels may require internal isolation from the remainder of the microsystem, a common practice on the macro scale requiring design practices and packaging and assembly methods not common on the micro and nano scale. Standardized connectors and “Piping” must be developed for a range of application parameters.

Shielding from threats within the application environment is a primary requirement in the packaging design and materials selection. Recall, the microsystem must have a well-defined interface with the measured or controlled parameter(s) in its environment, and be adequately isolated from all other parameters that could cause interference or damage. It is commonly recalled that some early ICs were so sensitive to electrostatic discharge that they were destroyed in the act of removing them from their shipping materials. Some MEMS applications are in high-powered RF and laser equipment, and will require special attention to proper shielding design.

Mounting methods are also needed for many applications. The microsystem must be securely attached with the proper orientation to function in its intended environment. It then often requires protection from thermal, shock, and vibration in its environment.

## 8 Packaging Strategy and Trends

A significant amount of attention is now being directed at packaging concerns for the MEMS community. Packaging was an afterthought for most MEMS designers and manufacturers only a few years ago. Now it is part of the initial design process (see the Design, Simulation and Modeling chapter for further insight). Today inputs to packaging strategy for MEMS devices can be summarized with the following list:

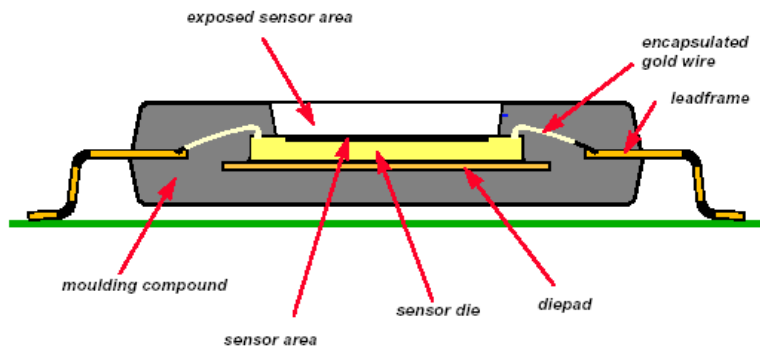
- 1) Reduce the overall system cost.
- 2) Provide differentiated package solutions.
- 3) Improve system robustness.
- 4) Reduce the time to qualify new packaging concepts.
- 5) Maintain and execute a component packaging roadmap with key customer inputs.
- 6) MEMS device and package design must be concurrent activities
- 7) MEMS users and manufactures must understand the key cost role that MEMS packaging adds to MEMS devices.

The question often asked ten or more years ago was “Can we package this device now that we have created it?” This question has been transformed into: “Which of the standard package concepts available will we chose for our product?”

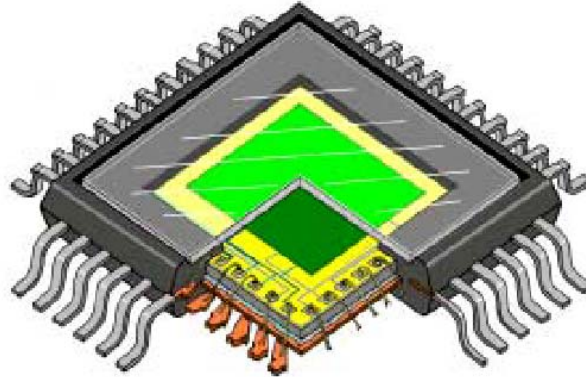
Although MEMS/MST production processes are, to a high degree, application-specific, some standard concepts are, gradually, coming into existence, including, two which are based on high volume electronics (plastic and ceramic packaging), and one more specifically related to MEMS/MST. Some major concepts are briefly described below, using examples supplied by commercial packaging and assembly providers.

### 8.1 Semi-standard packaging – adapted plastics concepts

Initially, plastic molding processes were regarded as fundamentally unsuitable for MEMS/MST due to the fact that the processing conditions are too harsh for these, often, very sensitive devices. In addition the need for other interconnections, such as optical or fluidic, or the need for hermeticity - as in accelerometers etc. - prevents the straightforward application of this technology. However a number of manufacturers have found solutions for those problems. One of these is Eurasem: they maintains the active sensor area open during moulding, through the use of a special nodule, which gently presses on the chip surface. The nodule prevents fluid compound reaching the sensor area during filling of the moulding cavity. In this concept the whole die, including the gold wires, is covered by the moulding compound. (see Figure 15) This results in good mechanical protection and comparable reliability properties as standard packages. Depending on the application, this opening can be covered by a lid. (see Figure 16)



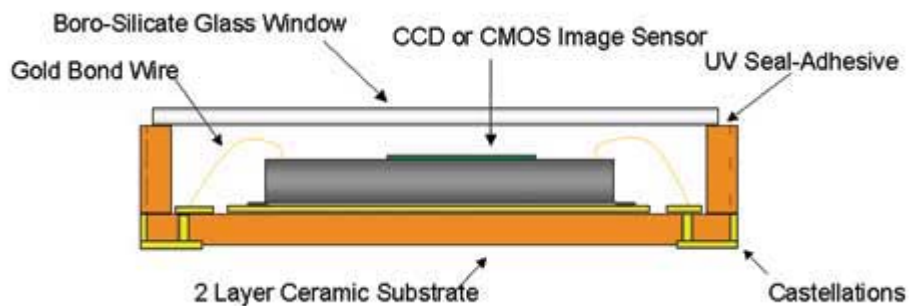
**Figure 15: Cross section of a moulded cavity package (courtesy Eurasem BV)**



**Figure 16: Plastic package with optical lid (Courtesy Eurasem BV)**

## 8.2 Semi-standard packaging – adapted ceramic concepts

Ceramic packages are ideal when stress is a concern, as is the case with many MEMS/MST products. In addition, small volume production is possible without high set-up cost. Following placing and fixation of the die in the package cavity, wire bonding ensures electrical interconnection and the cavity can, subsequently, be sealed by a lid. The lid can also be transparent for optical applications.



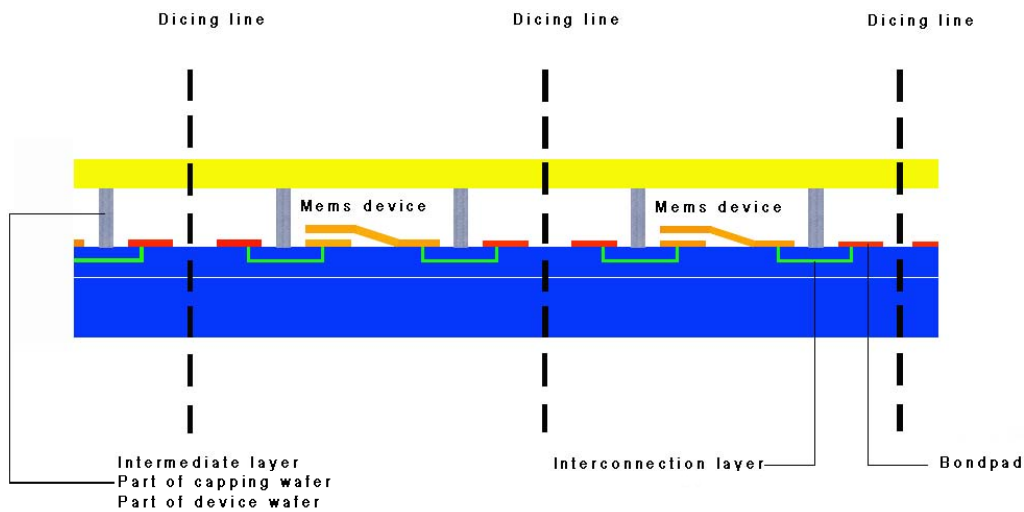
**Figure 17: cross section of a ceramic package (courtesy Amkor Technology)**

## 8.3 Waferscale packaging

Waferlevel packaging is becoming a key enabling technology, bringing front and back-end processing together. This technology and the related technologies of 3D packaging are of increasing importance in both semiconductors and MST/MEMS. Where for semiconductors the

benefits lay in minimizing interconnection lengths and decrease of package volume, for MST/MEMS the benefits include:

- Multi die processing
- Protection of the die during assembly
- Potential of short electrical interconnections



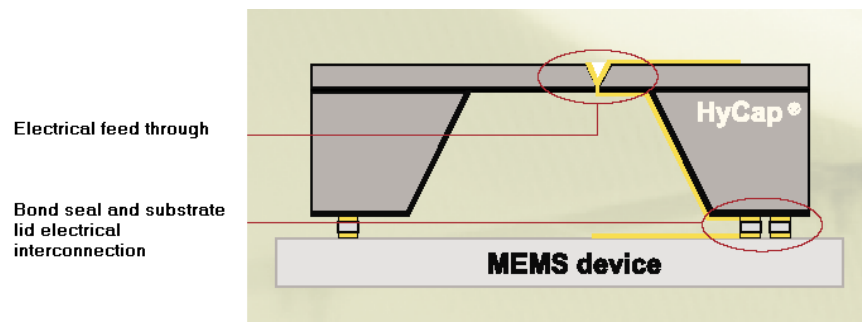
- Potential of added functionality in the capping wafer.

**Figure 18: Schematic view of bonded wafer stack (courtesy enablingMNT)**

As a last step in the wafer processing, the wafer is covered by a protective cap, hereby protecting the sensitive sensor area before the dicing process. This can either be done by placing individual lids on top of each sensor, or placing a second wafer with preformed cavities on top of the sensor wafer. (See Figure 18) The main advantage lays in the fact that the sensitive and fragile sensor is protected during the packaging and assembly process. It is also attractive while the process is waferscale, which is in potential more cost effective compared to die scale processing.

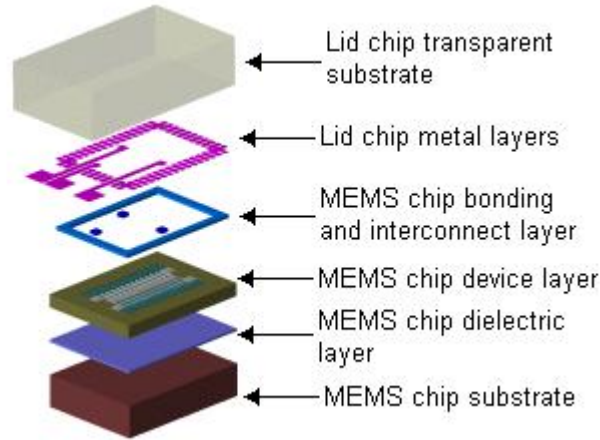
Electrical interconnection is a particular problem for waferscale packaging, as the bondpads are hidden by the capping wafer. One option is to provide access to them via the scribelines. Another option is to make electrical interconnections via through holes either in the capping wafer or in the sensor wafer.

Through the cap interconnection is used by Hymite (see Figure 19) The company utilises a capping wafer featuring cavities and sealed through holes. Hermeticity of the sensor or actuator is secured by solder seal rings that are made in the same process as the electrical interconnection of product wafer with the capping wafer. The end product is delivered with solder bumps for ease of assembly.



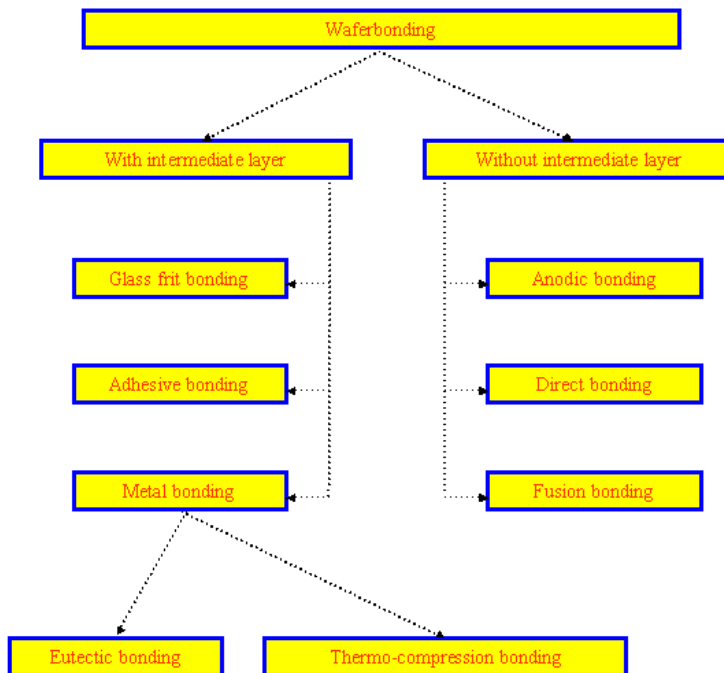
**Figure 19: Cross section of cavity and feedthrough in silicon cap (courtesy Hymite A/S)**

A similar concept is used by MicroAssembly Technologies. Their waferscale bonding process is based on metal to metal bonding (see Figure 20).



**Figure 20: Exploded view of bonded optical chip (courtesy MicroAssembly Technologies)**

Soldering is only one technology for bonding wafers. Several others are proposed. (see Figure 21)

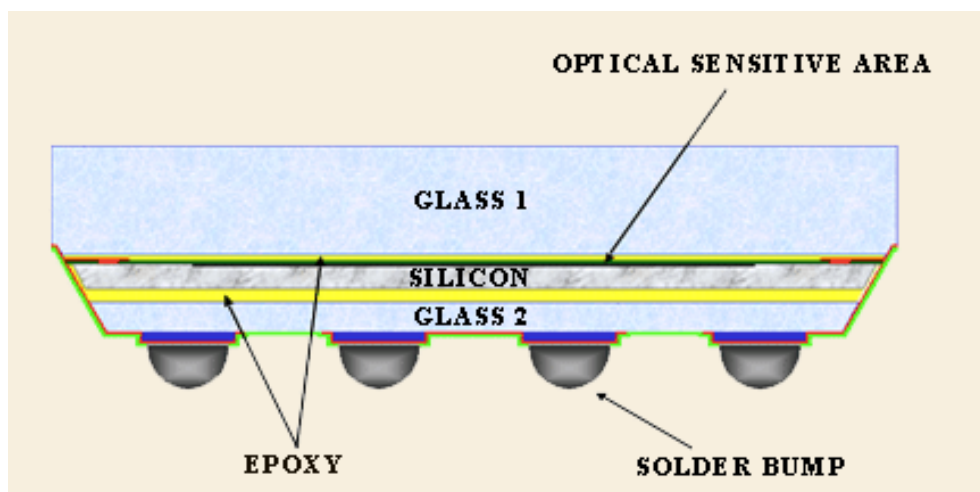


**Figure 21: Waferbond technologies (courtesy enablingMNT)**

In general bonding with an additional layer is advantageous when a cavity is wanted. The extra material to be added to the product can lead to reliability problems or having its influence on performance.

In most cases the interconnecting layer is not conductive and another way has to be found to make the electrical interconnections.

The first option is exploited by Shellcase as shown in figure 22.



**Figure 22: Waferscale packaged product (courtesy Shellcase)**

Above technologies are in principle generic and can therefore be used for then one customer or in different applications.

It has been claimed (Jeffrey C. Demming, Editor, Advanced Packaging, July 2001) that the year 2001 marked the convergence of wafer fabrication with packaging processes. Our contributors see this “Convergence” as a matter of degree. This is an important trend dependent on advances in several supporting technological advances. The culmination will be increased performance at lower costs and improved reliability for a growing range of products that reach commercialization.

Recent trends reported include: increased integration of modular designs, including specialized machines to increasingly optimize assembly steps; packaging on the wafer; chip scale packaging; variations on Ball Grid Arrays; stacking of multichip modules; “Bumping”; “Indent-Reflow-Sealing (“IRS”)”; and supporting methods for thermal management and assembly automation. These are discussed briefly in the following paragraphs.

Henne van Heeren noted in COMS 2000 that a “Supply Chain” approach is needed for cost-effective packaging and assembly. The process should involve project definition (i.e., performance specifications development), design, foundry work, and suppliers. He advised “Forward Integration,” describing this as performing steps as early in the process as can effectively be done.<sup>1</sup>

There continues to be a lot of talk about “Self-assembling,” but little to show for it. One major thrust for MSTs has been for development of assembly process devices to support the IC industry’s continued automation.

Single chip modules (SCM) are sufficient for many applications. Multichip modules (MCM) are emerging as the level of integration supports increased functional performance. A popular practice for increasing functional density with minimized volume is the “Flip Chip.” This provides silicon “Real Estate” on both sides of the chip and increases the area for interconnections. An important advantage is the ability to provide greater isolation between more sensitive components (e.g., ICs) and fluids; the substrate forms the protective barrier with controlled penetrations to preserve the isolation.

“Wafer Bumping” is another emergent trend. Flip chip’s origin was not a package type (like BGA). Flip chip describes the method of electrically connecting the die to the package

carrier. The package carrier, either substrate or lead frame, then provides the connection from the die to the exterior of the package. In "Wire Bonded" packaging, the interconnection between the die and the carrier is made using gold wire. The die is attached to the carrier face up, and then a gold wire is bonded first to the die, and then bonded to the carrier. After redistribution, an under bump metalization pattern defines the bump array which receives printed-on solder paste or electrodeposited solder. The interconnection between the die and carrier is made through the conductive solder bump that is placed directly on the die surface. The bump modified die is then "Flipped Over" and placed face down, with the bumps aligned to the carrier package or PWB substrate.

The most common packaging interconnect is solder, typically eutectic compositions. The trend is to assemble at the wafer scale with a high thermo-cycle bump that can endure subsequent re-flow cycles as a packaged device is exposed to multiple assembly re-flows during integration into a system. The solder bumped die is attached to a substrate by a solder re-flow process. After the die is soldered, under fill is added between the die and the substrate. Under fill is an epoxy that fills the area between the die and the carrier, surrounding the solder bumps. It is designed to distribute the stress in the solder joints. Once cured, the under fill absorbs the stress, reducing the strain on the solder bumps, greatly increasing the life of the finished package. In a wafer scale package the under fill also provides hermeticity. The chip attach and under fill steps are the basics of flip chip interconnect. After wafer bumping, the package assembly surrounding the die can take many forms and can utilize existing IC manufacturing processes and package formats along with MEMS specific interconnects that must accommodate gas and liquid flow

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<sup>1</sup> van Heeren, H., XXXX, (presentation 92), COMS 2000, September, 2000, Santa Fe, NM

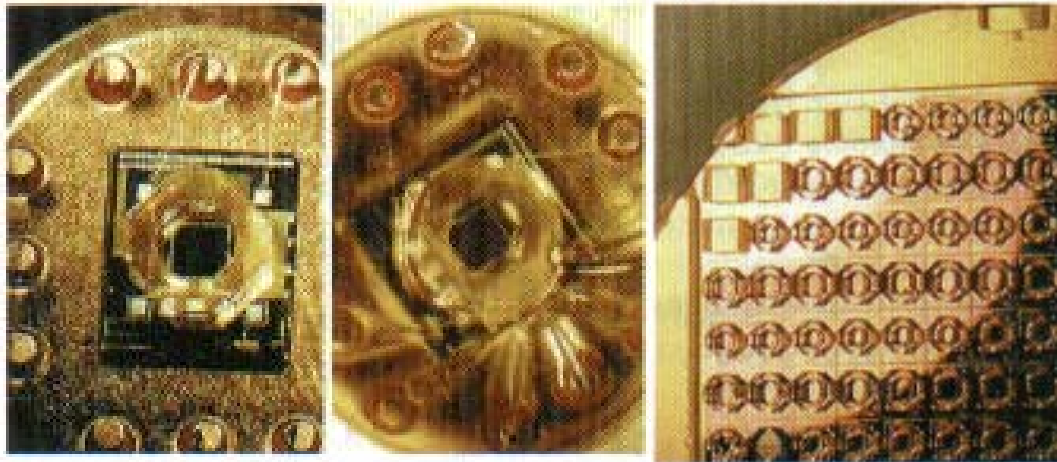
conduits as well as optic ports to provide a true single step mount in the assembly hierarchy. Solder bumps are used to provide controlled separation between layers.

#### **8.4 Modular Packaging and Assembly**

Monolithic integration has been touted as the “Holy Grail” for packaging but has not been achieved for many complex devices (see the Integration chapter for an in-depth discussion on this point). Hybrid microsystems are still the dominant packaging solutions for most microsystems applications. The trend is towards increased integration at the wafer level, reducing costs and size while increasing yield. These benefits accrue in production quantities that must be sufficient to offset the increased costs to develop the production capabilities.

*“The trend to higher integration in microelectronics and the integration of micro mechanical, micro fluidic and micro optical components in mainstream applications ... requires a new type of micro system. The full-custom designed system which is especially developed for a low volume application cannot be a sufficient solution.”<sup>2</sup>*

This quote leads an article describing results and current status of a German program sponsored by the German Ministry for Education and Research and supervised by the German Machinery and Plant Manufacturers Association (VDMA). There are MEMS application kits available and modularity of MEMS packaging solutions to meet environmental and sensing application needs. It is a trend that some of our contributors see as the wave of the future while others see this as unrealistic. A catalog of modules has been developed. The “MEMS Supplier Kit” categorizes four classes of “Integration Elements” that have been developed by Grosser, V., Reichl, H., Kergel, H., and Schuenemann (see MST News February, 2000). Wafer level packaging activities by Sandia National Laboratories are shown in Figure 23.



**Figure 23. Wafer-Level Packaging Example (Courtesy of Sandia National Laboratory)**  
**(a) Showing Sensor with Prepackaging Silicon Wall Structure on TO Header**  
**(b) With Silicone Gel Covering Wire Bonds**  
**(c) Wafer of Prepackaged Sensors.**

### 8.5 SiP - System in a Package

The automotive and appliance industries are driving this mass-production multipurpose device concept. SiPs are packages with multichip or few-chip packages with “Passives” contained within the package. Different applications interface the functions selected, and may employ proprietary embedded software to customize the performance from use of SiP devices.

### 8.6 Multichip Module (MCM) Assembly

Although many MST/MEMS devices have been developed with technologies similar to and sometimes even compatible with semiconductors, monolithic integration is not always practical. Therefore, another form of integration technology is necessary. Multi Chip Modules (MCM) can be regarded as an interesting alternative. MCM provides a MEMS solution that:

- 1) Increases flexibility for MEMS device application
- 2) Provides a potential for a higher pin count to the outside providing more I/O
- 3) MCM can drastically reduce the size of mini and macro systems

4) Reduces the interconnect inefficiencies as compared to macro and mini solutions thereby increasing speed and reducing power consumption

5) Reduces the overall connection count when compared to a macro system  
Reduces electronic noise by reducing the length of interconnects when compared to macro and mini systems.

The following technologies dominate the MEMS MCM packaging platforms:

- 1) MCM-L or MCM Laminate Technology
- 2) MCM-C or MCM Ceramic Technology
- 3) MCM-D or MCM Deposited Technology
- 4) MCM-S or MCM Silicon Technology
- 5) Mechatronics Packaging Technology

## **9 Assembly for MST/MEMS in General**

MST/MEMS components demand that the assembly equipment must be able to grip small (and often delicate) objects and place them with tolerance accuracies that reflect the features sizes of the constituent elements of the structure. In addition, in order to achieve economic processing, either very fast or multiple processing is required. As an example from the semiconductor industry, which demonstrates this fact, currently available die bonders can place approximately 1000 units per hour.

Comparing the semiconductor industry characteristics with those for MNT, it is possible to establish that:

- In general placement of the products needs only tolerances in the order of tens of microns, while electrical interconnections are very tolerant to alignment inaccuracies.

- The assembly of electrical components is in essence a 2D process; the object is nearly always placed on a flat surface.

- There is a high degree of standardization in this industry.

Whilst for MST/MEMS, the industry characteristics are:

- Placement accuracies in the region of microns and even below is usual
- Often 3D processing is required
- Application and often even customer specific products overshadow standards.

It is seen from this that the challenges for this industry lie in the need for more flexible micro assembly tools, capable of working in three dimensions.

Another challenge relates to the low production quantities required during the initial phases. This makes the purchase of dedicated equipment difficult to justify. To help the industry some equipment suppliers (Palomar, MA3) offer assembly services in addition to the sale of equipment. Many other companies, traditional assembly suppliers, foundries and design & engineering companies are also offering services in this area.

Others use equipment from neighboring industry segments or home-built equipment. Examples of a closely related industrial equipment business are flip chip bonders and optical assembly equipment.

Assembly, even more than packaging, needs very much application specific technologies, a few typical examples are discussed briefly below.

## 9.1 Photonic assembly

The major challenges that are uniquely associated with photonics packaging relate to the extremely tight assembly tolerances and the difficulty of handling fragile optical fibers during a volume production process and/or testing.

The first step in packaging such devices is, generally, pre assembly: device testing and sorting, in which initial performance characterization, inspection, burn-in, and sorting, is carried out.

The next step is package assembly— placing the components into a package or onto a submount prior to making the optical connection. Tolerances are typically in the region of 10 to 50  $\mu\text{m}$  level for these types of placements, and automation systems with machine vision can ensure repeatable high yields.

Optical assembly follows. Here the requirements are extremely specialized alignment and attachment processes that will maintain the alignment during both assembly and in the field. Generally, there are two different concepts used to achieve precision alignment:

Active alignment whereby active optimization is achieved by powering up the device and monitoring the coupled power and optimal alignment can be obtained by manipulating the parts using a precision stage. The part is then fixed by adhesives, laser welding or soldering.

Passive alignment: by carefully choosing the tolerances adequate for coupling to be achieved. Vision-assisted positioning systems can achieve passive alignments with accuracies of approximately 1  $\mu\text{m}$ .

Using the correct materials and concepts, minimizing the dimensional changes during curing and during the life of the device and, due to that, robust coupling and operation is

achieved. Controlled thermal management is also an important issue needing consideration. Active cooling is, in some very special cases, used. EMI shielding for the devices typically operate at high speeds.

Optical components must be hermetically sealed after alignment. This is often preceded by a bake out, which reduces or even eliminates moisture and contamination. Bake out is then followed by backfill with inert gases such as argon or nitrogen.

Another unique and highly challenging aspect of packaging optical versus electronic products lies in the optical fiber. Here designing package and manufacturing flow to minimize handling is critical.

## **9.2 Medical Assembly**

Assembly (and packaging) for medical applications provide their own rules and regulations, particularly for implantable devices. Biocompatibility and reliability are only two of the major items to be addressed.

Size is also an important parameter, not so much because of limited space in or outside the body, but because of the following reasons:

- Cosmetics / aesthetics
- Energy consumption
- Enabling minimal surgery.

## **9.3 High Precision Assembly**

The following are a few examples in the area of high precision assembly techniques:

Opus, specializing in semi automatic flip chip bonding for the opto-electronic industry, is able to supply “pick and place” tools for small components with an accuracy of +/- 1 micron.

Sporian, offers a unique and ingenious use of solder to “self-assemble” two-dimensional surface MST/MEMS based structures into useful three-dimensional structures. With this combined joining and assembly approach, the surface tension forces in molten solder serve to assemble the individual parts of each structure. Upon solidification of the solder, the individual parts of the structure are permanently and reliably joined. Using this technology, thousands of, precise, assembly actions can be performed simultaneously with a single batch reflow process.

Hybrid Micro Technology, as many others, uses flip chip technology for precise assembly. To obtain good pre-alignment, the company applies micro vibration. The resulting accuracy is: horizontal:  $<+/- 0.5$  micron, vertical  $+/- 0.3$  micron.

MicroTec specializes in the mass production of miniaturized optical components. These components are fabricated using a process of layer by layer laser hardening of liquid polymers. Resolution achieved is as low as 1 micron, but there is a trade off between resolution and production efficiency. Typical materials used are acrylics and epoxies, which are chosen based on the required properties, i.e. basic or neutral, hydrophobic or hydrophilic, for life science, transparent for optical applications and others. Assembly is facilitated by the fact that during fabrication the part and the production process can be stopped and a new part can be added, and the production continued, providing fixture and sealing or only fixture for the added component.

#### **9.4 Assembly for Liquid Sensing and Processing Products**

For the quick, flexible configuration of micro-fluidic systems Bartels Mikrotechnik has developed the special MFC (“Modular Fluid Concept”) components library. In MFC, the individual function elements are kept ready as a mask and defined in such a way that they can be

incorporated into a plastic body in a modular manner one after another. Standardized connection channels can then connect a number of levels of the structured elements into a complete system.

*Micro chem labs represent a very high level of capability essential for chemical and biological processes. Concurrent trends are pursuing Point of Care (POC) systems to enable “Real-time” diagnoses in the doctors’ offices and clinics, reducing the common practice of over prescribing antibiotics. There are military and public safety interests as well in the rapid detection of biological warfare, environmental toxins, and epidemics. These systems will require very hardy packaging and robust communications capabilities.*

## **10 Packaging and Assembly Services**

Until recently specialized packaging and assembly suppliers were underrepresented in the MST/MEMS area. The growing volumes triggered several companies to develop more or less standard technology concept, aimed at the MST/MEMS producer. The market for outsourcing is therefore rapidly growing. The diversity offers ample opportunity for small companies sustaining specialized technology platforms. Besides that, large traditional package suppliers are adapting their products to enable the MST/MEMS community to use their proven and cost effective concepts.