6

Equipment And Tooling For MNT

Chapter Leaders

Patric Salomon
EnablingMNT
patric@enablingmnt.com

Scotten Jones
IC Knowledge
info@icknowledge.com

Henne van Heeren
EnablingMNT
henne@enablingmnt.com

Job Elders
C2V
job.elders@c2v.nl

Contributing Authors

Kees Eijkel
Mesa + Institute
c.j.m.eijkel@el.utwente.nl

Srikanth Varma
University of New Mexico
srikanth@unm.edu

Bruce Kirchhoff
New Jersey Institute of Technology
kirchhoff@njit.edu

Michael Mignardi
Texas Instruments
m-mignardi@ti.com

Other Key Contributors: Tony Rogers (AML), Peter Dijkstra (Adixen), Johann Weixlberger (EVG), Twan Smetsers (MA3solutions), Carolyn Short (STSystems), and Joe Brown (Suss Microtec).

Numerous MANCEF members have contributed to this chapter this group along with the leaders were the authors

Executive Summary

The emerging markets for MST/MEMS (Micro Systems Technologies / Micro-Electro-Mechanical Systems) products created a demand for specialized equipment. The first to fulfill that demand were suppliers of tools including Deep Reactive Ion Etchers (DRIE), waferbonders and backside aligners. Those companies (STS, Alcatel, EV Group and Suss Microtec) are dedicated MST/MEMS suppliers are still in the forefront of this market. Spin-offs from universities were started to fulfill (niche) demands, whilst established companies entered this arena at a later stage, offering adapted processing tools developed for other industries, such as, those specializing in thin film processing. More interestingly, even the (large) semiconductor equipment manufacturers have begun to show an interest. Within this context, there is now available a mixture of general equipment facilities, designed and developed for other applications such as semiconductors and also equipment adapted or specially tailored for Micro-Nano Technologies (MNT) production.

This chapter categorizes the equipment market into the following, general, areas:

- Front end equipment
- Back end equipment
- Nanotechnology equipment
- Test and measurement equipment

Front end equipment as a term, generally, refers to equipment used to process wafers within a waferfab facility. Test and measurement equipment, on the other hand, combines the collection of instrumentation used to control and maintain the product’s quality. The definition of the back end equipment group is taken rather broadly as it covers equipment for assembly, packaging, material processing, moulding and other similar capabilities.

We investigated the market status of equipment suppliers servicing the nanotechnology industry in terms of production and fabrication from an MST/MNT perspective. This review invariably addresses the pre-production and experimental / trial plants claiming a capability in nanotechnology. Although equipment for nanotechnology, dedicated to research applications, is already on the market, it can be stated that the market for nanotechnology production equipment is still at the beginning of its lifecycle.

For the purposes of this review, nanotechnology is defined as a set of capabilities directed towards the development and manipulation of structures at the atomic scale (100 nm or less). Important developments in areas that either overlap with and/or influence the progress of nanotechnology, such as semiconductor lithography and direct writing, are also discussed in this chapter.

Unlike electronic devices, where only electrical parameters need to be tested, MNT devices require precise measurement of multi domain parameters. In the case of mechanical microsystems, the static and dynamic behavior must be investigated in such a way that the measurement does not interfere with the performance of the device. The two most critical area in testing of micro and nanotechnology are: identification of the Known Good Dies and measurement of material properties. In conclusion: availability of equipment dedicated to the needs of the MST/MEMS market is essential for the successful commercialization of our product applications.

1 Introduction and Background

The emerging markets for MST/MEMS (Micro Systems Technologies / Micro-Electro-Mechanical Systems) products have created a demand for specialized equipment. The first to fulfill that demand were the suppliers of dedicated micromachining processes and tools for microsystems (MST/MEMS) such as Deep Reactive Ion Etchers (DRIE), waferbonders and backside aligners. Companies such as STS, Alcatel, EV Group and Suss Microtec are still at the forefront of this market whilst, spin-offs from universities and companies also began to fulfill niche demands. The more established companies entered this arena at a later stage, offering adapted processing tools developed for other industries (e.g. those specializing in thin film processing). More interestingly, is the fact that even the (large) semiconductor equipment manufacturers have started to show an interest. The established MST/MEMS equipment companies now start to complete their offer by introducing other equipment aiming at the MNT market around their leading ones. As an example, Suss Microtech extended their lithography line with equipment for nanolithography and spaycoating (see figure 1).

Figure 1: Suss Microtec spay coating tool

Within this context, there is now available a mixture of general equipment, designed and developed for other applications such as semiconductors and also equipment adapted or specially tailored for Micro-Nano Technologies (MNT) production.

The MNT equipment market can be categorized into the following, general, areas:

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- Back end equipment
- Nanotechnology equipment
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MEMS and thin film MST are generally the premise of front end processing - the process used to transform the wafer into components. Together with micro assembly, handling, positioning and fixing MST/MEMS (sub) products form the basis of back-end processing. Historically front and back end processing were sharply divided, wafertest and final inspection being the last steps in the front end process and dicing the first step in the back end process. The borderline is becoming vague (see also figure 2) with the introduction of waferbonding (a waferscale packaging technology) and the decreasing features sizes in back end processing.

Testing is getting more and more attention lately, and a number of companies are now introducing specialized equipment to this market segment with its specific demands related to the non electrical signal handling and non standard dimensions.

Equipment for nanotechnology, the latest offspring of technology, needs again another set of equipment. This part of the MNT equipment industry is the less well developed but fast rising in importance.

Whatever technology path is chosen, it is safe to conclude that most will require expensive process equipment and capital infrastructure as well as highly qualified and experienced engineers for setting up the designs and process flows.

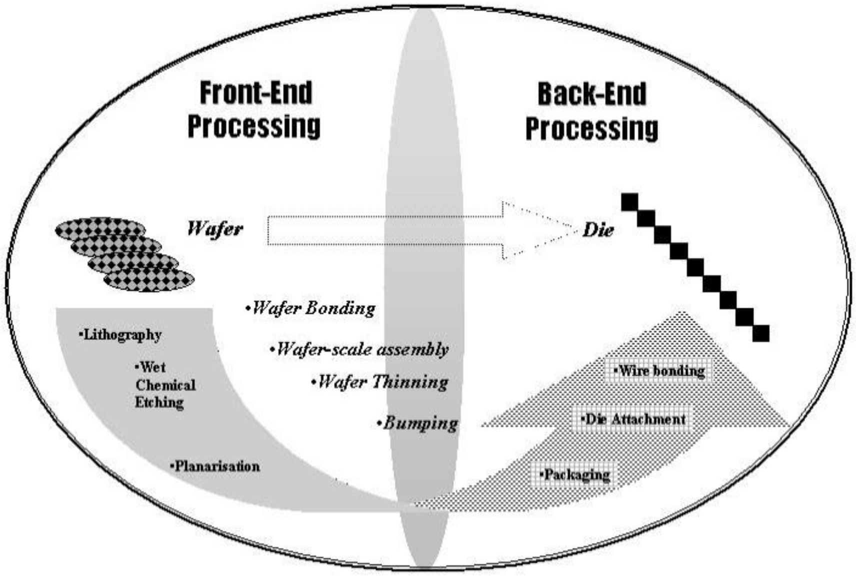


Figure 2. Processes crossing the borders between front end and back end processing

2 Strategies of Equipment Suppliers

The global market for MST/MEMS specific equipment is at about $0.73 B. The relatively large expenditure on capital invested in front end equipment in the past has clearly had implications on expenditure assigned to back-end and test & measurement equipment. Not only there is production overcapacity in a number of market segments, there are also viable suppliers of second hand equipment. (Courtesy Enabling MNT)

Purchase of capital equipment has a profound influence on any organization in terms of finance as well as on product quality and time to market.

Used equipment, either refurbished or not, can be an interesting alternative to buying new equipment. In general, the purchasing process can be much shorter and the price much lower. There are drawbacks, however, particularly if the equipment is purchased “as is”: The transfer of such equipment into production can introduce problems in term of time and manpower. In addition, used equipment is not always state of the art, leading to production with yesterday’s processes. The consequences of pursuing this solution should therefore be carefully considered.

Initially the larger semiconductor oriented companies neglected this area. Only recently, two of the largest suppliers entered the market: ASML introduced a backside align option on their steppers in 2002 and in 2003, TEL (Tokyo Electron Ltd.) released a new wafer prober for research and development applications specifically designed for MEMS products. It should be noted that both machines were designed with a view to target other market segments too. The subsequent entering of companies into this market is shown in Figure 3.

In times of economic downturn, semiconductor suppliers turn to niche markets such as those offered / enabled by MST/MEMS. In such markets suppliers can often revive older product lines, adapted to specific demands from this industry. In addition, several companies began to use their MST/MEMS process experience in order to produce dedicated equipment for this market, thus, resulting in the situation where equipment for MST/MEMS production is now readily available on a commercial basis.

One interesting way for a big company to enter this market without risking their ongoing activities is to buy start-up companies with specialized knowledge and presence in that new market. Veeco followed this route and has become, undoubtedly, the market leader for Scanning Probe Microscopes.

Generally, it is not easy for small companies to organize a global or even pan regional presence or to have an adequate maintenance and repair support. Larger customers expect their suppliers to be able to offer such maintenance support and to minimize the number of suppliers. One possible solution is to co-operate with local companies, which offer sales and "after sales" services in a certain area for a few of the (small) specialist companies. An interesting variant on this route is the setting up of collaborations, such as, for example, Exitech, Primaxx and Xatix with STS. Such collaborations benefit from the global presence of STS who are, in turn, able to broaden the service to their customers. STS shows another interesting example of specialization and co-operation. The Japanese market for DRIE is served by a local sister company SPP. They offer DRIE equipment based on the STS technology fabricated with Japanese components.

Another example of sharing forces is companies specialized in offering sales and support for number of MST/MEMS equipment companies in a certain area. MEMS 4U2 (led by Ed Voorneman) is a good example of that. MEMS 4U2 support among others AML and Adixen (ex Alcatel) in the German region.

3 Front End Equipment

We present in the following list, the key MST/MEMS Front End processing technologies:

- deep reactive ion etching for silicon
- LPCVD low stress silicon nitride
- front/backside alignment
- release etching and super critical cleaning
- waferbonding

3.1 Deep Reactive Ion Etching

Fabricating three dimensional and precisely micromachined silicon structures are an enabling process for many MST/MEMS suppliers who manufacture products such as: pressure sensors, accelerometers and gyroscopes. DRIE is a process optimized to achieve that goal, several suppliers bring equipment to the market from small scale manual equipment to high throughput automatic equipment (see figure 4).

Figure 4: STS automatic DRIE equipment(Courtesy STS)

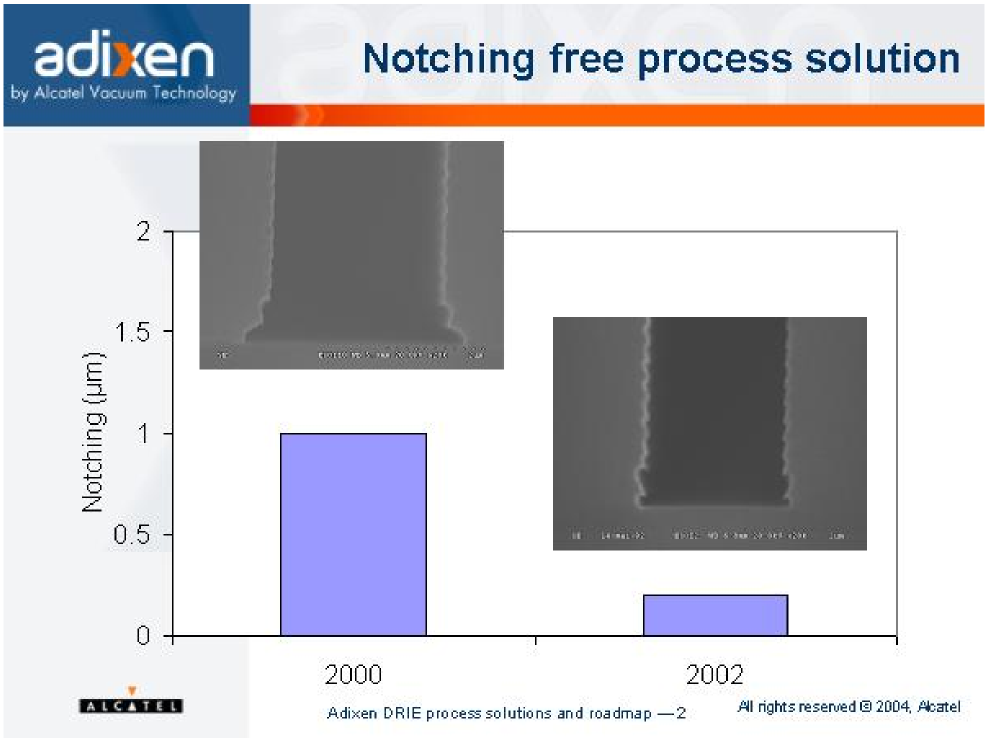
Historically, there are three major problems associated with DRIE, namely:

1. Cost price of the products is directly linked to equipment utilization and therefore with etch rates.

2. Aspect ratios are related to the minimal feature sizes achievable and the precision of the achieved structures.

3. Smoothness of sidewalls is, generally, a challenge.

The equipment industry as a whole has been working hard to improve the equipment to meet standards for telecom and other industries. Part of the result of that progress is given in the following figures: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Notching free process solution

Adixen DRIE process solutions and roadmap —2

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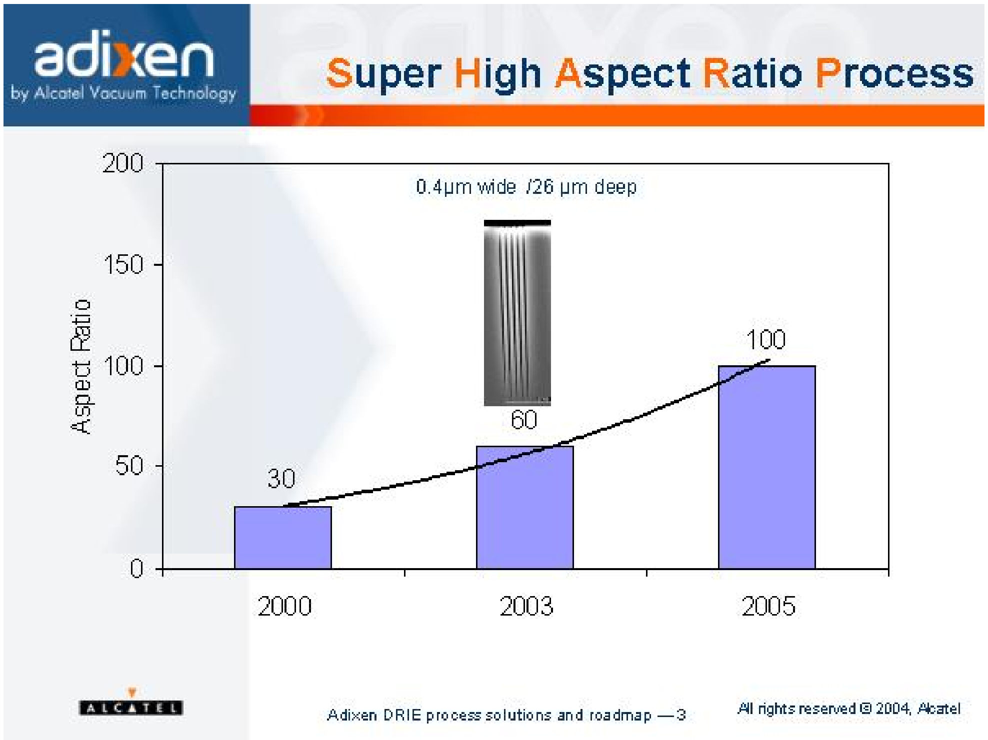
Figure 5: Evolution of minimizing notching effect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Super High Aspect Ratio Process

Adixen DRIE process solutions and roadmap —3

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Figure 6: Aspect ratio evolution

Aspects ratios are important in semiconductor industry (trench isolation), for the creation of typical MEMS products like gyros and accelerometers, and, of lately, for the creation of very small vias in wafer through connection for advance package concepts.

The etch speed is very important as it is directly related to the Cost of Ownership (CoO). This is even more important in the MST/MEMS case, where the etch depths are often much higher compared to other thin film products (hundreds of micrometers versus hundreds of nanometers). The challenge is, therefore, to increase the etch speed without excessive heating of the substrate and without losing on dimensional accuracy. In addition to the chemistry, the process is also influenced by the amount of energy in the plasma. In conventional RIE, the plasma density is limited by the method of coupling RF energy into the plasma. This problem becomes particularly acute at reduced pressure, often required to keep other process aspects under control (anisotropy and micro-loading). The in-coupling of plasma can be increased by using Inductive Coupled Plasma (ICP). Conventional RIE plasma sources typically achieve a plasma density in the 0.5 - 5.0 x 1010 cm^{-3} range. ICP operates in the 1011 to 1012 cm^{-3} area.

Inductively coupled plasma sources are said to have the following advantages over other high density sources, such as ECR (electron cyclotron resonance):

- simplicity of design
- less stringent requirements on operating pressures
- no requirement for a magnetic field.

While the etch depths are very high and the product demands are very strict with regard to the aspects ratios, process conditions to minimize side wall etching are needed. During the Cryo process, the substrate is cooled down to temperatures as low as –100 ^{o}C to –150 ^{o}C. At those low temperatures, SiO_xF_y is formed on the sidewall, preventing side way etching. For this reason, maintaining substrate temperature is critical. In this process, an electrostatic chuck is used to hold the wafer securely to the chuck by electrostatic forces, while flowing a small quantity of helium over the backside of the wafer.

To achieve high aspect ratios without heating the substrate, the Bosch process can be used. In this process, the etch process is carried out in small steps, each followed by a cleaning step. During the etch process a polymer is formed on the sidewalls, preventing side way etching. This polymer is subsequently removed during cleaning steps. The overall process is an alternation between etching and cleaning leading to a slightly waved side wall structure (scalloping).

There is always a trade off between etch rate on one side and scalloping and mask undercut on the other side. The Bosch process tend to have higher etch rates, the Cryo process on wall smoothness and pattern accuracy, but all major suppliers have intensive programs running on performance improvements.

The above processes are well developed by some suppliers, resulting in equipment/supplier specific processes, such as the Alcatel ARCE process aiming at precisely controlled etch depth, independent of layout variations and the STS ASE process aiming at very high etch rates.

	Bosch	Cryo
Resist selectivity		Slightly better selectivity, but higher temperature baking is needed
Critical hardware	Fast switching between the cleaning and deposition requiring the use of high quality mass flow controllers etc.	Good contact between chuck and wafer is required, presenting potential sensitivity to contamination, damaging and warpage of the wafer
Sidewall	Scalloping effect	smooth
Sidewall protection	Polymers to be cleaned regularly	SiO_xF_y formation
Main application area	General	Optical waveguides

Table 2: Comparison Between the Bosch and the Cryo Processes

3.2 Front/Backside Alignment

Usually only one side of an MST/MEMS substrate is processed. For many MST/MEMS devices, however, double sided processing is becoming increasingly common. For such cases functional layers on both sides of a wafer will need to be aligned with each other. This is generally achieved by simultaneously observing markers on the back of the wafer and markers on the mask positioned above the wafer. An alternative option is to view through the wafers using infrared (IR) light. This, however, is not as accurate a method and becomes more difficult with increasing wafer thickness and, usually, it is not used with wafers larger then 4'.

The company Suss was the first on the market with double side aligners and has installed over 2000 machines worldwide. Other companies followed, initially only with contact and proximity aligners, but since the late 1990s also with steppers. For the manufacturers of steppers, the alignment accuracy in the MST/MEMS markets is not thought to be very demanding, but adapting their equipment to the flexibility (substrate thickness and resist types) needed for this area is a challenge. In general the steppers have as an advantage the ability to reach very high accuracy and are, therefore, more suitable for high volume production. Their disadvantage lies in their relative inflexibility with regards to the thickness of substrates and resists. It must be noted that most of the stepper suppliers (Nikon, ASML, Ultratech etc.) now offer equipment with higher depth of focus than used in IC manufacturing. This is needed for MST/MEMS while the stepheights are rather large compared to mainstream semiconductors.

Contact aligners can introduce defects into the wafer which negatively affect the product yield due to the physical contact between mask and product. The use of steppers eliminates this problem as well as the high cost for mask-cleaning but the high investment required can be a barrier.

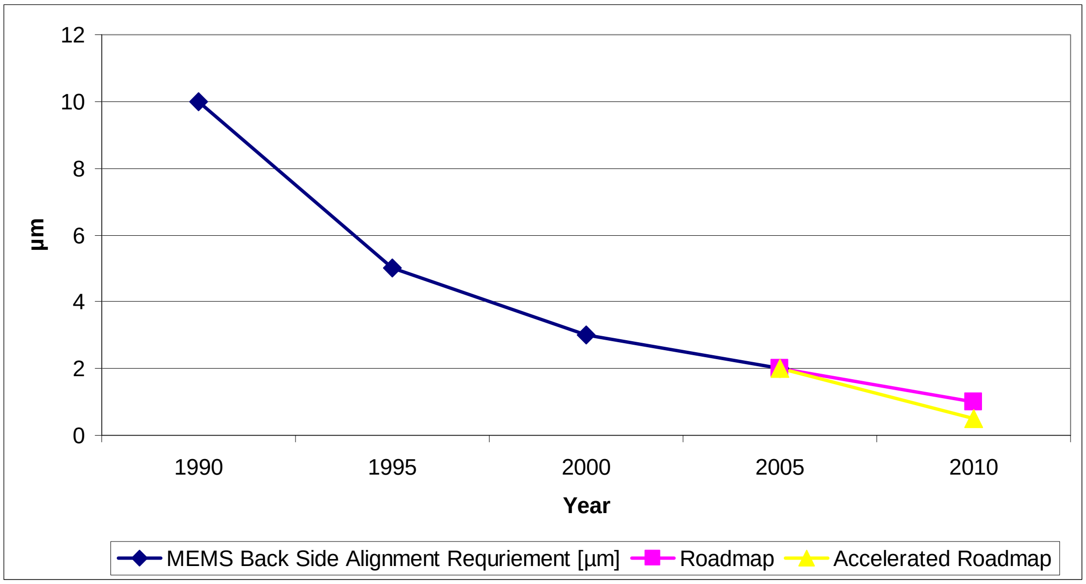

Figure 7: Backside alignment requirements (courtesy EVG)

As shown by figure 7, demand on equipment specifications are increasingly becoming more stringent, although it should be noted that semiconductors is often more driving this development then MST/MEMS, making it once again possible for MST/MEMS to piggyback on the IC industry.

3.3 Release Etching and Super Critical Cleaning

In MST/MEMS, often free-hanging small structures are created. This requirement necessitates a process to release those structures by removing the underlying layer (sacrificial layer). It is easy to imagine how critical such a fabrication process step is with typical structures having lateral dimensions in the order of tens to hundreds of microns and thickness of only a few microns which are free hanging at a distance of a few microns from the substrate.

There are two options for the release etch of the sacrificial layer: dry or wet chemical etching.

Dry etching of sacrificial layers can be a slow process, requiring a long time and using expensive equipment. This is especially the case when the equipment being used is designed for “normal” thin film processing, including for example barrel etchers. Such processes etch, at best, a few microns per minute which is not much compared to the large lateral dimensions required to be etched. To facilitate the etching process, sometimes the beam is perforated by a dense structure of holes. This may have a negative effect on the electrical performance and mechanical strength of the final product/device.

Wet etching is a more economically attractive process, insensitive to over etching and low temperature. It typically consists of three steps: removal of the sacrificial-layer material using liquid chemicals, rinsing, and the removal of the rinsing liquid (drying).

There is a disadvantage, however, where during the drying step of the product, the beam can be deflected causing stiction or similar damage. To overcome this problem, drying with supercritical fluids (mostly CO2) can be used.

3.4 Wafer bonding

Wafer bonding has received a considerable amount of attention lately while it enables a range of new products ranging from SOI wafers to fluidic devices. The processing is in a separate, vacuum chamber (see figure 8).

Figure 8: EVG automatic bonding machine (Courtesy EVG)

Wafer bonding techniques can be divided between processes where no additional material is added (direct, anodic and fusion bonding) and processes where an additional layer separates the wafers and form the bonding layer (organic, glass or metal). This layer is made of soft deformable or low temperature melting materials.

In general heat is required to create the bond. In nearly all cases the whole wafer is heated up to the bonding temperature. Generally, laser and microwave heating are often proposed to achieve localized heating area, particularly, when sensitive devices on the wafer have to be protected.

Several waferbonding techniques have been proposed. This graph (Figure 9) provides a good summary of the current techniques.

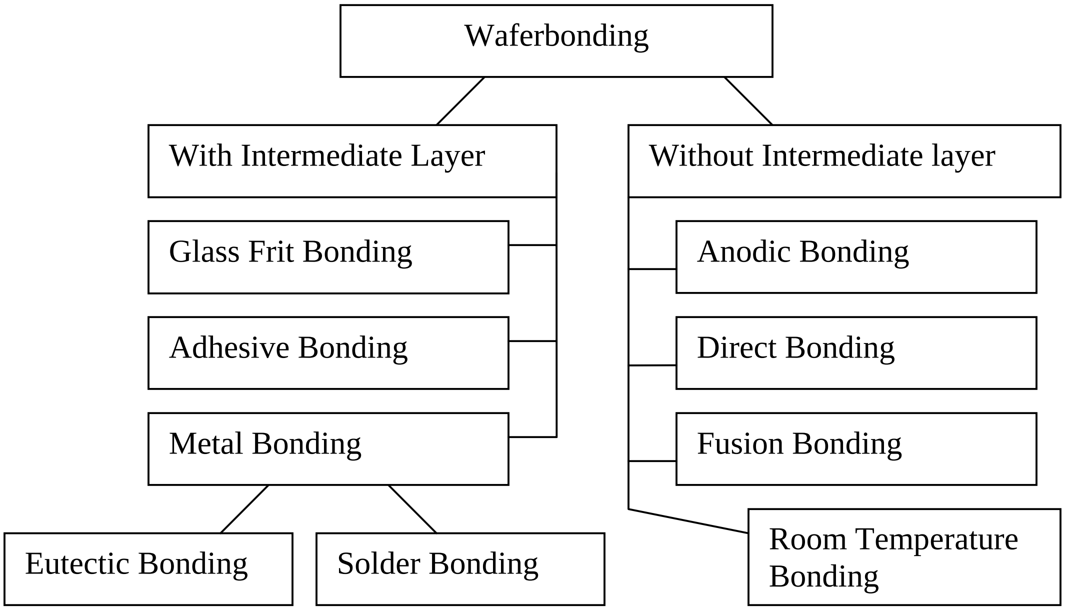

Figure 9: Overview of bonding techniques

3.4.1 Bonding Processes Without Intermediate Layers

Technologies such as anodic, direct and fusion bonding rely on the fact that smooth and flat surfaces are attracted to each other at room temperature. This initial bonding step is not very strong, although it can be a little enhanced by initial surface treatment with special chemicals or a plasma process. Bond strengths can be enhanced by applying a voltage (causing an initial pressing of the wafers together and thereafter diffusion of ions to make the surface active) and temperature. The low temperature adhesion is based on van der Waals forces (hydrogen bonds). Higher temperature bonds are based on chemical binding (see also figure 10).

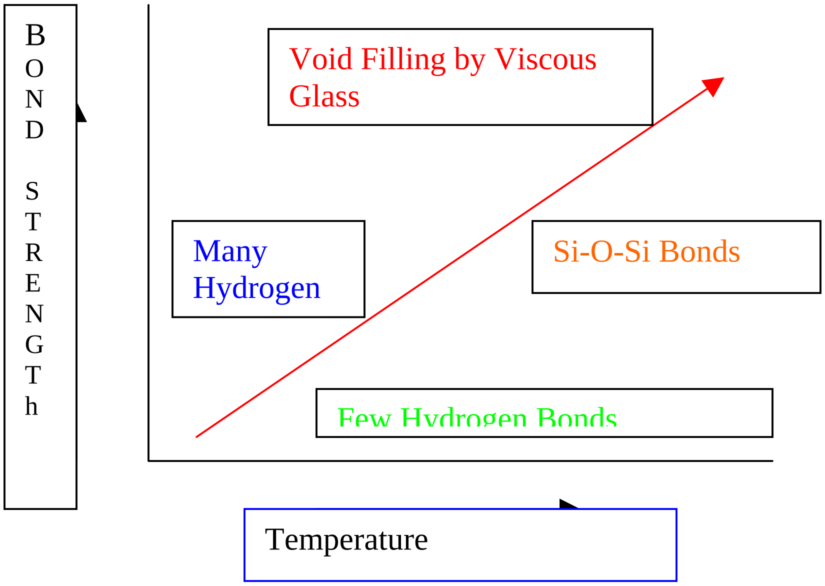

Figure 10: bonding technologies and bond strengths

This process is described in greater detail below for silicon to silicon bonding and silicon to silicon dioxide bonding. Direct and fusion bonding: Immediately before bonding, the surfaces are wet chemically etched by HF or plasma cleaned. This leaves the two surfaces slightly hydrophilic and covered by OH groups. The OH groups can form hydrogen bonds with each other, when the two surfaces are brought into close contact. As the temperature is increased, more and more OH groups are connected. At a more elevated temperature, water will leave the interface and strong Si-O-Si groups are formed. At even higher temperatures, the oxide layer will become viscous and micro-voids will be sealed off (see also Figure 7). Annealing at 200 – 400 ^oC in atmosphere is needed to create a bond with sufficient strength to withstand dicing. Without the high temperature anneal step, this process is referred to as direct bonding. When annealed at about 700 – 1000 ^oC, it is referred to as fusion bonding. With bonding at this high temperature, the intrinsic strength of bulk silicon is reached. For guaranteeing a high quality of direct bonding, the condition of the surfaces to be bonded is critical. Ziptronics offers a high quality bonding process for licensing. Their special surface treatment makes the surfaces of the wafers suitable for direct room temperature bonding. Silicon Genesis also offers their plasma-activated bonding technology for a license. This technology has a proven track record for SOI wafers, but can also be used for other applications. Both processes are limited to very flat and smooth wafers.

Anodic bonding makes use of the voltage-driven diffusion of sodium ions to achieve chemical bonding at lower temperatures. It is used to bond silicon and glass wafers. Again, the wafers are pre cleaned. The silicon and glass wafers are heated to between 300-500 ^oC (process temperature depends on the type of glass). At this temperature the alkali-metal ions in the glass become mobile. The wafers are brought into contact and a high voltage is applied across them. This causes the alkali cations to be driven from the interface. This results in a depletion layer and a high electric field strength between the two surfaces. The resulting electrostatic attraction brings the silicon and glass into intimate contact. Further current flow of the oxygen anions from the glass to the silicon causes an anodic reaction at the interface. The result is that the glass becomes bonded to the silicon with a permanent chemical bond. This technology is not restricted to glass– to- silicon bonding. Glasses with sufficient high alkali ions, can also be bonded to metal, ceramic or III-V substrates.

3.4.2 Bonding Processes With Intermediate Layers:

Glass frit bonding: The electronic industry has been using low melting point glasses for many years to form hermetic seals. This process is typically carried out in the temperature range 400 – 650 ^{o}C. Additional pressure is often used to ensure good uniform contact. The thermal expansion coefficient of the glass is normally chosen to be between the two values for the wafers being bonded.

Glass layers can be deposited with different methods: preform, spin-on, screen print, sputtered film, etc and patterned to define sealing areas. Although a wide range of glasses are commercially available, publicly available information relating to the choice of suitable materials and process conditions to be used for waferbonding is limited. This is especially a problem while the process window is small. If the temperature of the process step at which the organic binder is removed from the glass layer is too high or the process time too long, the wetting behavior is decreased and low strength bond results.

If the temperature is too low or the time too short, too much binding material is left in the layer, resulting in low life times of the device. The resulting process is very much equipment/operator/product dependent, making it difficult to control the process, resulting in variable quality and yield problems. Another disadvantage is the size of real estate needed for the glass. In general glass frit bonded wafers can host less devices on a wafer compared to direct, fusion or anodic bonding.

Adhesive bonding: Many organic layers (epoxies, silicones, photoresists, polyimides, etc) have been proposed as intermediate layers for wafer bonding. The large number of technologies available to apply the organic layers (spinning, spraying, screen printing etc.) is an advantage. As the resulting bonds are in general rather weak and prone to out-gassing, this technology is not often used for the permanent bonding of wafers.

Eutectic bonding: The eutectic temperature of a two-component system corresponds to the lowest melting point composition of the two components. This property can be used to form a bond between two wafers. The different components of the eutectic layer are deposited on the two wafers. When brought into contact and heated, diffusion ensures alloy forming at the surface. The eutectic has a lower melting point compared to the ingredients. The melted layer is therefore restricted to a thin, in-between, layer. The Au-Si system is often used for this as it melts at about 363 oC (97.1 Wt % Au : 2.85 Wt % Si.).

Solder bonding is a relatively low temperature (150 - 350 C) process. As the bonding material is a good conductor, mechanical bonding, sealing and electrical interconnection can be performed in one step. When a special gas filling is needed, a small hole can be left open during soldering. This venting hole is sealed off after gas filling. Compared to glass frit bonding, much smaller feature sizes (>20 micron) are possible. The metal structure can be a disadvantage in high frequency applications.

To use additional layers to separate the wafers and bond them has some advantages:

- With this layer a cavity can be formed
- This technology is more forgiving to surface irregularities

- The layer can help to release stress and accommodate different expansion coefficients

The disadvantages are:

- Less strong bonding
- Extra and complex processing steps

A global overview of the wafer bonding technologies' advantages and disadvantages is given in Table 16.

	Temp. (^{o}C)	Outgassing during life time	Creation of cavity between the wafers	Loss of real estate	Strength of bond	Remarks
Anodic	300 - 500	Oxygen release during bonding	No	Limited	Very good	Flat surface and high voltage needed
Silicon direct	> 700	No	Yes	Limited	Very good	
Glass frit	400 - 650	No	Yes	Considerable	Medium	Small process window
Adhesive	< 200	Yes	Yes	Medium	Medium	
Eutectic	370 – 400	No	Yes	Medium	Medium	
Solder	250 - 350	No	Yes	Medium	Medium	
Direct	< 100	No	No	Limited	?	Very flat surface and special surface treatment needed

Table 4: Advantages And Disadvantages Of Different Waferbonding Technologies

3.4.3 Trends in Wafer Bonding

At this moment direct bonding seems to become the leading technology due to the surprising fast lowering of the minimal needed bonding temperature (see figure 11), opening up many new market segments.

More completed technologies like glass frit and adhesive bonding lose market share. Anodic bonding is keeping its market share, partly suppliers like AML managed to speed up cycle time and minimizing the cost per bond. (See figures 12 and 13)

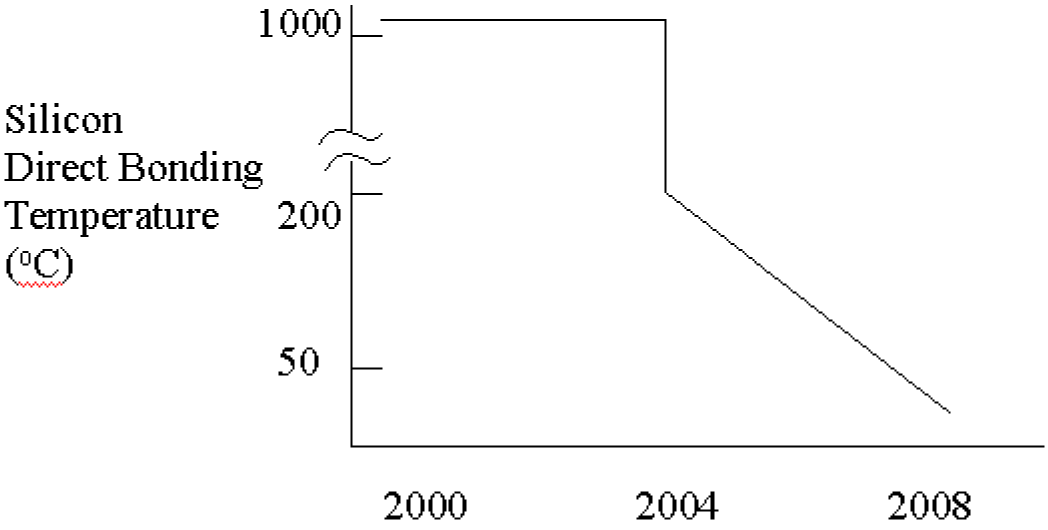

Figure 11: Lowering of minimal needed bonding temperature over time (courtesy AML)

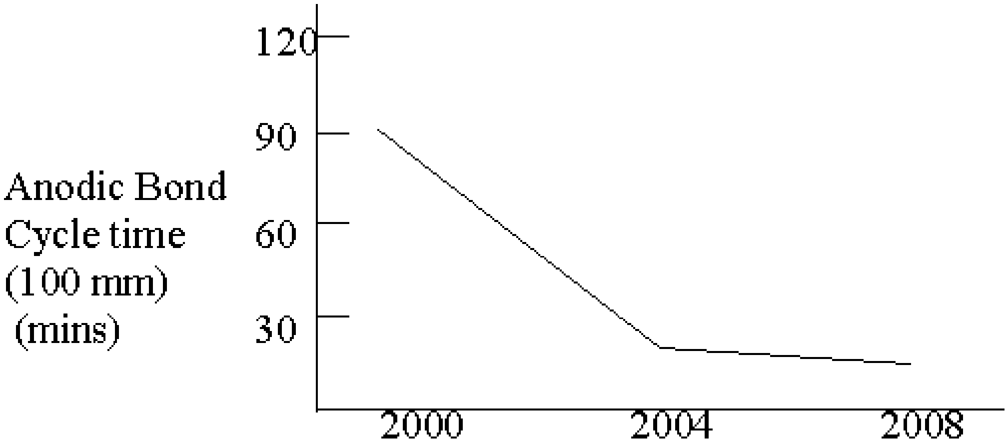

Figure 12: Anodic bond cycle time improvement (courtesy AML)

The improvement of cycle time in anodic bonding is largely the result of equipment improvements speeding up temperature ramp up and cool down, and increasing the maximum voltage/currents used.

All these improvements resulted in a decrease of cost per bond at the end of the last century to less the 50 Euro and it is expected that this could further decrease to perhaps 15 Euro, making this process a feasible option for use in the production of high volume consumer products.

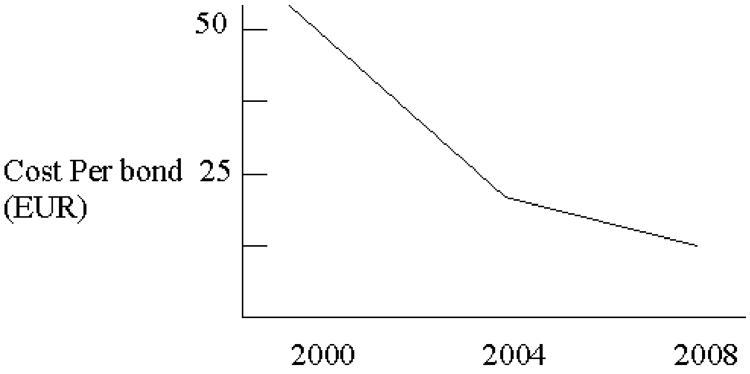

Figure 43: Decrease of cost per bond over time (courtesy AML)

4 Backside Equipment

MST/MEMS is an industry undergoing a rapid development process, using many new concepts and processes. At first sight the diversity is overwhelming and trends are difficult to see. There is, none the less, one trend that is clearly visible: the tendency to maximize the use of standard and commercially available high volume (electronic) processing, even if this means that the design has to be changed or additional steps must be introduced. Examples of such processes are: waferthining and microvia creation. In this context, the MST/MEMS market is able to follow the semiconductor roadmap aiming at less interconnection lengths and smaller package dimensions. This trend is inadvertently leading to the reliance on thinner wafers and 3D packaging, both requiring processes such as wafers thinning, microvia creation and new technologies for die separation. In a rising number of applications lasers are used. The advantages of flexibility and localized action compensate for the disadvantages of the “non multiple” and often slow processing.

Other industry segments have also had an influence on this market segment. Micro assembly equipment and equipment to assemble optical components are often very similar. Nanotechnology, too, is having a strong influence on the market with the growing availability of technology and equipment for micro positioning and manipulation.

5 Wafer Thinning

Wafer thinning is required for several applications such as advanced semiconductor packaging, smart cards, production of SOI wafers and also for MST/MEMS. As an example, bonded wafers must be thinned to fit within standard packages. Continuous improvement of processes and equipment has resulted in achieving thicknesses as low as 50 µm in production.

This is a typical example where semiconductors and MST/MEMS are pursuing the same goals and using the same or nearly the same technologies (see Figure 14).

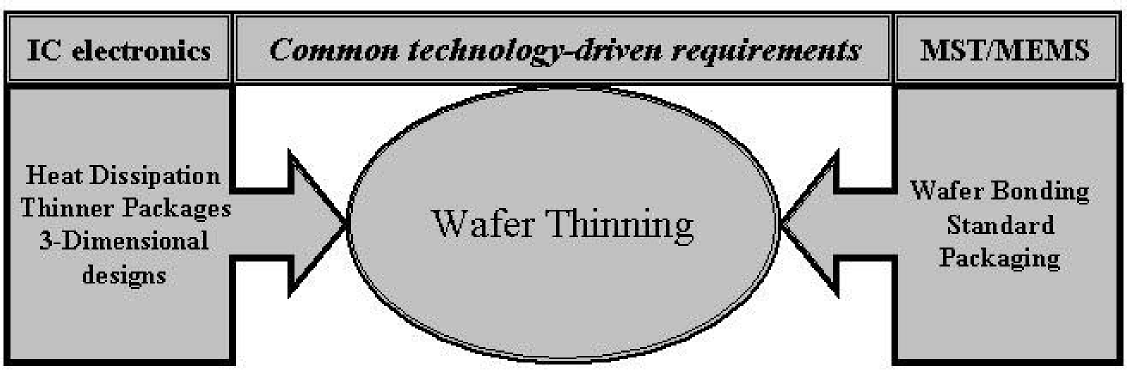

Figure 14: Technology drivers for wafer thinning in MST/MEMS and semiconductors (courtesy enablingMNT)

An additional benefit of thinning the wafer is to assist in wafer etching and die separation processes where the vias or dicing lines can be formed before thinning. The thinning process continues till the bottom of the vias/dicing lines are exposed, circumventing the dicing process and/or giving access to the electrical interconnection lines on the front of the wafer.

Wafer thinning usually entails the following steps:

- Tape lamination to protect the wafer against frontside damage and breakage
- Backgrinding or polishing to remove bulk silicon
- Tape se-lamination
- Final polish to remove the damaged layer, this can be achieved through:
    - Wet etching
    - Plasma etching
    - Dry polish
    - Chemical Mechanical Polishing
- Cleaning

Back grinding is the usual method for thinning silicon wafers in the semiconductors industry. The wafers are grounded using diamond abrasive grinding wheels on rotary grinders. On the wheels diamond abrasives are embedded in binders. Grinding is a fast, well known and economically attractive process step. It does, however, require additional treatment to remove stressed layers and create a smooth surface.

The limit for grinding is around 250um. Yield issues during the grinding and the downstream processes make it difficult to go below 150 um. Stresses can lead to increased wafer breakage and crystalline damage can extend to the active device regions and negatively influencing circuit performance.

In addition, grinding introduces a stressed layer, which has to be removed before further processing. The following processes can be used to remove that layer:

Polishing: the wafer is mounted onto a plate, which is brought into contact with abrasive slurry. The slurry is a combination of lapping liquid and hard particles such as silicon carbide or aluminum oxide. This has the disadvantage of high down force requirements, which may damage very thin wafers and "drive" the sub-surface damage further into the surface.

Wet etching: A process often used to remove backside grinding damage and stress. The spin-etching process provides for uniform removal, but the edges of the thin wafers are made sharper and more fragile.

Chemical Mechanical Polishing (a combination of wet etching and polishing) is not regarded as a very economical process. CMP has also the disadvantage of high down force requirements, which may damage very thin wafers and "drive" the sub-surface damage further into the surface.

Plasma etching. the equipment is rather expensive, making economic processing difficult, although etching rates as high as 25 µm/hr are reported.

Tru Si offers the alternative of atmospheric plasma etching. Their system clamps wafers in a special downward facing platen by employing a Bernoulli-based, differential pressure effect. The etcher utilizes a precise, magnetically controlled, high density, inert gas, and dc arc-plasma discharge. At a temperature of 10,000 K, the plasma decomposes 100% of all reactants and, at ambient pressure; charged species quickly recombine downstream from the plasma thereby eliminating their potential for causing ion damage. High energy, activated species are created in the plasma region, but at atmospheric pressure the plasma is thermal due to the small mean free path (<1 µm) of the plasma species. The kinetic energy of the ions, electrons and neutrals is about equal and very low

(< 1 eV). Particles in the chemical reaction zone surrounding the source thus also have low kinetic energy. These characteristics, combined with the low floating potential of the wafers in the process chamber prevent high-energy electron-ion bombardment and electrostatic charging of dielectric surfaces.

After removing the stress release layer by the processes described above, the wafers must be handled by special tooling. Standard vacuum tooling can no longer be used, while the wafer is prone to warping, thereby preventing vacuum contact and making insertion in standard slot difficult or impossible. Larger contact areas for pick up chucks and the Bernoulli effect to position the wafers is therefore used. In addition to the bow and warp problems, thin wafers are very fragile. Automated handling equipment can easily damage the wafers if handled too roughly.

It should be noted that although plasma thinning of silicon wafers is a fairly common process, thinning of GaAs or SiC wafers is less straight forward and more time consuming (25 µm/min compared to 3-5 µm/min).

Prices for thinning wafers are dependent on specification and wafer size. For, more or less standard thinning, \$3 - 4 for small wafers and up to \$8 – 15 for 200/300 mm wafers are usual when subcontracting in volume.

5.1 Die Separation

For many process steps MST/MEMS manufacturing can use the same - or nearly the same - technology as used for semiconductor fabrication. When applied to dicing, however, this is seldom the case. During dicing, the blade, (with diamond in a binder) crushes the substrate material and in order to cool the dice and remove the debris, a water jet is aimed at the dice blade. Damage due to substrate particles and cooling water reflected by the blade is a high risk for the sensitive MST/MEMS structures. Special precautions must be taken for protecting the devices, for instance by capping the devices before dicing, by waferbonding or by applying a coating over the die. When these solutions are not applicable, other separating technologies must be found.

It should be noted that the semiconductor industry is also looking into alternative separating technologies. One of the reasons is the increasing use of thinner wafers, making traditional dicing less suitable.

5.1.1 Alternatives to Mechanical Dicing

Dicing processes with very low or no water flow are sometimes used, but the equipment utilization is low. Breaking the wafer can be a clean alternative, but to let the substrate break at the right places a “starting” structure/point must be created. This can be achieved by dicing or laser-machining a small scribe line (a few micron will be sufficient). Hereafter, a force is applied to the bottom of the wafer and the wafer breaks along the scribe lines, cleanly separating the dies.

When the dies become very small (such as for passive components including diodes), the area for the dicing lines occupies a substantial part of the real estate and laser cutting is used as an alternative. For MNT products, on the other hand, contamination due to particle generation caused by the laser beam and substrate interaction is also a risk. Also temperature effects can cause problems, although pulsed lasers are more economical in that sense.

For standard wafers, laser dicing has been long seen as an uneconomical process while it is slow, but as wafers become thinner, as is the trend in semiconductors, laser dicing is gradually becoming a feasible option.

Wafer jet cutting (with a narrow high velocity water stream, with or without abrasive particles added), or air jet cutting are seldom used in MST/MEMS as these processes are prone to creating severe contamination. These have the advantage of less thermal damage and smoother edges without micro- cracks or chipping.

To use laser cutting in combination with a waterjet (referred to as microjet cutting) is a fairly new idea, which is claimed to produce better defined cuts when compared to standard laser cutting.

The different options and their main characteristics are summarized in Table 3.

5.2 Laser Micromachining

Machining materials with lasers, was first introduced in the early 1970's, and is now a process that is fairly commonly used in many industry sectors. As an example, the use of lasers in processing microelectronic devices, such as the trimming of thick and thin film resistors is so well established that the laser has become a common tool for that industry. This is especially true for high-volume, high-accuracy trimming applications.

	Water jet cutting	**Laser cutting**	**Microjet cutting**	**Mechanical dicing**	**Breaking after scribing**
Energy medium	Water	Light	Light	Abrasive material	Force on bottom wafer
3D cutting	Very limited	Limited	Possible if absorption is sufficient	Not possible	Not possible
Materials that can be cut	All materials	All metals except highly reflective metal	All metals except highly reflective metal	No soft or brittle materials	No soft or brittle materials
Material combinations	Possible without exception	Materials with different melting points can cause problems	Possible if absorption is sufficient	Complicated with sandwiched materials	Can cause problems
Max. material thickness for economical mnt processing	Up to 50 mm	Up to10 mm	Up to 3 mm	Up to 5 mm	Up to 1 mm
Major applications	Cutting of ceramics etc.	Cutting of sheets, i.e. metal		Semiconductors, magnetic heads	
Processing accuracy	~. 0.1 mm	~ 0.05 mm	< 0.01 mm	~ 0.1 mm	~. 0.1 mm
Thermal stress of material	None	High	Limited	Localised	None
Forces acting on material during processing	High	Limited	Limited	High	High
Main disadvantage for MST/MEMS	Damage by water	Damage by heat	Damage by water	Damage by water and particles	
Number of equipment and service suppliers	Limited	Many	Limited	Many	Limited

Table 6: Characteristics of Die Separation Processes

Using lasers for micromachining MNT products is a more recent development. Initially laser micromachining was based on the use of continuous wave or long-pulse lasers. A disadvantage of these lasers is the heat transferred from the laser beam to the work piece. Especially with the often delicate devices in MST/MEMS laser processing was not feasible.

In the early nineties it was discovered that the transfer of heat from the laser beam to the work piece could be minimized by using ultra-fast[1] laser pulses instead of standard long-pulse lasers. Ultra-fast pulses are so short that the energy they transfer to the material does not have time to leak away from the laser spot. The amount of energy liberated in a very small area is so high that the material is forced into a plasma. This plasma then expands and takes almost all the heat away with it. As a consequence, very little heat is left behind to damage the material. This limits the amount of heat dissipated and it keeps the size of the contact area small. Such lasers can therefore be utilized for high quality micromachining such as for:

- The creation of microvias
- Direct writing
- Structuring by laser ablation.

Laser ablation is a non-contact, non-thermal method developed for removing material using a mask. The result is effective, predictable material removal, with very little thermal loading of adjacent areas. A well-known example is the use of laser ablation techniques for making inkjet nozzles. Here hole-to-hole accuracies of 0.5 micron have been demonstrated.

One disadvantage of laser processing is its localised and serial processing functionality making equipment utilisation and thereby realisation of an economically

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[1] Ultrafast: a duration that is less that about 10 picoseconds

attractive processing activity difficult where it is easier to achieve such benefits through batch or waferscale processing.

It should be noted that in semiconductors, lasers have been in use for trimming devices, laser marking and repair of photo masks. Fairly new is the use of such techniques for localized annealing. The need for smaller structures imposes a requirement for less diffusion of implanted species. Even Rapid Thermal Processing (RTP) will keep the wafer at high temperatures for far too long. Lasers can anneal more locally and achieve steeper temperature gradients in time and distance. Another driving force for the use of lasers in semiconductors is the growing use of thinner wafers. Normal dicing tends to damage thin-sized wafers, leading to reduced fracture toughness. Laser dicing becomes feasible when the amount of material to be removed is much less compared to a normal sized wafer.

5.3 Microvia Fabrication

Microvias, as opposed to "through holes", with diameters below 250um (10 mil) are used to interconnect adjacent layers of printed circuit boards. In addition, microvias can also be used for the creation of other interfaces such as for fluidic access to MST/MEMS products. Given that the origin of most of the equipment lies in the traditional packaging and assembly industry, most machines are capable of handling many substrate formats. Directly linked to this industry segment are the companies capable of providing the electroplating service to fill up the vias with conductive material.

Fabricating vias using mechanical methods is a rather common kind of processing in the PCB industry.

The drive to higher densities and therefore smaller lengths of interconnects, increased the use of lasers in semiconductor back end processing. State of the art is now pushing for vias with 50 microns diameter and the drive is towards even smaller sizes without giving in on equipment throughput. There are now nearly 2000 piece of equipment installed for this kind of processing.

There is also a trend in the semiconductor industry to migrate towards to 3D packages. The combination of several functionalities (amongst which MST/MEMS or nanotechnology is prime) within one package (see Figure 16) is another impetus. Both trends are, in essence, driving through-wafer interconnects. An aspect of microvias not to be forgotten is the need to deposit inside the via a conductive material. Most deposition processes, however, are operating on flat surfaces. The only process capable of covering near vertical walls is electroplating.

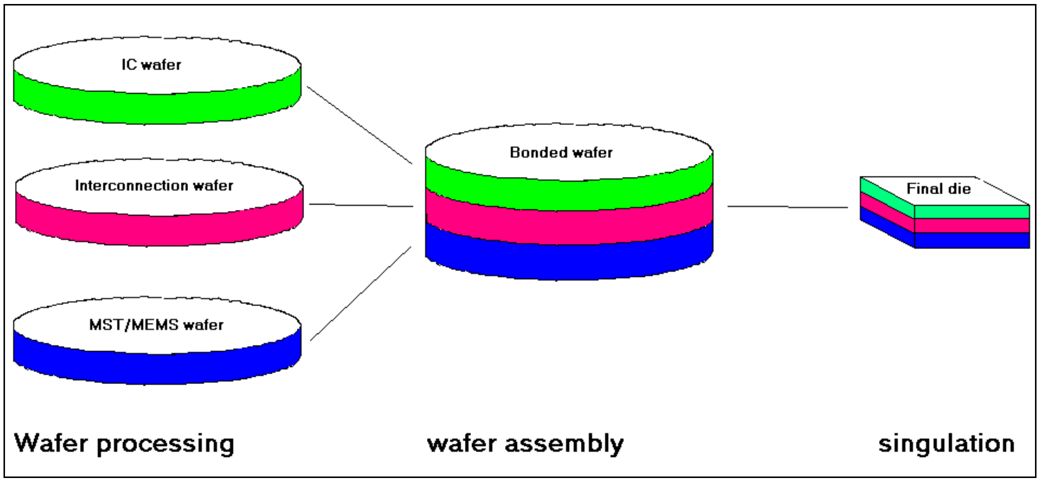

Figure 16: 3D wafer packaging (courtesy enablingMNT)

A special case specific to MST/MEMS is the need for through wafer interconnections within glass wafers. Lasers are not easy to use here, neither is DRIE.

Wet chemical etching or powder blasting are the preferred alternative technologies. An overview of the different technologies to create vias is given in Table 6.

	Remarks
Laser drilling	Large and increasing infrastructure
Mechanical drilling	Traditional PCB process, relative large holes
Wet etching	Real estate use a function of wafer thickness
Plasma etching	Real estate use a function of wafer thickness
DRIE	Expensive processing, but small hole sizes possible
Powder blasting	Niche technology, inexpensive, but real estate unfriendly

Table 8: Options for Microvia Creation

The cost for mechanical drilling of through wafer holes (over 150 µm diameter) in PCB is less then $1 for 1000 vias. This cost, however, is rising fast for smaller holes, and as a result laser drilling is becoming a more attractive option.

5.4 Microgripper

The fabrication and assembly of MNT (sub)systems necessitates the gentle and precise handling of all the constituent micro-components. Standard grippers and other handling tools are, generally, of limited use. Over the years, several companies and research organizations have developed “home-made” equipment for specialized handling. These developed into commercialized products, such as the microgrippers which consist of tiny jaws with appropriate clamping structures which allow the jaws to open wide and close gently. Clearly, excessive force can damage the fragile components. In addition, inaccurate movements of the jaws might miss the part entirely or place it incorrectly whilst non-parallel movement of the jaws can cause failure of lifting the object. Even if picking up and transporting a component to the right position is successful, the subsequent release of that particular part is not a trivial matter. Electrostatic or adhesion forces can in some cases prevent release.

Grippers are only one part of the handling issue. In other sections of this report, precise positioning and precision assembly equipment are addressed in greater detail.

Classification

Grippers are offered in many configurations, for many applications and made of many different materials depending on the purpose and intended application. The main distinction between commercial grippers lies, primarily, in the size of the object to be handled. The list shown in Table 8 provides a proposal for the classification of gripper equipment based on object sizes.

Type of grippers	**Size of objects to be handled**
Conventional grippers	Mm range
Low end microgrippers	Between 500 and 1000 µm
Mid range microgrippers	Between 100 and 500 µm
High end microgrippers	Between 1 and 100 µm
Submicron grippers	Below 1 µm
Nano grippers	(Macro) molecules

Table 10: Gripper Classification

Within the submicron and nano regime, grippers transgress into the domain of Scanning Probe Microscopes. Currently the principal utilization of high-quality microgrippers is in the research area. Mid range grippers are already in use in special assembly processes. Low-end grippers are becoming fairly common within the semiconductor industry.

The materials used to produce micro-grippers can also differ widely. Conventional and low end grippers are often made out of metal, offering good mechanical stability and wear resistance. For the high end grippers, silicon is a good alternative, offering the possibility of precise structuring.

5.5 Precision Position/Manipulation

The telecommunications industry in general, and optical telecommunications in particular, as well as nanotechnology, are the principle drivers for requirements in precision positioning. As an example, lasers and similar optical components demand accurate placement to minimize light loss. The entrance barriers to this equipment market segment are not high compared to the segments for front end and assembly equipment. In essence, it is relatively easy to create micromanipulation equipment. It is, however, more difficult to build reliable and reproducible equipment.

Alignment is, in general, enabled with active electronic control systems, which may provide either closed-loop or open-loop operation. For optical alignment, optical power is measured and maximized whilst alignment positioning is manipulated for maximum throughput/signal power. For open loop operation the sensitivity is determined by the sensitivity of the input signal and the associated amplifier noise. Creep and hysteresis can decrease the sensitivity. Open loop operation is only sufficient when alignment is being made, or when an external signal is being maximized (For instance during optical alignment the laser output power can be measured to find the optimal position). In microscopy applications, or in any application that demands repeatability or accurate measurement open loop systems are not sufficiently accurate. The performance is greatly improved when operating in a closed loop mode.

A control circuit compares the input signal to a signal from a position sensitive detector. The control circuit continuously adjusts the driver input to ensure that the input signal matches the position signal.

Piezo actuation is by far the most commonly used method for micro and nano positioning.

5.6 Precision Assembly

MST/MEMS components demand that the assembly equipment must be able to grip small (and often delicate) objects and place them with tolerance accuracies that reflect the features sizes of the constituent elements of the structure. (see figure 17)

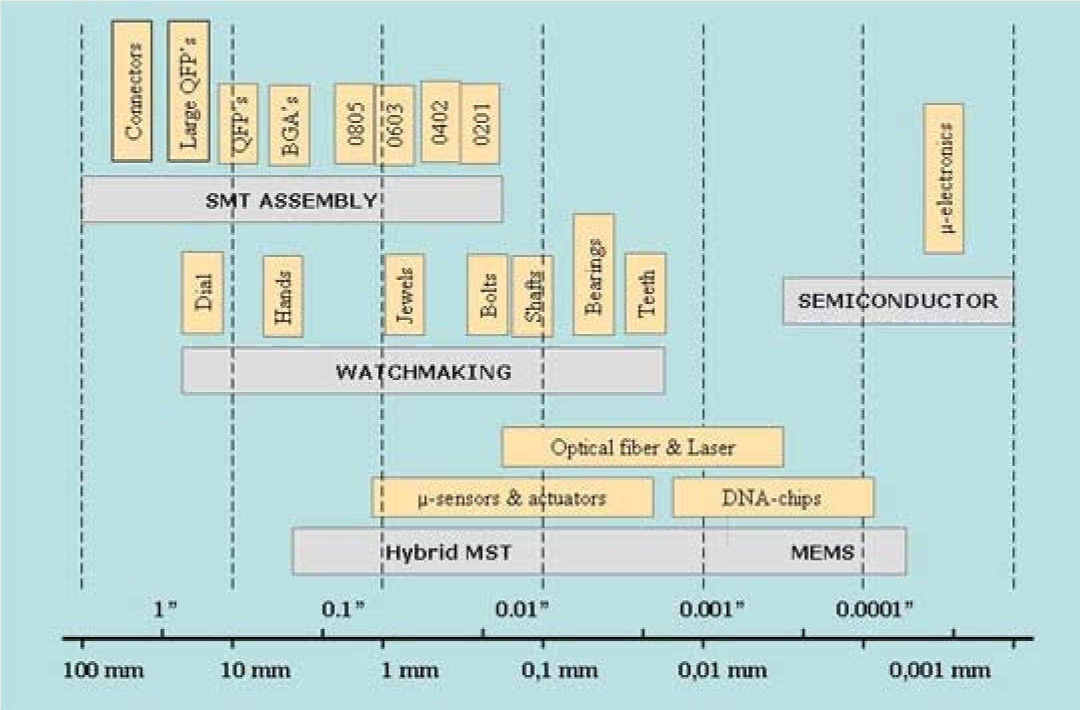

Figure 57: MST/MEMS microassembly compared to other market/technology areas(courtesyMA3soultions)

In addition, in order to achieve economic processing, either very fast or multiple processing is required. As an example from the semiconductor industry, which demonstrates this fact, currently available die bonders can place approximately 1000 units per hour.

Comparing the semiconductor industry characteristics with those for MNT, it is possible to establish that:

- In general placement of the products need only tolerances in the order of tens of microns, while electrical interconnections are very tolerant to alignment inaccuracies.
- The assembly of electrical components is in essence a 2D process, the object is nearly always placed on a flat surface.
- There is a high degree of standardization in this industry.

Whilst for MST/MEMS, the industry characteristics are:

- Placement accuracies in the region of microns and even below is usual
- Often 3D processing is required
- Application and often even customer specific products overshadow standards.

It is seen from this that the challenges for this industry lie in the need for more flexible micro assembly tools, capable of working in three dimensions and in a wide area of technologies and functional domains (see figure 18).

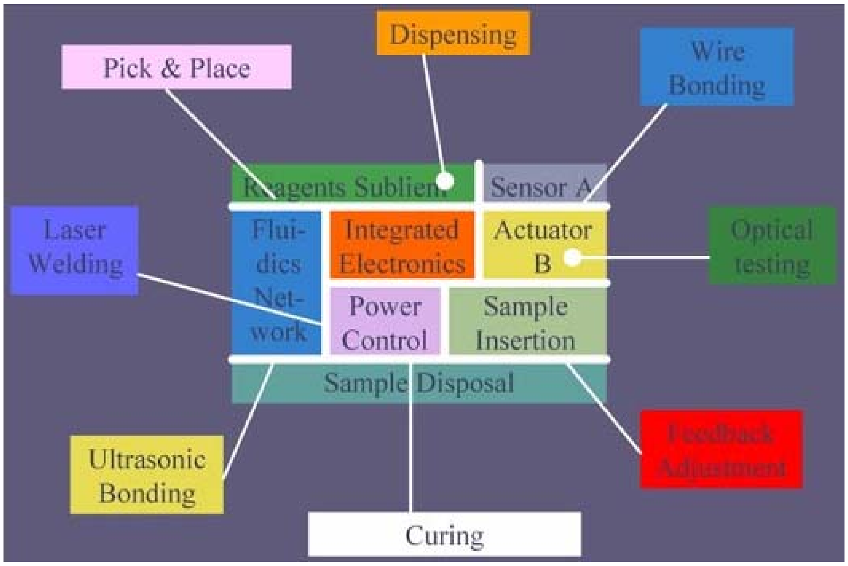

Figure 18: MST/MEMS microassembly is working in a wide area of technologies and functional domains (courtesy MA3Solutions)

Another challenge relates to the low production quantities required during the initial phases. This makes the purchase of dedicated equipment difficult to justify. To help the industry some equipment suppliers (Palomar, MA3solutions) offer assembly services in addition to the sale of equipment. Many other companies, traditional assembly suppliers, foundries and design & engineering companies are also offering services in this area.

Others use equipment from neighboring industry segments or home-built equipment. Examples of a closely related industrial equipment business are flip chip bonders and optical assembly equipment.

6 Nanotechnology

In order to investigate the market and distinguish trends, this study has classified nanotechnology production processes into the following four areas (see also figure 19):

Top down nanotechnology: top down nanotechnology utilizes processes and equipment used for high-end lithography and similar technologies, where large quantities of products are produced, mostly on flat substrates. In this area, the overlap with other equipment for MST/MEMS, semiconductor and data storage is significant. Main drivers for such developments include: nanotechnology product size, price of masks, cost of ownership of equipment and flexible production lines that allow for the cost effective production of small lot sizes. Main types of equipment in this group include: nanoimprinters, Atomic Layer Deposition tools (ALD) and Electron-beam aligners (E-beam).

Bottom up technologies: bottom up technology involves building up the nanotechnology products at the atom level by employing either mechanical manipulation or via molecules assembling other molecules. The former method uses Scanning Probe Microscope (SPM) based processes. Although SPM benefits from the widespread availability of SPM equipment, the processes are difficult to scale up. Molecular Self Assembly (MSA) is reported to be easier to scale up, however, to date this technology has only been demonstrated at laboratory scale.

Nanoparticle production: in nanoparticle production extended traditional physical and chemical methods are utilized to create small-sized particles, which exhibit special properties. Equipment for nanoparticle production either mechanically reduces the size of larger particles or introduces a chemical reaction that creates the desired material, followed by specific processes to keep the resultant particles small. Only a few companies offer such equipment. Most of the companies involved in nanoparticles production are also investigating suitable applications.

Nanotube production: nanotubes are considered to be the basis of very promising novel materials due to their unique properties. The technology (and the applications) is currently at a very early stage. The development of suitable equipment is becoming the differentiator between successful and not successful suppliers in this area.

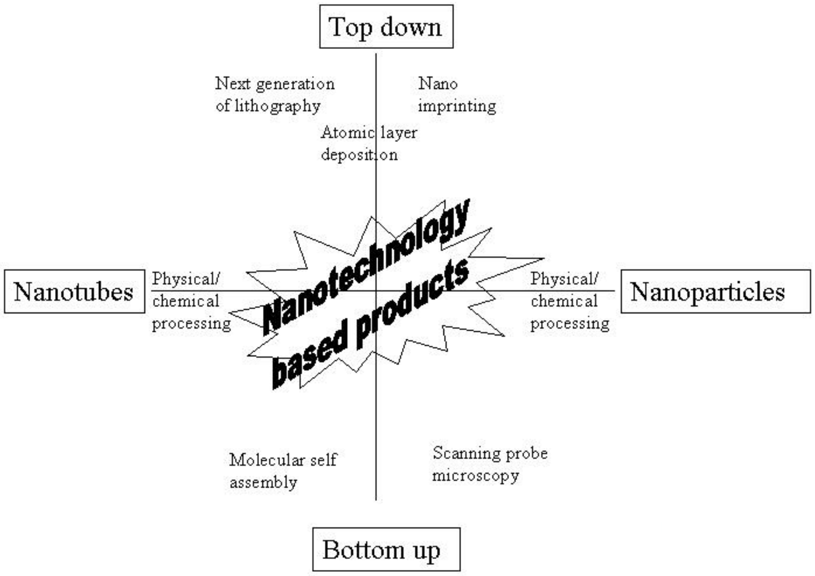

Figure 19: Nanotechnology production methods

It should be noted that the top down and bottom up approach (except for MSA) are mainly equipment oriented, whilst, MSA, nanoparticle and nanotube production are process oriented. Top and bottom nanotechnology equipment benefit from the available equipment infrastructure used extensively for semiconductor lithography and deposition and the ample availability of Scanning Probe Microscopes. The development of processes for the production of nanoparticles is mainly carried-out in-house, as there is limited equipment available on the market, although it benefits from experience derived from the chemical/physical process equipment market.

In general, both overlap and cross-fertilization can be seen. Nanoimprinting is seen by some as a potential contender for the next generation of lithography tools, which are now aiming at sub 100 nm feature sizes.

Given that nanotechnology equipment and equipment for high-end semiconductors are similar, a large number of companies offer modified semiconductor equipment (the so-called “top down” approach). Also several companies supply equipment based on chemical and physical processes for the production of small particles and nanotubes. The supply of equipment for the “bottom up” approach, which involves building nanotechnology products atom by atom, is very limited. Although there is an ample supply of Scanning Probe Microscopy based tools, it is not possible, however, to combine nanotechnology precision with industrial volume demand using such instruments. Processes for molecular self-assembly, potentially more suitable for economical mass production, are currently being developed but their commercialization is not expected in the near future.

The latest offshoot from the microtechnology revolution is that of nanotechnology. Promises of this technology even surpass that for more conventional MNT applications. In essence, nanotechnology already extends its influence into a large number of industrial segments, including semiconductors and consumer products, and also soon for data storage and sensors.

However, the supply chain for nanotechnology is not as yet very well developed, as processes with the following unique characteristics are required:

- A capability of producing well defined pure nanomaterials
- Processes which are environmentally safe
- Understood and well modelled processes
- Economically attractive.

The barriers to a breakthrough are substantial, including:

- Low yield of nanotube processing
- Expensive and slow top down equipment
- Modelling gab between fundamental quantum physics and micro level operation
- A lack of understanding of the fundamental device/material behaviour at this nanoscale.
- Finally, and most importantly, there is a need for accepted and proven applications.

Over 400 companies are currently claiming to be developing nanomaterials and are investigating applications using nanotechnology processes and materials. Already over 40 companies are offering equipment for this market.

The group of production equipment for nanotechnology can be divided in four subgroups: Top down, Bottom up, Nanoparticle processing and nanotube production.

6.1 Top Down

With 6 contenders in this field, the nanoimprinting market is well covered. The tools will have to compete with many alternatives. The ALD market, serving the semiconductor industry, will certainly be an area for experienced high volume suppliers. Initially, start ups may be established, however, the required investment is high, and historically only a small number of suppliers have survived in similar markets. There are, however, numerous opportunities in other areas, such as, biotechnology and sensors, where the demand for nanolayers is increasing.Probably the most promising area for dip

pen technology will be for the deposition of bioactive materials, which cannot be deposited or structured by the harsh conditions of thin film processing. It is expected that the focus for future applications will be the development of multiple processing tools that achieve a reasonable writing speed. The main challenge will lie in the area of reliability and the securing of proper working of each pen.

6.2 Bottom Up

Bottom up nanotechnology is the least developed area of nanotechnology. To manipulate atoms and molecules at atomic scale, a basic understanding of the processes at atomic scale is needed. Furthermore, equipment and processes must be able to combine atomic accuracy with volume demands. This problem is clearly seen with Scanning Probe Microscopes, which are used as nano manipulation tools.

Potentially Molecular Self Assembly -using molecules to create other molecules- is more favorable to become an industrial process for high volumes production, while it is in essence (bio) chemical processing. However, chemical processes are very difficult to scale up, and even at lab scale no suitable concepts have been developed yet. If the lifetime cycle follows the pattern of other material developments, full commercialization is not expected for another 15 – 20 years.

As the main part of the intellectual property (IP) for Molecular Self Assembly lies more in the processing and less in the equipment, licensing of process technology is an option. It is not clear if this area of the nanotechnology industry will allow for companies licensing out processes for MSA to develop in parallel with companies using their own propitiatory processes. Furthermore, there may not be a requirement for specialized equipment, besides the vast amount of process equipment already on the market for (bio) chemistry.

6.3 Nanoparticles

Technologies based on decreasing particle size to nanoscale dimensions face fundamental limitations. Future developments appear to focus on efficient processing technologies to create particles from the base chemicals and prevent agglomerization and clustering.

It should be noted that with regard to nanoparticles or fullerenes, the core enabler is the process. Thus, process knowledge and not equipment will be the most important differentiator among suppliers.

6.4 Nanotubes

Nanotube bulk production is causing an increase in availability and a decrease in price. The demand for specialized nanotubes, is increasing, allowing for the development of specialized process and separation equipment.

The major differentiator among suppliers will be the possession of equipment and processes to produce large quantities of nanotubes at low cost and with high purity.

7 Test and Measurement Equipment

In between the processing of base material and the delivery of the final product to the customer, a transformation of goals and methods of measurement and testing takes place. In the beginning the measurement is mainly done to control and improve the production process. As the materials are transformed into a product, gradually more and more aspects the final product characteristics will be tested. Following that transformation we divided the group of test and measurement concepts into the following types:

- Measurement of material properties; as an example the measurement of specific resistivity of a material
- Measurement of structural properties: for instance the measurement of the height of a structure
- Testing component properties, example: testing of resistance of an electrical coil
- Testing of application properties, mostly the performance of the finished products

7.1 Testing of MST/MEMS Material Properties

In depth knowledge of the material properties is essential for the understanding and prediction of device performance. The larger the object is, the more one can relay on the bulk material properties. For small devices one often sees deviation of material properties from the bulk and local deviation of properties. For thin film and more especially nanotechnology the surface properties become more important and often dominant. Measurement of these properties is therefore extremely important. The most important measurement technologies are:

7.2 In Situ Probing of Electrical and Mechanical Properties

Testing of materials used in the MST/MEMS production is an essential first step into quality control. Manufacturers of electronics, optical and medical devices, magnetic storage media, consumer goods, and automobiles can benefit from the fast and accurate mechanical characterization of many types of surfaces. Characterizing surfaces down to the level of a few nanometers has always been difficult. At this small scale, however, properties like hardness and modulus of elasticity can affect the performance of coatings, electronics, and implanted medical devices. The detailed knowledge of surface tribology, i.e. elasticity, adhesion and friction, on the micro- and nanometer scale is often important for the optimization of macroscopic material and surface properties. Making and indentation with a controlled force, while continuously monitoring the displacement of the indenter (the depth of the indentation), produces data from which the hardness of the material, Young's modulus, fracture behavior, and other mechanical properties can be calculated.

For nanoscale products it is of interest to measure electrical properties on nanoscale. The raising availability of scanning probe equipment gave a new input into the capabilities of the indentation equipment.

Due to their low working force range, mechanical microsystems are very sensitive to phenomena which are usually ignored in macroscopic mechanical systems, stiction[2] being one of them.

7.2.1 Particle Characterization

The stability, chemical reactivity, opacity, flowability and material strength of many materials are affected by the size and characteristics of the particles within them. The measurement of particle size is therefore an extremely important parameter cross many branches of industry. The upcoming nanotechnology industry increased the demand, especially for instruments capable of measuring at nanoscale. Particles can be measured by one or more of the following technologies:

- Sieves: cheap and readily usable for large particles, although with the availability of microfilters (Tfluxxion) also small particles (0.3 micron and larger) can be detected. Rodlike objects pass the filter dependent on their orientation. Suitable for low concentrations.

- Sedimentation: Traditionally used in paint and coatings industry. Practically limited to 2 – 50 microns and not suitable for low concentrations, also a slow process and sensitive to temperature etc..

- Electrozone testing (Coulter counting): capacitance measurement of a liquid with particle flowing through an orifice. In practice only used for blood testing

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[2] Stiction is the adhesion originating from contact of moving parts. This can result in immobilisation of the device.

- Microscopy. Cheap and instructive method while it gives information on the form of the particle. However, as it is a time consuming method, only a few particles are sampled leading to unrepresented sampling.

- Laser diffraction: this method relies on the fact that the diffraction angle is dependent on the particle size. Working in a range of 0.02- 3000 microns. It supplies reproducible information about size distribution.

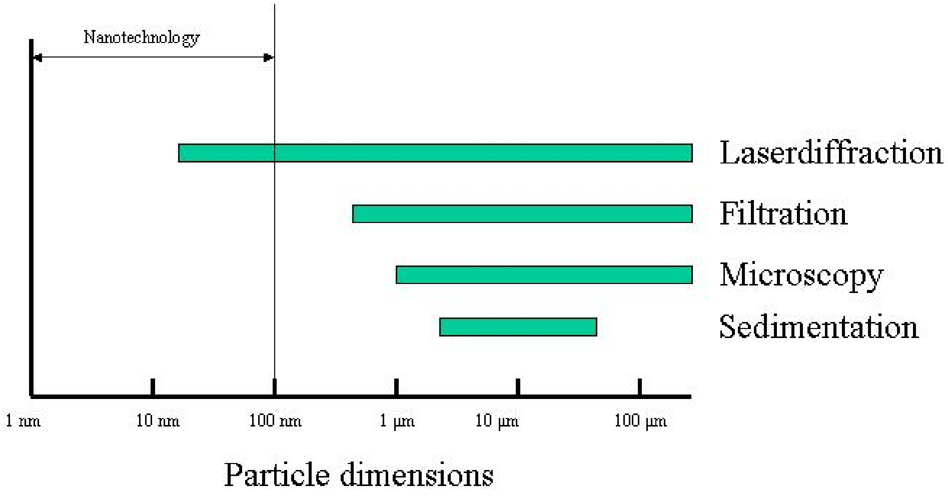

Figure 20: traditional particle measurement methodology.

As is shown in the graph traditional technologies only touch the nanotechnology arena. Several suppliers are now introducing equipment to the market expanding traditional technologies into the nanoscale domain.

7.3 Testing on MST/MEMS Structures

7.3.1 Thickness Measurement of Silicon

For some products micro structures are etched from the base silicon, with particular regions mechanically relieved and other regions firmly anchored. To create reliable and reproducible products the dimensions of those etched structures must be accurately controlled. As those dimensions are a result of etch time and thickness of the wafer, control of wafer thickness is critical to meet performance and component specification. Therefore there is a need for non-destructive, automated thickness monitoring instruments.

Mechanical thickness measurement is always an option, but unpractical, while it is difficult to automate this. Optical measurement can be an alternative, although is has several limitations:

Measuring thick layers of silicon is not trivial due to the high optical thickness (optical thickness = physical thickness * index, where index is about 3.5 for silicon), and because silicon more than a few microns thick is opaque in the visible wavelengths. This limits the use of optical thickness measurement of silicon to a few 100 microns.

The wafers must be double side polished.

7.3.2 3D Optical Measurement/Topography

Accurate measurement of layer thickness and structural dimensions of thin structures in the XY plane are well developed. MNT products offer a new challenge while they often feature three dimensional structures with very small dimensions and complex shapes due to internal or external stresses. The situation becomes even more complex when those small structures are not static and one wants to study their dynamic behaviour to check on hidden faults and investigate device performance.

The first profilometers where mechanical, but non-contact surface measurement based on laser and optical inspection technologies have so much advantages that they are now leading the market for static measurement. Their capabilities have been extended from simple line scans, to two dimensional area profile plotting in to three dimensional dynamic measurement of micro scale structures. One of the measurement complexities is the need to bring the structure into motion by supplying energy to the device to be measured. Nanoscale dynamic measurement will be the next stage.

7.3. Testing on MST/MEMS Components

7.3.1 Wafer Tester

Testing of the final product coming out of the waferfab is essential for:

- Getting direct feedback about the effectiveness and quality of the processing
- Select out of spec products from the good ones, either by scrapping complete wafer or by indicating faulty dies on the wafer for later selection after dicing.

Wafer testing is often the first time it becomes possible to do product performance testing instead of material and structural testing. In general most wafer testers are able to supply electrical data to the wafer and analyze the resulting electrical signals. This type of equipment is used in general in the semiconductor industry. MNT devices operate not only in the electrical domain, but also in others like optical, fluidic and mechanical, so that it requires wholly different systems from the one for the general semiconductor test process. First of all, an instrument to supply stable non electrical signals to the MNT device is required, and/or measuring technology with precision is necessary to detect the non-electric response produced. Even if the inputs and outputs are only electrical, the signal values can become a challenge especially with nanotechnology based products. Also different can be that special fixture technology is needed when physical force is applied on the device. MNT devices often have non standard dimensions and shapes or are fragile and in some cases must be tested under special environmental conditions.

7.3.2 Bonded Wafers

Voids, particles and other kind of contamination can cause local low quality bonding for wafer pairs used for MEMS or Silicon-On-Insulator (SOI) applications. Maintaining high yield and prevent yield related cost in back end processing makes it necessary to find the voids and defects as early as possible. Testing of the quality of bonded wafers is not trivial. As the to be inspected area is sandwiched between the two wafers, non of the traditional methods can be used.

7.4 Application Testing of MST/MEMS Products

To obtain an early estimation of product quality and get insight into the relation between process parameters and product characteristics, application testing or a comparable measurement is often done as early as possible. Before a set up a test program can be set up , one should estimate first the customers specification and transfer that to measurable quantities.

Although many MST/MEMS devices have their counterparts in traditional industries, sometime special test equipment is needed. Reasons can be diverse, but often because of the low signal levels, the fragility and the non standard dimensions of the devices.

7.4.1 Inertial Sensors

Not all mechanical testing of inertial sensors need elaborate sensing equipment. For example, drop testing is one of the best tools to confirm good mechanical design and stiction performance. Sometime the devices can be actuated by supplying an electrical signal, after which the response is measured in the form of a generated electrical signal. This makes testing on more or less standard equipment possible. Alternatively, the device is actuated by electrical input and the movements are analyzed by optical profilometers.

7.4.1 Optical Products

Optical backend processing (optical assembly) tend to be one of the most expensive ones in MNT due to the needed high accuracies needed. The ROI (Return on Investment) time for equipment to test and select the dies after waferfab processing to prevent faulty products entering the backend factory is often very short.

Another factor driving the need for accurate testing in optical MEMS can be the need to obtain specific performance values to tune the backend processing.

Systems for testing optical MEMS are designed with an emphasis on accuracy and industrial floor compatibility; they must be configurable to meet a wide range of customer specifications. They also must be able to characterize and monitor the stringent requirements for optical quality and performance of the optical telecommunications industry.

8 Summary and Conclusions

This chapter has focused on the processes adopted by manufacturers that cater specifically for back-end production of MST/MEMS and, possibly, MNT based products. It has assessed the processes in the context of commercial availability and accessibility addressing the various facets of the commercialization business. Commercial equipment for MST/MEMS front and back end processing is becoming more and more available. This applies equally for the specialized equipment as it does for the more general processing equipment. Given that the demands for MST/MEMS are less stringent compared to those placed by the semiconductors industry, second hand suppliers are, fortunately, able to cover a large portion of that market. In many cases semiconductors leads the way for MST/MEMS or supports ongoing developments here.

Over the past decade, semiconductors and MST/MEMS processing techniques have drifted apart although based on similar underlying processes. This is attributed to the fact that customer specific demands tend to rule and the IC industry was initially neglecting this market segment. As a consequence the MST/MEMS businesses and companies were forced to develop their own processes and equipment. It is noticed that there is a tendency to return to the benefits of the semiconductor industry by making use of (adapted) standard processing.

In this context, a comparable tendency in the market for back end equipment is also observed. The background is however different. In packaging and assembly MST/MEMS is often using (adapted) existing technology lines. With regards to equipment, MST/MEMS, semiconductor and other industries developments are often exploring similar technology options (see Figure 20).

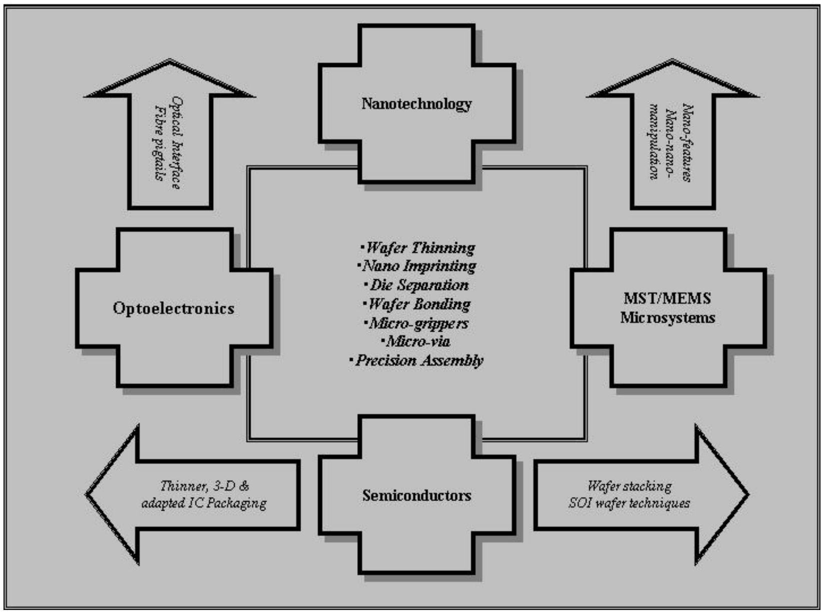

Figure 20: Driving forces on several processes used by the MST/MEMS and other industries (courtesy EnablingMNT)

A major challenge in micro assembly is to satisfy customer demands for:

- High volume option
- High quality
- Affordable prices
- Flexibility.
- Along with customer limitations in term of:
- (Initially) low volumes
- Application specific technology.

This demand leads to a tendency for imitating the high volume electronics manufacturing industries, although the limitations push for a job-shop kind of operation. The solution must lie in highly automated equipment working with standardized processes and specifications, as well as with fast set up options, to ensure the possibility of using such equipment for the assembly of multiple low volume products.

The quantities for each individual product in the market for MST/MEMS are relatively low and the product specifications tend to be very customer specific. Still, to be able to create and use affordable high volume assembly equipment and processes, standardization is a must. This is, as yet, hardly explored by this industry. In fact, this should become a focal point for product designers and equipment suppliers. The standardization efforts should be directed into specifications for:

- Interfaces (not only electrical but optical, fluidic and other)
- Component outer dimensions (required for parts feeding and handling)
- Processes (required for material development and equipment layout).

If possible specifications and standards from other markets / applications (especially high volume markets) should be exploited. Standardization in assembly equipment will ensure flexibility as it will offer the possibility to use the equipment for a wide range of products.

The difficulty to ensure cost effective assembly with high accuracies will force the designers towards the route of forward integration, creating, as much as possible, functionalities at the chip level. This is however hard to achieve in an economical fashion, as the yield will invariably decrease with increasing chip complexity. Assembly has always had the benefit of being confident of the quality of the individual functional parts, and the possibility of realizing parallel developments. Finally, the potential benefits of shorter interconnections will always be a bonus for forward integrated of multi-functional products.

The industry as a whole could benefit from exchange of information and consensus over process and product specifications and related equipment specifications.

It is however unlikely that industry wide roadmaps will play a role similar to the role played for the semiconductor industry. This is due to the fact that there is no MST/MEMS equivalent to the transistor and it is not to be expected there will be one. It is more likely, however, that application roadmaps will extend their influence into the MST/MEMS arena. In essence, the customers and the end users will determinate the roadmap and not the (equipment) suppliers. This will undoubtedly lead to a more diverse set of processes, equipment and standards in MST/MEMS as compared to semiconductors. A situation that is likely to create a much wider range of opportunities for smaller (equipment) suppliers, as long as they are able to combine flexibility with quality and staying power.

This study confirms that the areas of wafer bonding, backside alignment and Deep Reactive Ion Etching of silicon are well covered. In general, there is ample choice of equipment and, for wafer bonding and Deep Reactive Ion Etching, a good supply of services.

For silicon wet etching and LPCVD low stress nitride, the supply chain is less well organized. The reason for this lies in the possibility for customers to purchase equipment from local suppliers or use standard semiconductor equipment with only small process adjustments. HF vapor etching and super critical drying equipment is mostly used in other area and there is a limited availability of this type of equipment for MST/MEMS.

XeF_2 etching and electro deposition of resist are rather new processes introduced for MST/MEMS and it still remains to be seen if these processes will grow into a similarly strong position as wafer bonders DRIE equipment and backside aligners.