DESIGN CHAPTER 2010 UPDATES

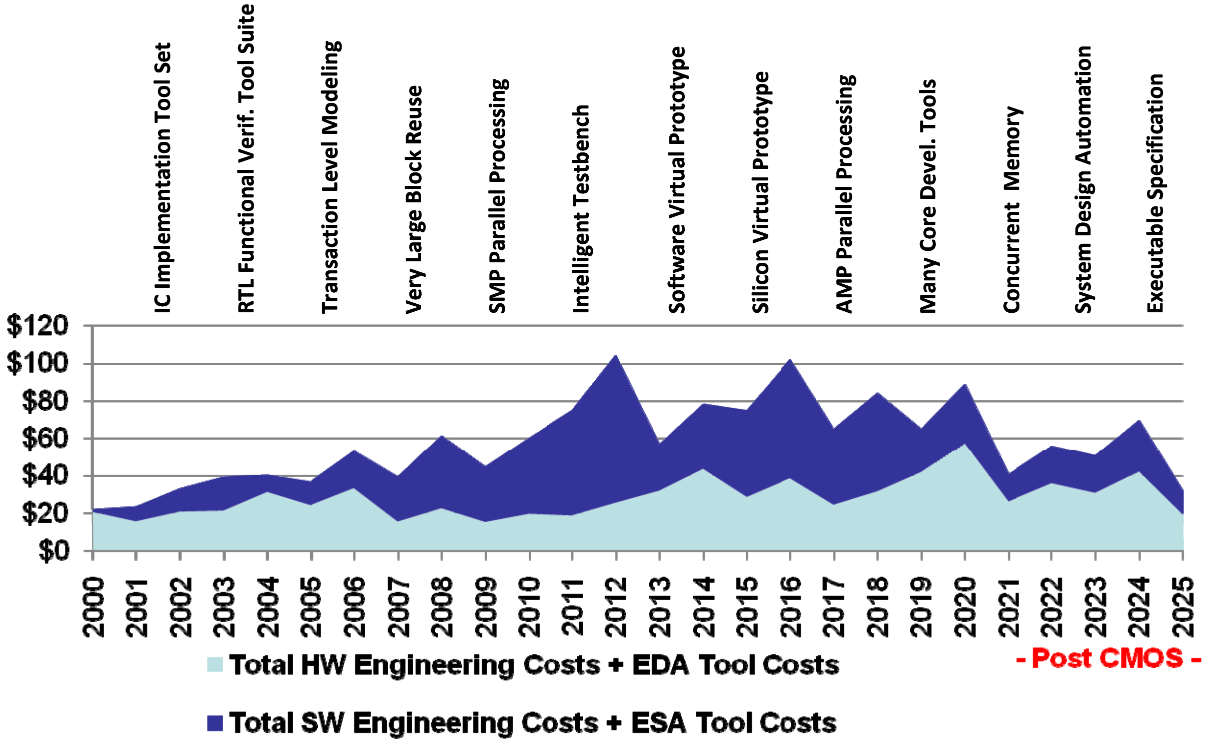

Figure DESN1 -- Impact of Design Technology on SoC SOC Consumer Portable Implementation Cost—UPDATED

ANALOG, MIXED-SIGNAL AND RF SPECIFIC DT TRENDS AND CHALLENGES — *UPDATED SECTION*

Analog/mixed-signal and RF circuits (AMSRF circuits) are different compared to digital circuits. Digital circuits contain coarsely quantized information that is interpreted in a defined range of voltage levels only. The two states of a bit (“high” (V_{dd} – noise tolerance) and “low” (V_{ss} + noise tolerance)) are widely separated by a forbidden band. Moreover, in synchronous circuits the signal levels are only interpreted at discrete time instances (such as clock edges). The signals processed in AMSRF circuits on the other hand are continuous in time and amplitude up to a much higher degree of precision. Therefore non-idealities like non-linearity, noise, parasitic elements, and any kind of parametric variation of the devices of the circuit directly cause distortion and noise in the analog or RF signals. Digital circuits have the built-in ability to suppress a high level of these noise sources due to a significant gain in the transition point of each logic gate and synchronous operating paradigm. This simple signal-recovery principle cannot be used in analog and RF signal processing due to continuous operation and the much higher dynamic range of the involved signals. Speed issues, or simply the fact that a signal-recovery circuit may produce more noise and distortion than it prevents, make these issues much more challenging and less straightforward in the analog domain.

AMSRF design inherently deals with a huge number of specific classes of design problems, each of which requires a customized design approach. An operational amplifier, a sense amplifier of a RAM, a phase-locked loop, an A/D converter, an analog receiver front end: Each requires its own design flow and optimization constraints. Therefore, “THE” AMSRF design flow does not exist, AMSRF design is full-custom and will never reach the same degree of automation as digital design. It should also be accepted that attempts to transfer design technology from the digital domain to the analog domain must fail due to the full-custom nature of AMSRF design. But as long as the fraction of AMSRF parts of a system is small enough that the effort for their design is small compared to the digital parts, and as long as every competitor has to deal with the same tasks this is not really a problem. However, recent advances in digital DT have lead to the situation where AMSRF components start to lie on the critical path of the chip design flow. In this situation, relief is produced in two ways of design technology enhancement: further AMSRF design automation, or, substitute analog components by digital circuit techniques.

FURTHER AMSRF DESIGN AUTOMATION

Interactive and semiautomatic AMSRF design. Despite continuing advances in academic algorithms for automated analog design, practical AMSRF design in industry is still manual if it goes beyond simulation. This has two reasons: First analog design is strongly interrelated to system design. For instance, the decision where to place gain elements, mixers, ADCs or DACs in the signal chain is a difficult one, as it depends on a huge number of system trade-offs and constraints that often cannot be translated into a goal-function. Even in the digital domain system and architecture decisions are not taken by synthesis tools but rather by experienced human system architects. Second the design of building blocks is hard to automize as goal and cost functions are usually multidimensional and the weighting between different performance figures is often based on experience and the knowledge on other system components and constraints. For example timing closure in digital design is a clear and hard criterion that is not subject to discussion. The decision to trade power for noise and accuracy, for instance, is a continuous soft constraint that depends on overall system specification and other building blocks in the signal chain.

Simulation based on more or less abstract models on transistor or behavioral level is virtually the sole area where EDA tools are frequently applied in practice. Synthesis and optimization on the other hand is still manual despite the available methods in literature and tools. Even the synthesis and optimization tools that find their way into the tool suites of big EDA vendors vanish from the scene after a while. As a roadmap to analog synthesis has been on the agenda for decades unsuccessfully, we should simply let go the goal of a digital-domain like synthesis process and set more realistic goals. Obviously, it is more desirable to support the manual AMSRF design process with computer aids and make it an interactive process between designer and computer tool. In the following, some major challenges in AMSRF design technology are described, which result from this interactive approach.

Parametric models and simulation of complex AMSRF blocks. As simulation is the acknowledged EDA method for design as well as for verification of AMSRF circuits, it must be enhanced to provide simulation of complex blocks that include both analog and (small) digital parts as well as both transistor level and behavioral level models (mixed-mode simulation). The designer must be enabled to simulate, e.g., a phase-locked loop, an A/D converter or a receiver frontend over a representative time interval. This can happen either as a whole, or in a two-step approach, where sub-blocks are simulated on transistor level and the results are transferred to the block simulation on behavioral level. If a two-step approach is taken, it should work automatically without an interactive requirement on the designer during simulation. The industrial state of the art is that transistor parameter extraction and transistor models allow the designer to automatically simulate simple AMSRF blocks like operational amplifiers. An extensive simulation of complex blocks like the mentioned ones does not yet exist. New technologies supplementing CMOS, like for instances carbon nanotubes, MEMS, or simply passives like coils and capacitors, lead to new types of sub-blocks that must be modeled and included into the simulation capability as well. The task is to provide complete models that can be used by the designer rather than providing the modeling methods and leaving the modeling to him. The solution of this task requires the cooperation of EDA engineers and design engineers. While EDA engineers contribute, e.g., automatic modeling methods like response surface modeling, symbolic analysis, design engineers contribute, e.g., the knowledge about the physical behavior to be modeled or the system requirements. Following the mentioned approach of interactive design support, the established sub-block and block models should not be buried in a synthesis flow or tool, but should be made available to the design engineer in the sense of library elements. Therewith, the designer is enabled to understand the challenges and trade-offs to make the adequate system decisions, e.g. can select a more appropriate architecture for the respective building block.

ADDED Table DESN Required Simulation Models for AMSRF Design*

Available 2010	Required 2011	Required 2012
Transistor models Transistor level models of OpAmps, oscillators, mixers, low noise amplifiers	Parameterized behavorial models of oscillators, mixers, low-noise amplifiers, etc, which are pin-compatible with corresponding transistor-level models	Parameterized behavioral models of phase-locked loops, A/D and D/A converters, receiver front ends, etc

**Table numbering will be updated in the 2011 edition of this chapter to avoid confusion with 2009 chapter numbering.*

Standardized modeling and analysis of physical effects and complex performance features. Besides the basic transient or frequency domain behavior that has to be captured by the above mentioned simulation models, it is necessary to provide a library of potentially relevant performance features and circuit parameters for each sub-block and block of the AMSRF circuit classes under consideration and the necessary items to automatically simulate these features. The simulation models of a circuit block or sub-block should therefore include

- the set of all potential performance features (like gain, bandwidth, phase margin, noise figure, input/output voltage range, PSRR, CMRR for an OpAmp)
- the simulation bench (extra circuitry and input stimuli) to simulate these features, and
- the extraction routines to compute these features from the output waveforms,

in such a way that the designer can select what he/she wants to simulate by simply pressing a button.

Appreciation of simulation as THE abstraction from the physical layer in AMSRF design. AMSRF design despite the physical foundation of its finely discretized signals provides a mean to abstract from the physical layer: simulation. While simulation itself still has a physical character due to the underlying differential equations, the subsequent extraction of well-defined performance features provides the establishment of a mathematical function, whose values depend on circuit parameters included in the simulation models. This mathematical function represents the abstraction from the physical layer of an AMSRF circuit to its mathematically abstract description $y=f(x)$. It is the task of the simulation models to provide not only the performance features y, but include any relevant parameter x, be it a design parameter like transistor width, a parameter from the manufacturing process like Vth, an operation parameter like temperature, or a parameter that describes the aging of a component. Simulation must be prepared in such a way that the mathematical model $y=f(x)$ is available point-wise. This means that a set of parameter values can be given, simulation is activated, and a set of performance values results without any user interaction. This automatic simulation is the crucial interface to any interactive and semi(or fully)-automatic design. Electronics circuit design usually follows a hierarchical approach. This must reflect also in the simulation tools—a small transistor level building block needs accurate modeling and simulation. After the block specification is met most of the internal performances figures may be dropped and only some relevant parameters must be passed to the next level of hierarchy. However, this level has to handle many blocks, i.e., a much higher complexity. An appropriate simulator may handle this increased complexity at reduced accuracy. According to state-of-the-art system design SPICE simulators are used for critical blocks, fast-MOS simulators for the next level, followed by VHDL-AMS, MATLAB/Simulink, and system C (or equivalent tools by other vendors). So far it is the task of the designer to choose and determine the relevant parameters and to pass them to the next level of hierarchy. Together with the automatic simulation approach proposed in the previous section it would be desirable to have a predefined interface to other simulators including automatic model and parameter generation. However, it has to be understood that this has nothing to do with synthesis.

Appreciation of simulation as THE interface for design automation in AMSRF design. There are several reasons why simulation should be an open interface from any EDA design tool or algorithm. The first reason is the mentioned abstraction from physics that simulation provides. An EDA design tool that allows to interact with arbitrary simulators will be applicable to a large class of design problems. Another reason is the customized simulation environments in industry. If an EDA design tools comes with its own simulator it will encounter unwillingness at the design side that is used to its own simulators. A third reason are the transistor and other models involved in simulation. They are usually specific to design classes and manufacturing technologies. Take what is there rather than bring in new models will increase the acceptance of an EDA design tool. This holds as well for response surface modeling techniques. While being attractive to reduce overall simulation cost of an EDA design tool, they add another source of modeling error which reduces acceptance on the designer side.

Provide simulators with sensitivity analysis capabilities. It has been fashionable, necessary and advantageous to provide simulators with extensive capabilities to write one's own models. However, this came at the cost of missing capability of simulators to perform a sensitivity analysis, e.g., using the adjoint method. Virtually any available simulator, with the exception of some inhouse simulators, nowadays cannot provide the sensitivity of performance features with regard to circuit parameters at reasonable cost, e.g., 10% CPU overhead per parameter. Instead, costly finite difference approaches have to be taken, involving a 100% CPU overhead per parameter. The reason lies in the missing sensitivity models that allow for an adjoint-method-based sensitivity analysis. It would be a blessing if simulators finally came up with a cheap sensitivity analysis, which give a first (linear) insight in how a multi-objective, multivariate design problem behaves in detail.

Education of AMSRF design engineers and EDA tool developers. Having accepted that AMSRF design is a process where EDA tools are applied in a customized way immediately leads to the requirement of an extended education of both, AMSRF designers and their counterparts developing EDA tools. In order to be able to select the right tools for his design problem and to be able to effectively apply these tools, a design engineer must know about the algorithms inside those tools. AMSRF design curriculums should therefore be supplemented with topics like statistics and numerical optimization. On the other hand, developers AMSRF design tools must know more about specific circuit classes and the actual design steps done by design engineers. EDA courses should therefore be supplemented with design courses. In addition, EDA tool developers should sit close to the designers, and engineers should work some time "on the other side", i.e., an AMSRF designer should also develop some tool sometime, and an EDA developer should design some circuit sometime.

AMSRF design tools are not for a flow but for a class of design problems. In trying to automate parts of AMSRF design tasks, there is no virtue in talking about general levels of abstraction and where synthesis switches between them like in digital design. It should rather be talked about the class of circuits that is targeted and that can be handled, e.g., as in the table above. In AMSRF design, we basically have the (nonlinear) transistor level, the hardware description level with some language (e.g., Verilog, VHDL) and the (linear) architectural level (e.g., Matlab/Simulink). Depending on the available models, we can include a transfer from one level to the other, but the synthesis and optimization process is based on whatever model is there. Having that in mind, there are a number of problems that still are not solved satisfactorily:

- Interactive design aids for the generation and selection of circuit structures
- Interactive design aids for placement and routing
- Interactive design for yield and reliability
- Discrete optimization (e.g. layout fingers, manufacturing grid)
- Closer interaction between structural synthesis and layout synthesis
- Design space exploration
- Enhanced simulation speed

Research on these tasks have to take great care on how self-explanatory the developed solutions are and how much "consulting overhead" they involve.

SUBSTITUTE ANALOG COMPONENTS BY DIGITAL CIRCUIT TECHNIQUES

Analog, mixed-signal, and RF circuits have always been susceptible to parameter and environmental variations. Indeed variability and circuit sensitivity increase, but the basic problem is not new. Countermeasures in terms of trimming, calibration loops, digital calibration and error correction are well known techniques. However, their realization was often not feasible due to area and power penalties. In nano-scale CMOS technologies power and area consumption per basic digital function is incredibly low so complex calibration and correction engines become affordable. If the amount of analog and RF components can be reduced or if the accuracy requirements can be reduced by adding some thousands of digital gates, these gates should be spent. The same holds if digital assist techniques can improve the analog performance by forground/background calibration and/or redundancy, and/or error correction. Even if the digital approach does not pay off immediately, it should be taken into account as the digital shrink factor assures a benefit in the next or over next product generation.

Ongoing device scaling will further degrade the analog device performance, especially the intrinsic gain of a single transistor. Circuit techniques for gain and accuracy improvement such as cascodes become impractical due to the small voltage headroom of around 1V. As noise does not scale the decreasing signal levels lead to diminishing signal-to-noise ratios. Digital delays on the other hand scale continuously. The same holds for area and power of basic digital gates. This leads to an emerging class of mixed-signal circuits, namely time-to-digital converters. Time-to-digital converters are data converters that quantize a continuous input signal. While ADCs work on continuous voltages TDCs work on continuous time intervals. The first and most prominent example for a successful application of time-to-digital converters is the all-digital phase-locked-loop.

It is to be understood that it is neither the goal nor possible to fully replace analog functionality by digital realizations. Often analog realizations are not only straight forward but also cheaper and better in performance than digital ones. However, digital assist techniques shall improve the overall system performance, improve reproducibility, and provide a simple and powerful interface. Obviously these advantages do not come for free: Extensive digital circuitry near analog/RF building blocks cause not only additional power consumption but may pollute substrate and power supply so may lead to increased noise levels.