

16-17 July ITRS IRC/ITWG 2007 Summer Workshop and 18 July ITRS Public Conference



IRC/ITWG Plenary
Meeting Handout



ITRS IRC/ITWG Workshop Objectives

Prepare for finishing the 2007 ITRS by August 31, 2007

- **Meet with Teams to *finish***
 - **challenges,**
 - **technology requirements, and**
 - **potential solutions charts**

Prepare for conference

- **Final presentations due to Sarah Mangum by lunchtime,
Tuesday 17 July**

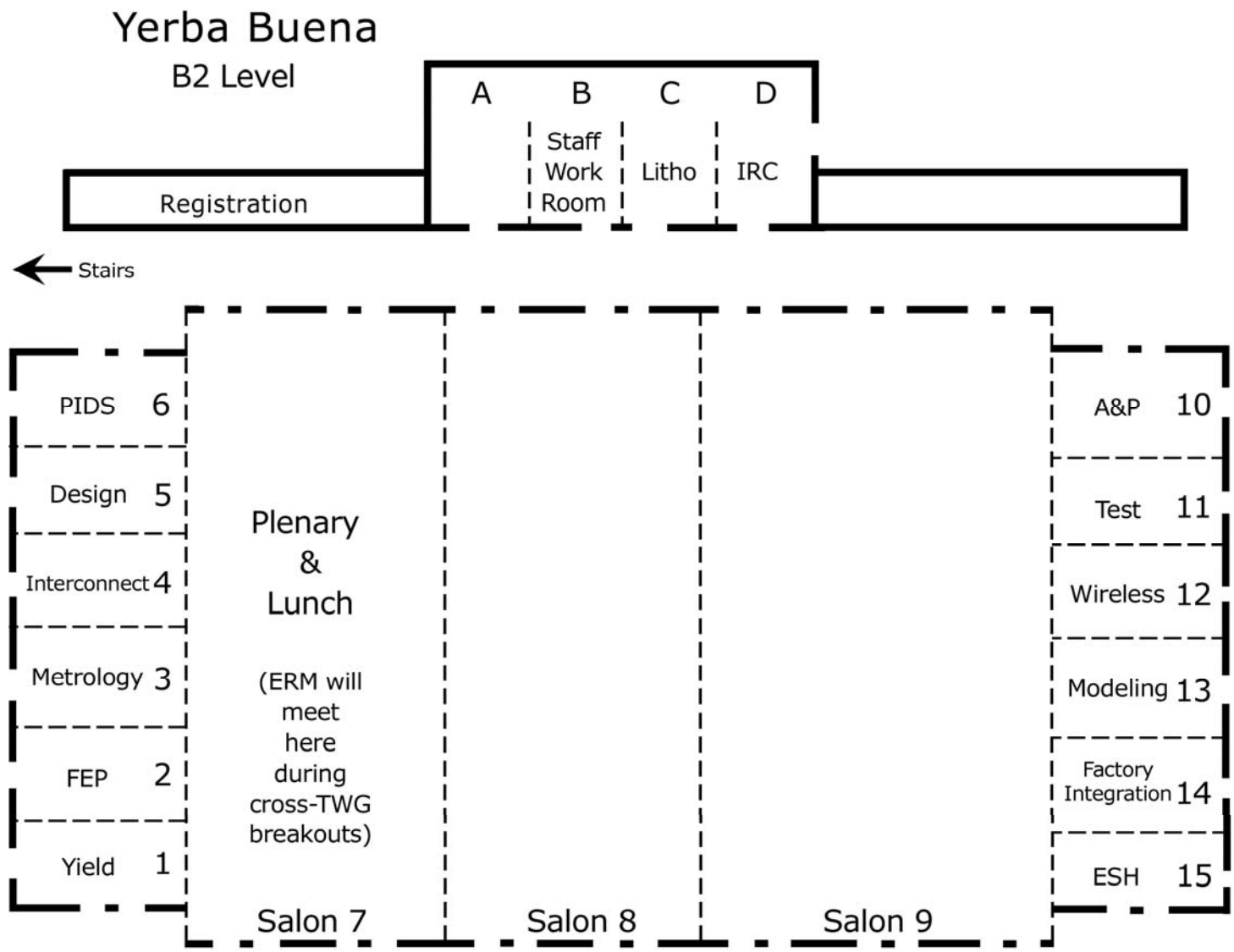


ITRS IRC/ITWG Events

- Monday Evening – SEMI Presidents' Reception
 - 6:00pm–7:30pm
 - West Hall, Level 2, Moscone Center
 - San Francisco, CA
- Tuesday – SEMI Keynote Speech 1:30 – 2:30: Paolo Gargini
- Tuesday Evening -- ITRS Dinner at the California Academy of Sciences
- Wednesday – ITRS Networking Social
(ITRS teams are invited to the SEMATECH VIP/20th Anniversary Reception back at the Marriott afterwards)



ITWG/IRC Room Assignments – Marriott Hotel Yerba Buena (B2 Level)



Tuesday, July 17 – Marriott Hotel (except for evening event)

- 9:00 – 12:00 IRC/ITWG Breakouts
 - Coffee break available from 10:00 to 10:30
- 12:00 – 13:15 Lunch
- 13:30 – 17:00 IRC/ITWG Breakouts
 - Coffee break available from 16:00 to 16:30
- 17:00 – 18:30 Plenary session including Winter and 2008 Spring meeting announcements
Key messages from all ITWGs
- 18:30 Adjourn
- 19:00 Dinner at the California Academy of Science

NOTE for Tuesday after Lunch

*Option to attend the
SEMI Keynote Address
by Paolo Gargini from 13:30-14:40*



July 16-17, Breakout Schedule:

IRC, Factory Int., Modeling & Simulation, Assembly & Packaging, Lithography

Day 1 ITWG/IRC Meetings					
	IRC Team Meetings	Factory Int. Team Meetings	Modeling Team Meetings	Assy&Pkg Team Meetings	Lithography Team Meetings
8:30-9:00	Registration				
9:00-10:00	[at Plenary]				
10:00-10:30 Coffee Break is Available					
10:30-11:30	IRC - 300/450mm at 11	Factory	Modeling	Assy&Pkg	Lithography
11:30-12:30		Factory	[meet in Design area]	Assy&Pkg / ESH	Lithography / ERM
12:30-14:00	LUNCH				
14:00-14:45	IRC / A&P	Factory	Modeling	Assy&Pkg - IRC	Lithography
14:45-15:30	In Plenary Room MtM Meeting with IRC/ 6 TWGs 14:45-16:00	Factory	[meet in FEP area]	In Plenary Room MtM Meeting with IRC/ 6 TWGs 14:45-16:00	Lithography
15:30-16:30		Factory	Modeling / ERM		Lithography / Yield
16:00-16:30 Coffee Break Available					
16:30-17:00	IRC	Factory	Modeling	Assy&Pkg / Interconnect	Lithography
17:00-17:45	IRC	Factory	Modeling	Assy&Pkg / Test	In Plenary Room Meeting with Litho/FEP/ Design/PIDS
18:00	SEMI Presidents' Reception -- West Hall, Level 2, Moscone Center -- NO DINNER				



July 16-17, Breakout Schedule:

IRC, Factory Int., Modeling & Simulation, Assembly & Packaging, Lithography

Day 2 ITWG/IRC Meetings					
	IRC Team Meetings	Factory Int. Team Meetings	Modeling Team Meetings	Assy&Pkg Team Meetings	Lithography Team Meetings
9:00-10:00	IRC	Factory	Modeling	Assy&Pkg	Lithography
10:00-10:30 Coffee Break is Available					
10:30-11:15	IRC - MEMS team at 11	Factory	Modeling / Interconnect	Assy&Pkg	Lithography
11:15-12:00		Factory	Meet in Assy&Pkg area	Assy&Pkg/ Modeling	Lithography
12:00-13:15 LUNCH					
13:30-14:45 LUNCH until 13:15 /Option to attend SEMI Keynote by Paolo Gargini from 13:30-14:30					
13:30-14:00	IRC/PG speech	Factory	Modeling	Assy&Pkg	Lithography
14:00-14:45	IRC/PG speech	Factory/ Yield	Modeling	[meet in Design area]	Lithography
14:45-15:30	IRC	Factory / Metrology	Modeling	Assy&Pkg	Lithography / ESH
15:30-16:00	IRC	Factory / Litho	Modeling	[meet in RF/AMS Wireless area]	[meet in Factory area]
16:00-16:30	IRC/ TSV	Factory/ESH	[meet in Litho area]	Assy&Pkg / IRC	Lithography / Modeling
16:00-16:30 Coffee Break Available					
16:30-17:00	IRC	Factory / FEP	Modeling / PIDS	Assy&Pkg / ERM	Lithography / Metrology
17:00-18:15	[at Plenary]	[at Plenary]	[at Plenary]	[at Plenary]	[at Plenary]
18:30-22:00	IRC and ITWG DINNER -- California Academy of Science				



July 16-17, Breakout Schedule: Front End Processes, RF/AMS Wireless, ESH, Interconnect, Metrology

Day 1 ITWG/IRC Meetings					
	FEP Team Meetings	RF/AMS Wireless Team Meetings	ESH Team Meetings	Interconnect Team Meetings	Metrology Team Meetings
8:30-9:00	Registration				
9:00-10:00	[at Plenary]				
10:00-10:30 Coffee Break is Available					
10:30-11:30	FEP	RF/AMS Wireless	ESH	Interconnect	Metrology
11:30-12:30	FEP	RF/AMS Wireless	[meet in Assy&Pkg area]	Interconnect	Metrology
12:30-14:00	LUNCH				
14:00-14:45	FEP / PIDS	RF/AMS Wireless	ESH	meet in Yield area	Metrology
14:45-15:30	FEP / Modeling	In Plenary Room MtM Meeting with IRC/ 6 TWGs 14:45-16:00	ESH/ERM	In Plenary Room MtM Meeting with IRC/ 6 TWGs 14:45-16:00	Metrology
15:30-16:30	FEP		ESH		Metrology
16:00-16:30 Coffee Break is Available					
16:30-17:00	FEP/Metrology	RF/AMS Wireless	ESH	Interconnect meet in Assy&Pkg area	[meet in FEP area]
17:00-17:45	In Plenary Room Meeting with Litho/FEP/ Design/PIDS	RF/AMS Wireless	ESH	Interconnect/ ERM	Metrology / Yield
18:00	SEMI Presidents' Reception -- West Hall, Level 2, Moscone Center -- NO DINNER				



July 16-17, Breakout Schedule: Front End Processes, RF/AMS Wireless, ESH, Interconnect, Metrology

Day 2 ITWG/IRC Meetings					
	FEP Team Meetings	RF/AMS Wireless Team Meetings	ESH Team Meetings	Interconnect Team Meetings	Metrology Team Meetings
9:00-10:00	FEP	RF/AMS Wireless	ESH	Interconnect	Metrology
10:00-10:30 Coffee Break is Available					
10:30-11:15	FEP/ ERM	RF/AMS Wireless	ESH/Yield	[meet in Modeling area]	Metrology
11:15-12:00	FEP/Yield	RF/AMS Wireless	ESH	Interconnect	Metrology
12:00-13:15	LUNCH				
13:30-14:45	LUNCH until 13:15 /Option to attend SEMI Keynote by Paolo Gargini from 13:30-14:30				
13:30-14:00	FEP	RF/AMS Wireless	ESH	Interconnect	Metrology
14:00-14:45	FEP	RF/AMS Wireless	ESH	Interconnect	Metrology
14:45-15:30	FEP/ Interconnect	Wireless / PIDS	[meet in Litho area]	[meet in FEP area]	[meet in Factory area]
15:30-16:00	FEP / ESH	Wireless / Assy&Pkg	[meet in FEP area]	[meet in Metrology area]	Metrology / Interconnect
16:00-16:30	FEP	[meet in Test area]	[meet in Factory]	Interconnect / IRC	Metrology / ERD/ERM
16:00-16:30 Coffee Break is Available					
16:30-17:00	[meet in Factory area]	Wireless / Design	[meet in Interconnect area]	Interconnect / ESH	[meet in Litho area]
17:00-18:15	[at Plenary]	[at Plenary]	[at Plenary]	[at Plenary]	[at Plenary]
18:30-22:00	IRC and ITWG DINNER -- California Academy of Science				



July 16-17, Breakout Schedule: Process Integration, Yield Enhancement, Design/System Drivers, Test, ERM

Day 1 ITWG/IRC Meetings					
	PIDS Team Meetings	Yield Enhnc. Team Meetings	Design Team Meetings	Test Team Meetings	ERM Team Meetings
8:30-9:00	Registration				
9:00-10:00	[at Plenary]				
10:00-10:30 Coffee Break is Available					
10:30-11:30	PIDS	Yield	Design	Test	ERM
11:30-12:30	PIDS	Yield	Design / Modeling	Test	Meet in Litho area
12:30-14:00	LUNCH				
14:00-14:45	[meet in FEP area]	Yield / Interconnect	Design	Test	ERM
14:45-15:30	In Plenary Room MtM Meeting with IRC/ 6 TWGs 14:45-16:00	Yield	In Plenary Room MtM Meeting with IRC/ 6 TWGs and Weil/Le Masson 14:45-16:00	Test	Meet in ESH area
15:30-16:30		[meet in Litho area]		Test	Meet in Modeling area
16:00-16:30 Coffee Break is Available					
16:30-17:00	PIDS	Yield	Design	Test	ERM
17:00-17:45	In Plenary Room Meeting with Litho/FEP/ Design/PIDS	[meet in Metrology area]	In Plenary Room Meeting with Litho/FEP/ Design/PIDS	[meet in Assy&Pkg area]	Meet in Interconnect area
18:00	SEMI Presidents' Reception -- West Hall, Level 2, Moscone Center -- NO DINNER				



July 16-17, Breakout Schedule: Process Integration, Yield Enhancement, Design/System Drivers, Test, ERM

Day 2 ITWG/IRC Meetings					
	PIDS Team Meetings	Yield Enhnc. Team Meetings	Design Team Meetings	Test Team Meetings	ERM Team Meetings
9:00-10:00	PIDS	Yield	Design	Test	ERM
10:00-10:30 Coffee Break is Available					
10:30-11:15	PIDS / Design	[meet in ESH area]	[meet in PIDS area]	Test	Meet in FEP area
11:15-12:00	PIDS	[meet in FEP area]	Design / Test	[meet in Design area]	ERM
12:00-13:15	LUNCH				
13:30-14:45	LUNCH until 13:15 /Option to attend SEMI Keynote by Paolo Gargini from 13:30-14:30				
13:30-14:00	PIDS	Yield	Design	Test	ERM
14:00-14:45	PIDS	Yield (meet in Factory area)	Design / Assy&Pkg	Test	ERM
14:45-15:30	[meet in Wireless area]	Yield	Design	Test	ERM
15:30-16:00	PIDS	[meet in Design area]	Design / Yield	Test	ERM
16:00-16:30	[meet in Yield area]	Yield/PIDS	Design	Test / Wireless	Meet in Metrology area
16:00-16:30 Coffee Break is Available					
16:30-17:00	[meet in Modeling area]	Yield	[meet in Wireless area]	Test	ERM meet in Assy&Pkg area
17:00-18:15	[at Plenary]	[at Plenary]	[at Plenary]	[at Plenary]	[at Plenary]
18:30-22:00	IRC and ITWG DINNER -- California Academy of Science				



ITRS Public Conference —

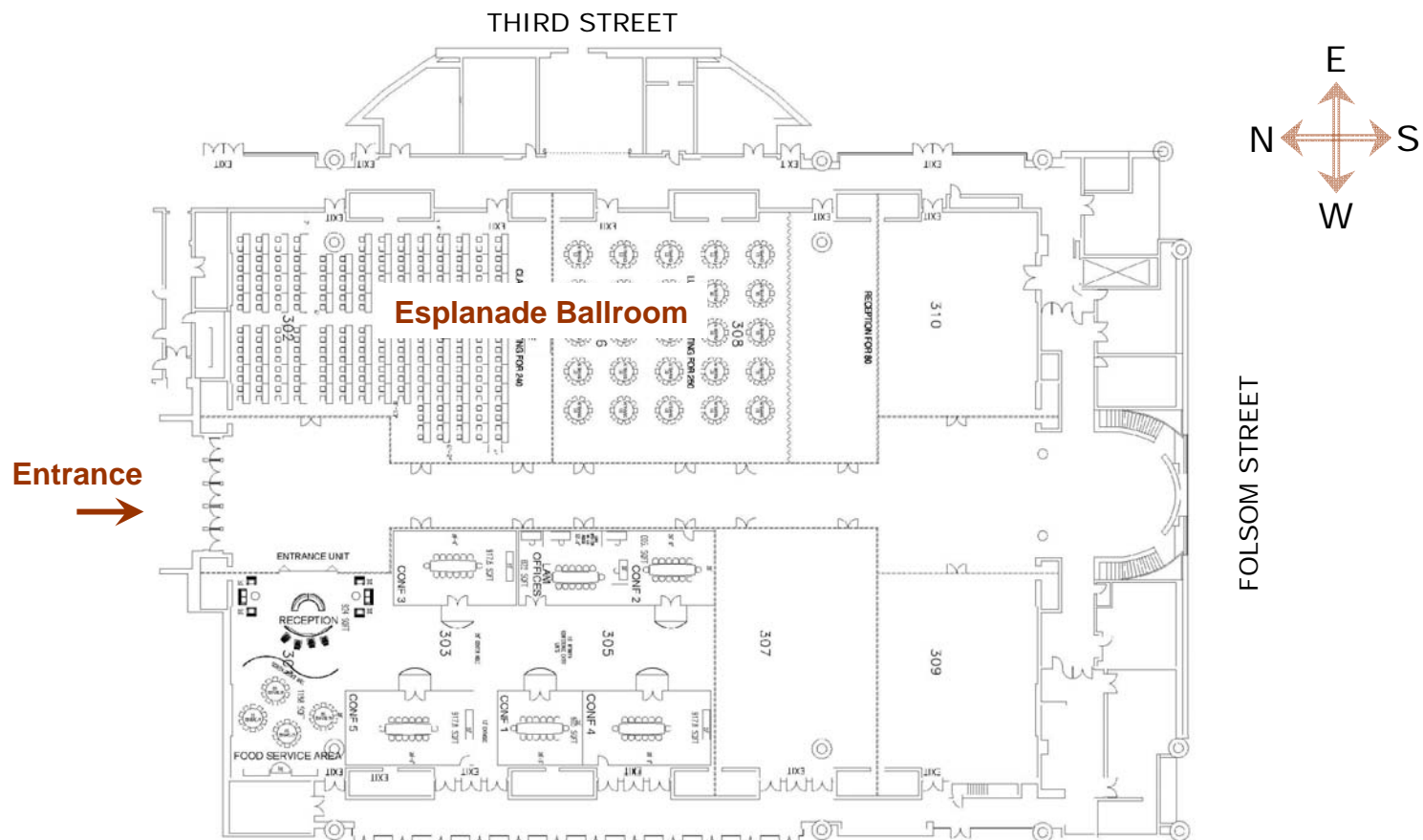
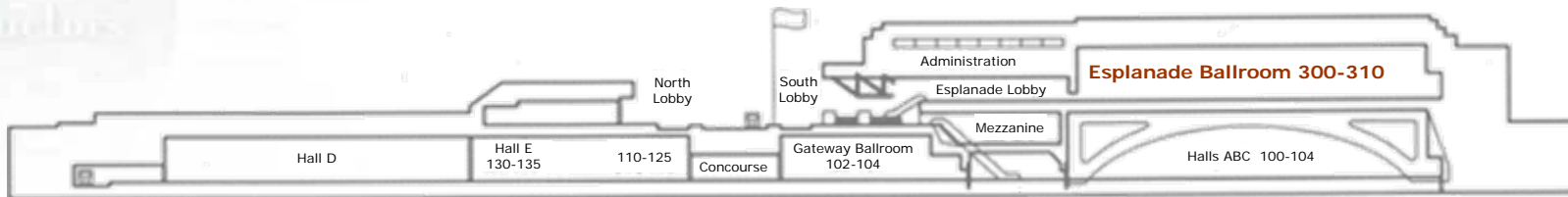
- Co-hosted by



- *All* working groups will present.
- All final presentations due to Sarah Mangum by lunchtime on Tuesday, July 17.
- There is a *More than Moore* panel discussion after lunch with IRC representatives and several working group chairs.



ITRS 2007 Summer Public Conference – The Moscone Center in the Esplanade Hall Ballroom



INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
2007 ITRS PUBLIC CONFERENCE

18 JULY 2007 THE ESPLANADE AT THE MOSCONE SAN FRANCISCO, CALIFORNIA

MORNING AGENDA

7:30	Registration and Continental Breakfast	
8:00-8:15	Opening Remarks & Orientation	
	<i>ESIA – Wolfgang Arden</i>	
	<i>JEITA – Toshihiko Osada</i>	
	<i>KSIA – TBA *</i>	<i>IRC members</i>
	<i>TSIA – Carlos Diaz</i>	
	<i>SIA – Bob Doering</i>	
	8:15 – Session 1 Greetings by Europe IRC – Mart Graef	
8:15-8:35	Overall Roadmap Technology Characteristics	<i>Alan Allan</i>
8:35-8:55	Process Integration, Devices, and Strucs.	<i>Peter Zeitzoff</i>
8:55-9:15	Emerging Research Materials	<i>Mike Garner</i>
9:15-9:35	Emerging Research Devices	<i>Jim Hutchby</i>
9:35-9:45	Q&A	
9:45-10:00	Break and Poster Review	
	10:00 – Session 2 Greetings by Japan IRC – Toshihiko Osada	
10:00-10:20	RF and A/MS Technologies for Wireless Comm.	<i>Herb Bennett</i>
10:20-10:40	Metrology	<i>Alain Diebold</i>
10:40-11:00	Environment, Safety, and Health	<i>Jim Jewett</i>
11:00-11:20	Lithography	<i>Mike Lercel</i>
11:20-11:30	Q & A	
11:30-13:00	Lunch	



**INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS
2007 ITRS PUBLIC CONFERENCE**

18 JULY 2007 THE ESPLANADE AT THE MOSCONE SAN FRANCISCO, CALIFORNIA

AFTERNOON AGENDA

13:00 – 14:00 Panel Discussion --- More than Moore, Paolo Gargini, chair

*IRC presenters: Mart Graef, Patrick Cogez, Hidemi Ishiuchi, Alan Allan, Pushkar Apte
Working Group Panelists: Harold Hosack, Jack Pekarik, Juan-antonio Carballo, Peter Zeitzoff,
George Bourianoff, Bill Bottoms*

14:00 – Session 3 Greetings — Pushkar Apte

14:00-14:20	Test & Test Equipment	<i>Roger Barth</i>
14:20-14:50	System Drivers and Design	<i>Juan-antonio Carballo</i>
14:50-15:10	Interconnect	<i>Christopher Case</i>
15:10-15:30	Factory Integration	<i>Mani Janakiram</i>
15:30-15:40	Q & A	
15:40-16:00	Break and Poster Review	

16:00 – Session 4 Greetings by Taiwan IRC — Carlos Diaz

16:00-16:20	Yield Enhancement	<i>Lothar Pfitzner</i>
16:20-16:40	Front end Processes	<i>Jeff Butterbaugh</i>
16:40-17:00	Modeling and Simulation	<i>Jurgen Lorenz</i>
17:00-17:20	Assembly and Packaging	<i>Bill Bottoms</i>
17:20-17:30	Q & A	
17:30-17:45	Open Discussion & Closing Remarks	<i>Paolo Gargini</i>
17:45-18:30	ITRS Networking Social	

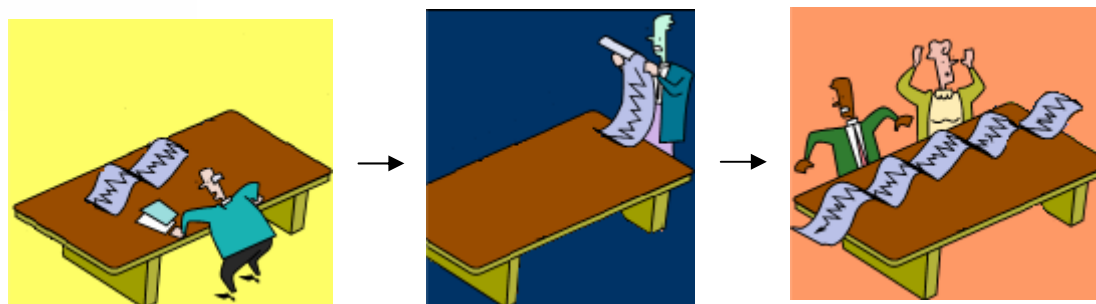


2007 ITRS Schedule

- ▶ Jul 16 – 17 ITRS ITWG/IRC meeting in San Francisco at the Hotel Marriott
2007 drafts are reviewed by ITWGs and CrossTWGs
- ▶ Jul 18 ITRS Public Conference at the Moscone Center, Esplanade Hall
- July 20 ALL FINAL tables due and shared among all teams
- Aug 31 ALL FINAL drafts chapter WRITING is due [tables, figures, TEXT]
Drafts to editor and IRC at this date –
NO EXCEPTIONS
IRC needs to write the Executive Summary
Editor needs to produce 2007 document
Working with 16 TWG editors
- Sep 15** **2007 ITRS content is frozen**
[ANY additional or late material deferred to 2008 ITRS]
Citations with permissions, Linked files, Acknowledgements due!
- Oct Regional Executives Advisory board approve ITRS
- Nov 9 Presentation Drafts due for preparing for
December Public meeting materials
- ▶ Dec 3-4 ITRS ITWG/IRC meetings TBD Hotel, Kamakura, Japan
- ▶ Dec 5 ITRS Public Conference TBD Hotel, Makuhari, Japan
- December 2007 ITRS is posted online for the public



2007 ITRS Editing Process



- ITRS edit team is ready to help !
- ALL tables are in 2 Excel files.
- ALL 2005 – 2006 materials are available and editable.
 - Online information – easy to download and revise as Word, Excel, or Powerpoint
 - Text from 2005/2006 available online as Word files
 - Pre-formatted charts in either Visio or Excel

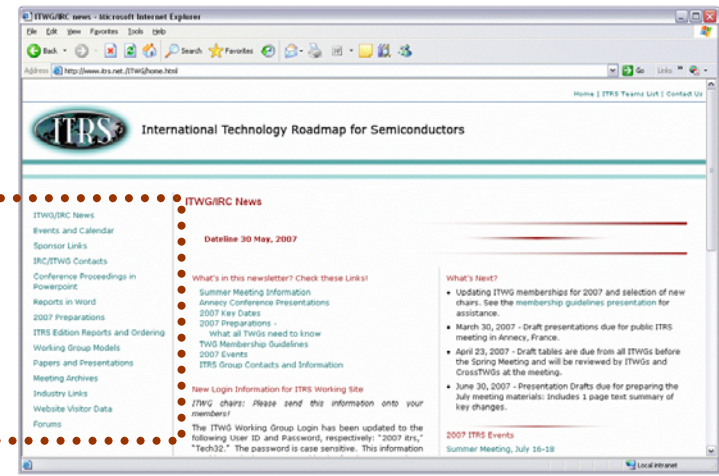




- ITWG/IRC News
- Events and Calendar
- Sponsor Links
- IRC/ITWG Contacts
- Conference Proceedings in Powerpoint
- Reports in Word
- 2007 Preparations

- ITRS Edition Reports and Ordering
- Working Group Models
- Papers and Presentations
- Meeting Archives
- Industry Links
- Website Visitor Data
- Forums

Online Information ITWG Site Pages



Online Information ITRS Chapters in Word !

- ITWG Site Login page
 - User ID is **2007 itrs**
 - Password is **Tech32**

<http://www.itrs.net/login.cfm>



- Word files
 - <http://www.itrs.net/Links/2007ITRS/2007Preparations.html>
 - Other 2007 preparation files are also on this page



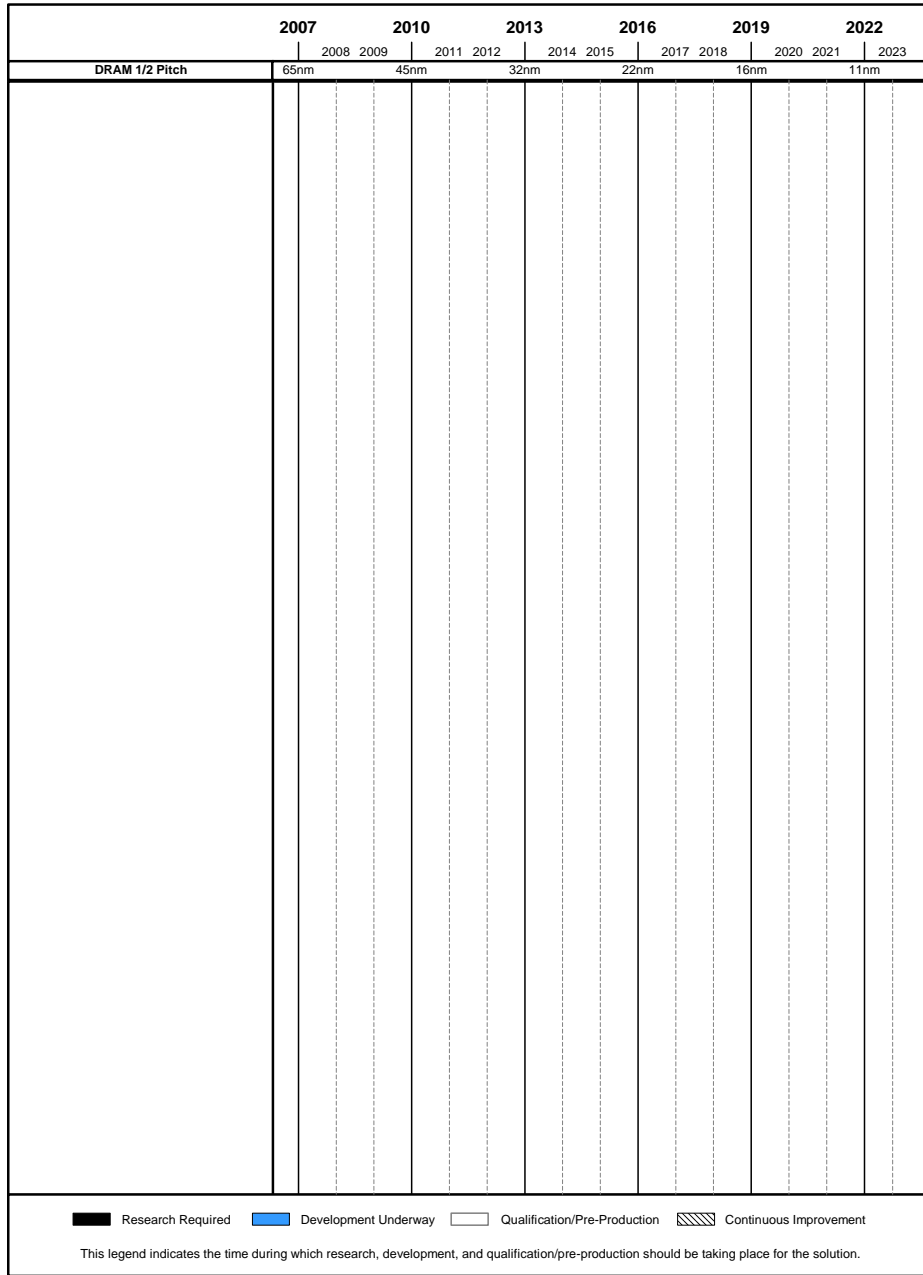
Online Information ITRS Tables in Excel !

- Excel files
 - All ITRS tables in 2 Excel files for all working groups to use/compare
 - Indexed for ease in finding specific tables
 - Download from ITRS website

The screenshot shows a complex Excel spreadsheet with multiple columns and rows. The data is color-coded, with yellow and red cells indicating specific values or trends. The table appears to be a detailed technical specification or performance comparison across different technology nodes.

2007 Potential Solutions Charts

Visio

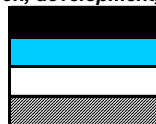


2007 Potential Solutions Charts Excel

First Year of IC Production DRAM 1/2 Pitch	2007 65nm	2008 57nm	2009 50nm	2010 45nm	2011 40nm	2012 35nm	2013 32nm	2014 28nm	2015 25nm	2016 22nm	2017 20nm	2018 18nm	2019 16nm	2020 14nm	2021 13nm	2022 12nm

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

- Research Required
- Development Underway
- Qualification / Pre-Production
- Continuous Improvement



2007 Page Count Allocation –
Chapters size – *including citations' pages*

Executive Summary	60
ORTC	32
System Drivers	25
Design	53
Test and Test Equipment	63
Process Integration, Devices, and Structures (PIDS)	55
RF and Analog/Mixed Signal Technologies for Wireless Communications	40
Emerging Research Devices (ERD)	74
Front-End Processes (FEP)	66

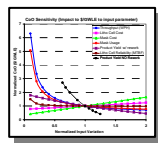
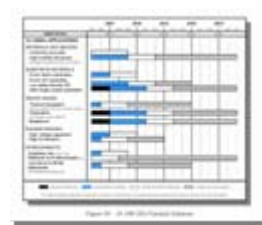
Lithography	29
Interconnect	62
Factory Integration	45
Assembly and Packaging	50
Emerging Research Materials (ERM)	45
Environment, Safety, and Health (ESH)	27
Yield Enhancement	41
Metrology	47
Modeling and Simulation	36



The Final Stretch !

...Due August 31 – 4 files!

- One Chapter file ...
Word
- One Table file ...
Excel
- One Potential Solutions file ...
Excel or Visio
- One Figures file ...
Powerpoint



Due August 31 !

1. Chapter file -- Word document file including references/works cited AND acknowledgments

- ***NO individual sections sent separately***
- **Add placeholders to show where tables and figures need to be placed in the Chapter.**
- **Start the numbering of the tables, figures, and footnotes at 1.**

The Final Stretch !

ACKNOWLEDGMENTS

INTRODUCTION, MICROWELL COAST/ITRS
 #Fengze - Wolfgang Anden, Patrick Cypri, Mark Oshro, Gerhard Guder
 #Angeles - Robert Bensch, Toshihiro Oishi
 #Kobayashi - Jun-ichi Nakata, Shigenori Chikama
 #Furuta - Ming-Ching Chang, Chien-Hsiang Liu, C.Y. Lu
 #C.I.A. - Pauline Apts, Bob Downing, Peter Grogan

TECHNOLOGY WORK

Chip-Start Challenge
 Donald Haskel, ITRI
 Shigeru Yamada, LSI
 Kenjiro Yamada, ITRI
 Kazuo Nishimura, ITRI
 Masahiro Iwano, ITRI
 Gao Chen, Tsinghua
 Wolfgang Eder, ITRI
 Shigeru Takagi, Tsinghua
 Andrew Kahng, Intel
 Jun-ichi Kim, Toshiba
 Toshihiro Oishi, ITRI
 Jun-ichi Nakata, ITRI
 John Hradky, Intel
 Martin Schaeffgen, ITRI
 Tai-Kang Tang, ITRI
 Paul Werneck, LSI
 Ichiro Yamamoto, ITRI
 Eui and Eui-Eun
 Gyeong-Ah Park, Daejeon
 Hyeon-Ho Park, ITRI
 Gordon Green, ITRI
 Stefan Eckstein, ITRI
 Mike Harris, Kacific
 Howard Wang, Taiwan
 Matt Lindemann, ITRI
 Peter Mariani, ITRI
 Yasuhiko Nakamura, ITRI
 Matt Green, Intel
 Charles Eubank, ITRI
 Lee Song, Chameleon
 Dan Van Overbeek, ITRI
 Cheng Wen Wu, ITRI
 Takanori Endo

Process Integration: J

REFERENCES

MEMBER

1. Elzard, K., et al. "A Silicon Nanocrystal Based Memory." *Applied Physics Letters*, 68 (1996): 1377.
2. Lombardo, S., B. De Salvo, C. Garabiti, and T. Benelli. "Silicon nanocrystal memories." *Microelectronics Engineering*, 72 (2004): 188-194.
3. Wang, X., et al. "A novel MCMOS-type nonvolatile memory using high-dielectricity for improved data retention and programming speed." *IEEE Trans. Electron Devices*, 51.4 (2004): 597.
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5. Ehrman, F., F. Capozzi, J. E. Walker, and R. J. Malik. "Memory Phenomena in Heterostructure Structures - Evidence For Suppressed Thermionic Emission." *Applied Physics Letters*, 53 (1988): 376.
6. Libaver, K. K. "Riding the crest of a new wave in memory." *IEEE Circuits and Devices*, 36.4 (2000): 16-21.
7. Ciavarella, B., P. Romano, M. Romanello, J. Van Haack, and K. De Meyer. VARIOT: a novel multilayer tunnel barrier for low-voltage, nonvolatile memory devices. *IEEE Electron Device Letters*, 24.2 (2003): 99-101.
8. Ehrman, F., F. Capozzi, J. E. Walker, and R. J. Malik. "Memory Phenomena in Heterostructure Structures - Evidence For Suppressed Thermionic Emission." *Applied Physics Letters*, 53 (1988): 376.
9. <http://www.itrs.net>

DESIGN

SCOPE

Design technology (DT) enables the conception, implementation, and validation of microelectronics-based systems. Elements of DT include tools, libraries, manufacturing process characterizations, and methodologies (DT transforms ideas and objectives of the electronic systems designer into manufacturable and testable representations. The role of DT is to enable profile and growth of the semiconductor industry via cost-effective production of designs that fully exploit manufacturing capability. In the 2007 ITRS, the Design International Technology Working Group (DITWG) is responsible for the Design and Design Drivers chapters, along with models for clock frequency, feature density, and power dissipation in support of the Overall Roadmap Technology Characterization Specifics. DT challenges and needs are supported, as appropriate, by System Drivers. Readers of this chapter are encouraged to also review previous editions of the ITRS Design Report, which provide excellent and well-referenced summaries of DT needs.

The main message in 2007 remains—*Cost of design is the greatest threat to continuation of the semiconductor roadmap*. Cost determines whether differentiating value is best achieved in software or in hardware, on a programmable commodity platform or on a non-IC. Manufacturing semiconductor engineering (SME) costs are on the order of millions of dollars (mask set + probe card), design SME costs routinely reach tens of millions of dollars, with design efficiency being responsible for almost 50% of total manufacturing SME. Rapid technology change drives shorter product life cycles and makes time-to-market a critical issue for semiconductor customers. Manufacturing cycle times are increased as works with low uncertainty. Design and verification cycle times are measured in months or years, with high uncertainty. Without broader automation and electronic automation (EDA) for supplier solutions, the semiconductor innovation cycle stalls. ITRS estimates prior to 2010 have demonstrated a design productivity gap—the number of available innovations grows faster than the ability to successfully design them. Via investment in process technology (not in the dominated investment in design technology). The good news is that enabling progress in DT continues. Figure 17 shows that estimated design cost of the power-efficient system-on-chip (SoC) defined in the System Drivers chapter is near \$200 in 2007, versus around \$5000 for DT innovations between 1998 and 2005 not included (simple device are given in the Appendix). The bad news is that software cost accounts for 80% of embedded-systems development cost, we can't buy generic exponentially relative to manufacturing cost, verification engineers outnumber design engineers on management project teams, etc. Today, many design technology gaps are critical.



• ... Due August 31 !

2. Table file –
Excel

- Text tables can be in Word inside the Chapter

2. Potential Solutions charts file –
Excel or Visio

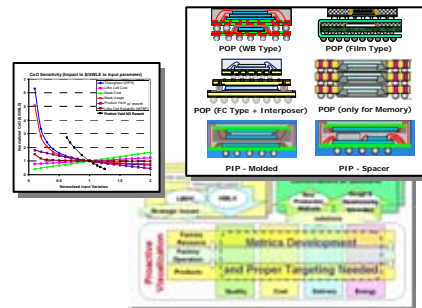
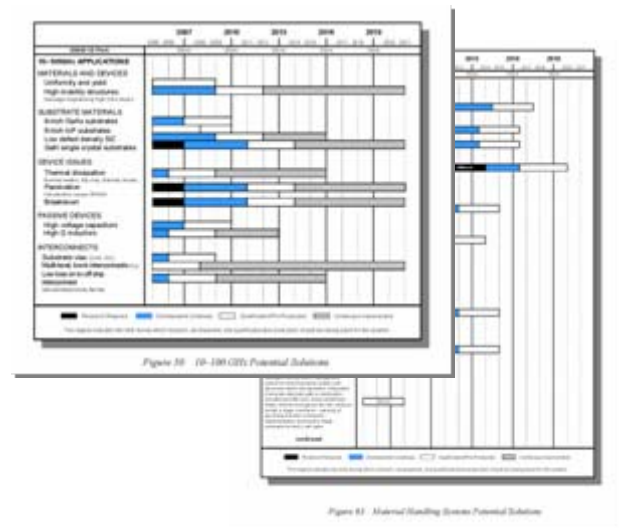
2. Figures file –
Powerpoint

The Final Stretch !

Table 17a: Emerging Technology Requirements - Interconnects

Table 17b: Emerging Technology Requirements - Interconnects

Legend:
 - Yellow: Requirements under development
 - Red: Requirements to be developed



The Final Stretch !

Other Activities after TWGs turn in chapter materials

- Editing and reformatting by editor begins to assemble the chapters for the entire ITRS
 - *Project Scope*
+900 pages, +200 tables, +100 figures, +500 citations
- **September 15 – Content is Frozen until 2008**
- Supplemental electronic files for links are due September 15
- October 31 – IRC approves roadmap
- November – prepare roadmap for release
- December 3-5 – ITRS Winter meeting in Japan

