INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Overall Roadmap Technology Characteristics

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TABLE OF CONTENTS

Overall Roadmap Technology Characteristics 1
Glossary 21

LIST OF TABLES

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years 1
Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term Years UPDATED 1
Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years 3
Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years UPDATED 3
Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years 4
Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years UPDATED 5
Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years UPDATED 6
Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED 7
Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years UPDATED 9
Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years UPDATED 10
Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years 11
Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years UPDATED 11
Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years UPDATED 12
Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years UPDATED 13
Table 4a Performance and Package Chips: Pads, Cost—Near-term Years UPDATED 14
Table 4b Performance and Package Chips: Pads, Cost—Long-term Years UPDATED 15
Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years 16
Table 4d Performance and Package Chips: Frequency, On-chip Wiring Levels—Long-term Years UPDATED 16
Table 5a Electrical Defects—Near-term Years 17
Table 5b Electrical Defects—Long-term Years UPDATED 17
Table 6a Power Supply and Power Dissipation—Near-term Years UPDATED 18
Table 6b Power Supply and Power Dissipation—Long-term Years UPDATED 18
Table 7a Cost—Near-term Years 19
Table 7b Cost—Long-term Years UPDATED 20

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

Link to the 2003 ITRS Executive Summary

ORTC TABLES

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
ASIC/Low Operating Power Printed Gate Length (nm) ††	**90**	**75**	**65**	**53**	**45**	**40**	**35**
ASIC/Low Operating Power Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term Years UPDATED

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
WAS	*DRAM ½ Pitch (nm)*	*45*		*35*	*32*		*25*	*22*		*18*
IS	*DRAM ½ Pitch (nm)*	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
WAS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**		**42**	**38**		**30**	**27**		**21**
IS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
WAS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**		**35**	**32**		**25**	**22**		**18**
IS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	*MPU Printed Gate Length (nm) ††*	**25**		**20**	**18**		**14**	**13**		**10**
IS	*MPU Printed Gate Length (nm) ††*	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**
WAS	*MPU Physical Gate Length (nm)*	**18**		**14**	**13**		**10**	**9**		**7**
IS	*MPU Physical Gate Length (nm)*	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
WAS	*ASIC/Low Operating Power Printed Gate Length (nm) ††*	**32**		**25**	**22**		**18**	**16**		**13**
IS	*ASIC/Low Operating Power Printed Gate Length (nm) ††*	**32**	**28**	**25**	**22**	**20**	**18**	**16**	**14**	**13**
WAS	*ASIC/Low Operating Power Physical Gate Length (nm)*	**22**		**18**	**16**		**13**	**11**		**9**
IS	*ASIC/Low Operating Power Physical Gate Length (nm)*	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**	**9**

Notes for Tables 1a and 1b:

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "physical" gate lengths may be reduced from the "as-printed" dimension. These "physical" gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

In addition, during the 2003 ITRS development, an attempt has been made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology node manufacturing in 2003. Since the metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance).

The IRC has decided that the best way to minimize confusion between the ITRS and individual company public announcements is to identify the ITRS table header node with the industry's most aggressive half-pitch targets, and to label these targets as hpXX (i.e., hp90, hp65, hp45, etc.). Currently the industry's most aggressive half pitch is the DRAM cell metal half-pitch.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Cell area factor [a]	**8**	**8**	**7.5**	**7**	**7**	**6**	**6**
Cell area [$Ca = af^2$] (mm^2)	**0.082**	**0.065**	**0.048**	**0.036**	**0.028**	**0.019**	**0.015**
Cell array area at production (% of chip size) §	**63.00%**	**63.00%**	**63.00%**	**63.00%**	**63.00%**	**63.00%**	**63.00%**
Generation at production §	**1G**	**1G**	**1G**	**2G**	**2G**	**4G**	**4G**
Functions per chip (Gbits)	**1.07**	**1.07**	**1.07**	**2.15**	**2.15**	**4.29**	**4.29**
Chip size at production (mm^2)§	**139**	**110**	**82**	**122**	**97**	**131**	**104**
Gbits/cm^2 at production §	**0.77**	**0.97**	**1.31**	**1.76**	**2.22**	**3.27**	**4.12**

Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
WAS	*DRAM ½ Pitch (nm)*	*45*		*35*	*32*		*25*	*22*		*18*
IS	*DRAM ½ Pitch (nm)*	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
WAS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**		**42**	**38**		**30**	**27**		**21**
IS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
WAS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**		**35**	**32**		**25**	**22**		**18**
IS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	*MPU Printed Gate Length (nm) ††*	**25**		**20**	**18**		**14**	**13**		**10**
IS	*MPU Printed Gate Length (nm) ††*	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**
WAS	*MPU Physical Gate Length (nm)*	**18**		**14**	**13**		**10**	**9**		**7**
IS	*MPU Physical Gate Length (nm)*	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
WAS	*Cell area factor [a]*	**6**		**6**	**6**		**6**	**5**		**5**
IS	*Cell area factor [a]*	**6**	**6**	**6**	**6**	**6**	**6**	**5**	**5**	**5**
WAS	*Cell area [$Ca = af^2$] (mm^2)*	**0.012**		**0.0077**	**0.0061**		**0.0038**	**0.0025**		**0.0016**
IS	*Cell area [$Ca = af^2$] (mm^2)*	**0.012**	**0.0096**	**0.0077**	**0.0061**	**0.005**	**0.0038**	**0.0025**	**0.002**	**0.0016**
WAS	*Cell array area at production (% of chip size) §*	**63.00%**		**63.00%**	**63.00%**		**63.00%**	**63.00%**		**63.00%**
IS	*Cell array area at production (% of chip size) §*	**63.00%**	**63.00%**	**63.00%**	**63.00%**	**63.00%**	**63.00%**	**63.00%**	**63.00%**	**63.00%**
WAS	*Generation at production §*	**4G**		**8G**	**8G**		**16g**	**32G**		**32G**
IS	*Generation at production §*	**4G**	**8G**	**8G**	**8G**	**16g**	**16g**	**32G**	**32G**	**32G**
WAS	*Functions per chip (Gbits)*	**4.29**		**8.59**	**8.59**		**17.18**	**34.36**		**34.36**
IS	*Functions per chip (Gbits)*	**4.29**	**8.59**	**8.59**	**8.59**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**
WAS	*Chip size at production (mm^2)§*	**83**		**104**	**83**		**104**	**138**		**87**
IS	*Chip size at production (mm^2)§*	**83**	**131**	**104**	**83**	**131**	**104**	**138**	**110**	**87**
WAS	*Gbits/cm^2 at production §*	**5.19**		**8.23**	**10.37**		**16.46**	**24.89**		**39.51**
IS	*Gbits/cm^2 at production §*	**5.19**	**6.53**	**8.23**	**10.37**	**13.07**	**16.46**	**24.89**	**31.36**	**39.51**

Notes for Tables 1c and 1d:
§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:
1999-2004/8×: 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.
DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:
1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).
InTER-generation chip size growth rate model target for Production-phase DRAMs is now "flat" at less than 140 mm^2, similar to the MPU model. This new flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Table 1c,d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63% , which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above).The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.
Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
DRAM ½ Pitch (nm)	**100**	**90**	**80**	**70**	**65**	**57**	**50**
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Cell area factor [a]	**8**	**8**	**7.5**	**7**	**7**	**6**	**6**
Cell area [$Ca = af^2$] (mm^2)	**0.082**	**0.065**	**0.048**	**0.036**	**0.028**	**0.019**	**0.015**
Cell array area at introduction (% of chip size) §	**72.23%**	**72.61%**	**72.95%**	**73.25%**	**73.52%**	**73.76%**	**73.97%**
Generation at introduction §	**4G**	**4G**	**8G**	**8G**	**16G**	**16G**	**16G**
Functions per chip (Gbits)	**4.29**	**4.29**	**8.59**	**8.59**	**17.18**	**17.18**	**17.18**
Chip size at introduction (mm^2) §	**485**	**383**	**568**	**419**	**662**	**449**	**356**
Gbits/cm^2 at introduction §	**0.88**	**1.12**	**1.51**	**2.05**	**2.59**	**3.82**	**4.83**

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	-	42	38	-	30	27	-	21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Cell area factor [a]	6	-	6	6	-	6	5	-	5
IS	Cell area factor [a]	6	6	6	6	6	6	5	5	5
WAS	Cell area [Ca = af2] (mm^2)	0.012	-	0.0077	0.0061	-	0.0038	0.0025	-	0.0016
IS	Cell area [Ca = af2] (mm^2)	0.0120	0.01	0.0077	0.0061	0.005	0.0038	0.0025	0.0020	0.0016
WAS	Cell array area at introduction (% of chip size) §	74.16%	-	74.47%	74.61%	-	74.83%	74.93%	-	75.09%
IS	Cell array area at introduction (% of chip size) §	74.16%	74.30%	74.47%	74.61%	74.70%	74.83%	74.93%	75.00%	75.09%
WAS	Generation at introduction §	32G	-	32G	64G	-	64G	128G	-	128G
IS	Generation at introduction §	32G	32G	32G	64G	64G	64G	128G	128G	128G
WAS	Functions per chip (Gbits)	34.36	-	34.36	68.72	-	68.7	137.4	-	137.4
IS	Functions per chip (Gbits)	34.36	34.36	34.36	68.72	68.72	68.7	137.4	137.4	137.4
WAS	Chip size at introduction (mm^2) §	563	-	353	560	-	351	464	-	292
IS	Chip size at introduction (mm^2) §	563	458	353	560	456	351	464	378	292
WAS	Gbits/cm2 at introduction §	5.2	-	8.2	10.4	-	16.5	24.9	-	39.5
IS	Gbits/cm2 at introduction §	6.10	7.71	9.73	12.3	15.5	19.6	29.6	37.3	47.1

Notes for Tables 1e and 1f:

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows:

1999-2004/8×: 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016–2018/5×. The delay of the "6" DRAM Cell design improvement Factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a 3-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1. at the Introduction phase, after the 16 Gbit generation/2007, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation/2003, the introduction rate is 4×/five years (2×/two–three years).

The original 2001 ITRS InTER-generation chip size growth rate was targeted to fit one chip per 572 mm^2 field at Introduction and two chips per 572 mm^2 field at Production. Due to the delay of the cell area factor reductions, Introduction chip sizes increased, but the new 704 mm^2 maximum affordable Litho field allows the Introduction chip to double bits per chip every two years through the 16 Gbit generation (660 mm^2/2007). Slowing the "Moore's Law" bits per chip of the Introduction-phase DRAM model to an average of 2× per 2.5 years enables the Introduction DRAMs to remain under the original 572 mm^2 affordable target after 2007. The InTRA-generation chip size shrink model remains at 0.5× every technology node in-between cell factor reductions, and eventually (ranging from five to six years), the Introduction-phase DRAMs shrink below the 140 mm^2 Production-phase chip size target.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	SRAM Cell (6-transistor) Area factor ++	120.3	117.8	115.6	113.7	111.9	110.4	109
	Logic Gate (4-transistor) Area factor ++	320	320	320	320	320	320	320
	SRAM Cell (6-transistor) Area efficiency ++	0.63	0.63	0.63	0.63	0.63	0.63	0.63
	Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50
ADD	SRAM Cell (6-transistor) Area ++	1.23	0.95	0.74	0.58	0.45	0.35	0.28
	SRAM Cell (6-transistor) Area w/overhead ++	2.0	1.5	1.2	0.93	0.73	0.57	0.45
ADD	Logic Gate (4-transistor) Area ++	3.27	2.59	2.06	1.63	1.30	1.03	0.82
	Logic Gate (4-transistor) Area w/overhead ++	6.5	5.2	4.1	3.3	2.6	2.1	1.6
	Transistor density SRAM (Mtransistors/cm^2)	305	393	504	646	827	1,057	1,348
	Transistor density logic (Mtransistors/cm^2)	61	77	97	122	154	194	245
	Generation at introduction *	--	p07c	--	--	p10c	--	--
WAS	Functions per chip at introduction (million transistors [Mtransistors])	180	226	285	360	453	571	719
IS	Functions per chip at introduction (million transistors [Mtransistors])	307	386	487	614	773	974	1227
	Chip size at introduction (mm^2) ‡	280	280	280	280	280	280	280
	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	110	138	174	219	276	348	438
	Generation at production *	--	p04c	--	--	p07c	--	--
	Functions per chip at production (million transistors [Mtransistors])	153	193	243	307	386	487	614
	Chip size at production (mm^2) §§	140	140	140	140	140	140	140
	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	110	138	174	219	276	348	438

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	SRAM Cell (6-transistor) Area factor ++	107.8		105.7	104.8		103.4	102.8		101.7
IS	SRAM Cell (6-transistor) Area factor ++	107.8	106.7	105.7	104.8	104.1	103.4	102.8	102.2	101.7
WAS	Logic Gate (4-transistor) Area factor ++	320		320	320		320	320		320
IS	Logic Gate (4-transistor) Area factor ++	320	320	320	320	320	320	320	320	320
WAS	SRAM Cell (6-transistor) Area efficiency ++	0.625		0.625	0.625		0.625	0.625		0.625
IS	SRAM Cell (6-transistor) Area efficiency ++	0.625	0.625	0.625	0.625	0.625	0.625	0.625	0.625	0.625
WAS	Logic Gate (4-transistor) Area efficiency ++	0.5		0.5	0.5		0.5	0.5		0.5
IS	Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
ADD	SRAM Cell (6-transistor) Area	0.22	0.17	0.13	0.11	0.084	0.066	0.052	0.041	0.032
WAS	SRAM Cell (6-transistor) Area w/overhead ++	0.22		0.13	0.11		0.066	0.052		0.032
IS	SRAM Cell (6-transistor) Area w/overhead ++	0.35	0.27	0.22	0.17	0.13	0.106	0.083	0.07	0.052
ADD	Logic Gate (4-transistor) Area	0.65	0.51	0.41	0.32	0.26	0.20	0.16	0.13	0.10
WAS	Logic Gate (4-transistor) Area w/overhead ++	1.3		0.82	0.65		0.41	0.32		0.2
IS	Logic Gate (4-transistor) Area w/overhead ++	1.30	1.03	0.82	0.65	0.51	0.41	0.32	0.26	0.20
WAS	Transistor density SRAM (Mtransistors/cm^2)	1,718		2,781	3,532		5,687	7,208		11,558
IS	Transistor density SRAM (Mtransistors/cm^2)	1,718	2,187	2,781	3,532	4,484	5,687	7,208	9,130	11,558
WAS	Transistor density logic (Mtransistors/cm^2)	309		490	617		980	1,235		1,960
IS	Transistor density logic (Mtransistors/cm^2)	309	389	490	617	778	980	1,235	1,555	1,960

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED (continued)

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
WAS	*DRAM ½ Pitch (nm)*	45		35	32		25	22		18
IS	*DRAM ½ Pitch (nm)*	45	40	35	32	28	25	22	20	18
WAS	*Generation at introduction **	p13c		--	p16c		--	p19c		--
IS	*Generation at introduction **	p13c	--	--	p16c	--	--	p19c	--	--
WAS	*Functions per chip at introduction (million transistors [Mtransistors])*	1,546		2,454	3,092		4,908	6,184		9,816
IS	*Functions per chip at introduction (million transistors [Mtransistors])*	1,546	1,948	2,454	3,092	3,896	4,908	6,184	7,791	9,816
WAS	*Chip size at introduction (mm^2) ‡*	280		280	280		280	280		280
IS	*Chip size at introduction (mm^2) ‡*	280	280	280	280	280	280	280	280	280
WAS	*Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡*	552		876	1,104		1,753	2,209		3,506
IS	*Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡*	552	696	876	1,104	1,391	1,753	2,209	2,783	3,506
WAS	*Generation at production **	p10c		--	p13c		--	p16c		--
IS	*Generation at production **	p10c	--	--	p13c	--	--	p16c	--	--
WAS	*Functions per chip at production (million transistors [Mtransistors])*	773		1,227	1,546		2,454	3,092		4,908
IS	*Functions per chip at production (million transistors [Mtransistors])*	773	974	1,227	1,546	1,948	2,454	3,092	3,896	4,908
WAS	*Chip size at production (mm^2) §§*	140		140	140		140	140		140
IS	*Chip size at production (mm^2) §§*	140	140	140	140	140	140	140	140	140
WAS	*Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡*	552		876	1,104		1,753	2,209		3,506
IS	*Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡*	552	696	876	1,104	1,391	1,753	2,209	2,783	3,506

Notes for Tables 1g and 1h:

++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p01c, was introduced in 1999, but not ramped into volume production until 2001; similarly, the p04c, is introduced in 2001, but is targeted for volume production in 2004.*

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/1999), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years
UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
	MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
	MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
	Logic (Low-volume Microprocessor) High-performance ‡							
WAS	Generation at production **	**p03h**	**--**	**p05h**	**--**	**p07h**	**--**	**p09h**
IS	Generation at production **	**--**	**p04h**	**--**	**--**	**p07h**	**--**	**--**
	Functions per chip (million transistors)	**439**	**553**	**697**	**878**	**1,106**	**1,393**	**1,756**
	Chip size at production (mm^2) §§	**310**	**310**	**310**	**310**	**310**	**310**	**310**
	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	**142**	**178**	**225**	**283**	**357**	**449**	**566**
	ASIC							
	ASIC usable Mtransistors/cm^2 (auto layout)	**142**	**178**	**225**	**283**	**357**	**449**	**566**
	ASIC max chip size at production (mm^2) (maximum lithographic field size)	**572**	**572**	**572**	**572**	**572**	**572**	**572**
	ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**810**	**1,020**	**1,286**	**1,620**	**2,041**	**2,571**	**3,239**

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years
UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Logic (Low-volume Microprocessor) High-performance ‡									
WAS	Generation at production **	--		--	p13h		p15h	--		--
IS	Generation at production **	p10h	--	--	p13h	--	--	p16h	--	--
WAS	Functions per chip (million transistors)	2,212		3,511	4,424		7,022	8,848		14,045
IS	Functions per chip (million transistors)	2,212	2,787	3,511	4,424	5,574	7,022	8,848	11,147	14,045
WAS	Chip size at production (mm^2) §§	310		310	310		310	310		310
IS	Chip size at production (mm^2) §§	310	310	310	310	310	310	310	310	310
WAS	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	714		1,133	1,427		2,265	2,854		4,531
IS	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	714	899	1,133	1,427	1,798	2,265	2,854	3,596	4,531
	ASIC									
WAS	ASIC usable Mtransistors/cm^2 (auto layout)	714		1,133	1,427		2,265	2,854		4,531
IS	ASIC usable Mtransistors/cm^2 (auto layout)	714	899	1,133	1,427	1,798	2,265	2,854	3,596	4,531
WAS	ASIC maximum chip size at production (mm^2) (maximum lithographic field size)	572		572	572		572	572		572
IS	ASIC maximum chip size at production (mm^2) (maximum lithographic field size)	572	572	572	572	572	572	572	572	572
WAS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081		6,479	8,163		12,958	16,326		25,915
IS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081	5,142	6,479	8,163	10,284	12,958	16,326	20,569	25,915

Notes for Tables 1i and 1j:
*** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001, the p03h in2003, and so forth.*
‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.
§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.
Refer to the Glossary for definitions

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Lithography Field Size							
Lithography Field Size—area (mm^2)	**704**	**704**	**704**	**704**	**704**	**704**	**704**
Lithographic field size—length (mm)	**32**	**32**	**32**	**32**	**32**	**32**	**32**
Lithographic field size—width (mm)	**22**	**22**	**22**	**22**	**22**	**22**	**22**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300**	**300**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**54**		**42**	**38**		**30**	**27**		**21**
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**45**		**35**	**32**		**25**	**22**		**18**
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	MPU Printed Gate Length (nm) ††	**25**		**20**	**18**		**14**	**13**		**10**
IS	MPU Printed Gate Length (nm) ††	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**
WAS	MPU Physical Gate Length (nm)	**18**		**14**	**13**		**10**	**9**		**7**
IS	MPU Physical Gate Length (nm)	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
	Lithography Field Size									
WAS	Lithography Field Size—area (mm^2)	**704**		**704**	**704**		**704**	**704**		**704**
IS	Lithography Field Size—area (mm^2)	**704**	**704**	**704**	**704**	**704**	**704**	**704**	**704**	**704**
WAS	Lithographic field size—length (mm)	**32**		**32**	**32**		**32**	**32**		**32**
IS	Lithographic field size—length (mm)	**32**	**32**	**32**	**32**	**32**	**32**	**32**	**32**	**32**
WAS	Lithographic field size—width (mm)	**22**		**22**	**22**		**22**	**22**		**22**
IS	Lithographic field size—width (mm)	**22**	**22**	**22**	**22**	**22**	**22**	**22**	**22**	**22**
	Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)									
WAS	Bulk or epitaxial or SOI wafer	**300**		**450**	**450**		**450**	**450**		**450**
IS	Bulk or epitaxial or SOI wafer	**300**	**300**	**450**	**450**	**450**	**450**	**450**	**450**	**450**

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
	MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
	MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
	Number of Chip I/Os (Number of Total Chip Pads)—Maximum							
WAS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,328	3,584
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,109	1,195
IS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,024	1,024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,219	2,389
IS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,048	2,048
WAS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,600	4,800
IS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,400	4,600
WAS	Signal I/O pads—ASIC high-performance	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Signal I/O pads—ASIC high-performance	1700	1800	2000	2100	2200	2200	2300
WAS	Power and ground pads—ASIC high-performance (½ of total pads)	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Power and ground pads—ASIC high-performance (½ of total pads)	1700	1800	2000	2100	2200	2200	2300
	Number of Total Package Pins—Maximum [1]							
WAS	Microprocessor/controller, cost-performance	500–1,452	500–1,600	550–1,760	550–1,936	600–2,140	660–2,354	720–2,568
IS	Microprocessor/controller, cost-performance	--	500–1600	550–1760	550–1936	600–2140	600–2400	660–2800
WAS	Microprocessor/controller, high-performance	1,452	1,600	1,760	1,936	2,140	2,354	2,568
IS	Microprocessor/controller, high-performance	--	1,600	1,760	1,936	2,140	2,400	2,800
WAS	ASIC (high-performance)	2,400	3,000	3,400	3,800	4,000	4,400	4,600
IS	ASIC (high-performance)	--	3,000	3,400	3,800	4,000	4,400	4,600

Notes for Tables 3a and 3b:
[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost.
The highest pin count applications will as a result use larger pitches and larger package sizes.
The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4.

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Number of Chip I/Os (Number of Total Chip Pads)—Maximum									
WAS	Total pads—MPU	3,840		4,096	4,224		4,352	4,416		4,544
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,280		1,365	1,408		1,451	1,472		1,515
IS	Signal I/O—MPU (1/3 of total pads)	1024	1024	1024	1024	1024	1024	1024	1024	1024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,560		2,731	2,816		2,901	2,944		3,029
IS	Power and ground pads—MPU (2/3 of total pads)	2048	2048	2048	2048	2048	2048	2048	2048	2048
WAS	Total pads—ASIC high-performance	4,800		5,200	5,400		5,800	6,000		6,400
IS	Total pads—ASIC high-performance	4,800	4,800	5,000	5,400	5,400	5,600	6,000	6,000	6,200
WAS	Signal I/O pads—ASIC high-performance	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Signal I/O pads—ASIC high-performance	2,400	2,400	2,500	2,700	2,700	2,800	3,000	3,000	3,100
WAS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	2,400	2,500	2,700	2,700	2,800	3,000	3,000	3,100
	Number of Total Package Pins—Maximum [1]									
	Microprocessor/controller, cost-performance	780–2,782		936–3,338	1014–3,616		1217–4,340	1318–4,702		1521–5,426
	Microprocessor/controller, high-performance	2,782		3,338	3,616		4,340	4,702		5,426
	ASIC (high-performance)	4,009		4,810	5,335		6,402	7,042		8,450

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
	MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
	MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
	Chip Pad Pitch (micron)							
WAS	Pad pitch—ball bond	**40**	**35**	**30**	**25**	**25**	**20**	**20**
IS	Pad pitch—ball bond	**40**	**40**	**35**	**35**	**30**	**30**	**25**
WAS	Pad pitch—wedge bond	**30**	**25**	**20**	**20**	**20**	**20**	**20**
IS	Pad pitch—wedge bond	**30**	**30**	**30**	**25**	**25**	**25**	**20**
	Pad Pitch—area array flip-chip (cost-performance, high-performance)	**150**	**150**	**130**	**130**	**120**	**110**	**100**
	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	**60**	**60**	**40**	**40**	**30**	**30**	**20**
	Cost-Per-Pin							
	Package cost (cents/pin) (cost-performance)—minimum-maximum	**.75–1.30**	**.71–1.24**	**.67–1.17**	**.64–1.11**	**.61–1.05**	**.58–1.00**	**.55–.96**
WAS	Package cost (cents/pin) (Memory)—minimum–maximum	**0.30–0.56**	**0.29–.53**	**.27–.50**	**,26–.48**	**,25–.45**	**.23–.43**	**.22–.41**
IS	Package cost (cents/pin) (Memory)—minimum–maximum	**0.30–0.56**	**0.30–.53**	**.27–.50**	**.26–.48**	**.25–.45**	**.23–.43**	**.22–.41**

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years UPDATED

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
WAS	*DRAM ½ Pitch (nm)*	*45*		*35*	*32*		*25*	*22*		*18*
IS	*DRAM ½ Pitch (nm)*	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
WAS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**		**42**	**38**		**30**	**27**		**21**
IS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
WAS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**		**35**	**32**		**25**	**22**		**18**
IS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	*MPU Printed Gate Length (nm) ††*	**25**		**20**	**18**		**14**	**13**		**10**
IS	*MPU Printed Gate Length (nm) ††*	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**
WAS	*MPU Physical Gate Length (nm)*	**18**		**14**	**13**		**10**	**9**		**7**
IS	*MPU Physical Gate Length (nm)*	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
	Chip Pad Pitch (micron)									
WAS	*Pad pitch—ball bond*	**20**		**20**	**20**		**20**	**20**		**20**
IS	*Pad pitch—ball bond*	**25**	**25**	**25**	**25**	**25**	**25**	**25**	**25**	**25**
WAS	*Pad Pitch—wedge bond*	**20**		**20**	**20**		**20**	**20**		**20**
IS	*Pad Pitch—wedge bond*	**20**	**20**	**20**	**20**	**20**	**20**	**20**	**20**	**20**
WAS	*Pad Pitch—area array flip-chip (cost-performance, high-performance)*	**100**		**90**	**90**		**80**	**80**		**70**
IS	*Pad Pitch—area array flip-chip (cost-performance, high-performance)*	**90**	**--**	**90**		**--**	**80**	**--**	**--**	**70**
WAS	*Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)*	**20**		**20**	**20**		**15**	**15**		**15**
IS	*Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)*	**20**	**20**	**20**	**20**	**--**	**15**	**15**	**15**	**15**
	Cost-Per-Pin									
	Package cost (cents/pin) (cost-performance)— minimum–maximum	**0.52–0.94**		**0.5–.86**	**0.5–.77**		**0.5–0.69**	**0.5–0.65**		**0.5–0.59**
	Package cost (cents/pin) (Memory)—minimum–maximum	**.22–.41**		**0.22–0.36**	**0.22–0.35**		**0.22–0.31**	**0.22–0.29**		**0.22–0.27**

Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Chip Frequency (MHz)							
On-chip local clock	**2,976**	**4,171**	**5,204**	**6,783**	**9,285**	**10,972**	**12,369**
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	**2,000**	**2,500**	**3,125**	**3,906**	**4,883**	**6,103**	**7,629**
Maximum number wiring levels—maximum	**13**	**14**	**15**	**15**	**15**	**16**	**16**
Maximum number wiring levels—minimum	**9**	**10**	**11**	**11**	**11**	**12**	**12**

Table 4d Performance and Package Chips: Frequency, On-chip Wiring Levels—Long-term Years
UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**54**		**42**	**38**		**30**	**27**		**21**
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**45**	-	**35**	**32**	-	**25**	**22**	-	**18**
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	MPU Printed Gate Length (nm) ††	**25**	-	**20**	**18**	-	**14**	**13**	-	**10**
IS	MPU Printed Gate Length (nm) ††	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**
WAS	MPU Physical Gate Length (nm)	**18**	-	**14**	**13**	-	**10**	**9**	-	**7**
IS	MPU Physical Gate Length (nm)	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
	Chip Frequency (MHz)									
	On-chip local clock	**15,079**		**20,065**	**22,980**		**33,403**	**39,683**		**53,207**
	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	**9,536**		**14,901**	**18,626**		**29,103**	**36,379**		**56,843**
WAS	Maximum number wiring levels—maximum	**16**		**16**	**16**		**17**	**18**		**18**
IS	Maximum number wiring levels—maximum	**16**	**16**	**16**	**16**	**17**	**17**	**18**	**18**	**18**
WAS	Maximum number wiring levels—minimum	**12**		**12**	**12**	-	**13**	**14**	-	**14**
IS	Maximum number wiring levels—minimum	**12**	**12**	**12**	**12**	**13**	**13**	**14**	**14**	**14**

Note for Tables 4c and 4d:
[1] The off-chip frequency is expected to increase for a small number of high-speed pins that will be used in combination with a large number of lower speed pins
[2] In 2001, high-speed serial communications transceiver devices are achieving chip-board frequencies of 3.125 GHz using CMOS, and 10 GHz using SiGe. In 2002 it is expected that 10 GHz transceivers will be fabricated using CMOS. 40 GHz SiGe devices are expected in 2003. The roadmap for higher levels of integration with wider bus widths, is shown in the High Frequency Serial Communications section in the Test chapter.
[3] The minimum number of wiring levels represents the interconnect metal levels, and the maximum number of interconnect wiring levels includes the Minimum number of wiring levels plus additional optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

Table 5a Electrical Defects—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**2,216**	**2,791**	**3,751**	**2,532**	**3,190**	**2,345**	**2,954**
MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	**1,395**	**1,395**	**1,395**	**1,395**	**1,395**	**1,395**	**1,395**
# Mask Levels—MPU	**29**	**31**	**33**	**33**	**33**	**35**	**35**
# Mask Levels—DRAM	**24**	**24**	**24**	**24**	**24**	**24**	**24**

Table 5b Electrical Defects—Long-term Years UPDATED

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
WAS	*DRAM ½ Pitch (nm)*	*45*		*35*	*32*		*25*	*22*		*18*
IS	*DRAM ½ Pitch (nm)*	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
WAS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**		**42**	**38**		**30**	**27**		**21**
IS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
WAS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**		**35**	**32**		**25**	**22**		**18**
IS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	*MPU Printed Gate Length (nm) ††*	**25**		**20**	**18**		**14**	**13**		**10**
IS	*MPU Printed Gate Length (nm) ††*	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**
WAS	*MPU Physical Gate Length (nm)*	**18**		**14**	**13**		**10**	**9**		**7**
IS	*MPU Physical Gate Length (nm)*	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
WAS	*DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §*	**3,722**		**2,954**	**3,722**		**2,954**	**2,233**		**3,545**
IS	*DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §*	**3,722**	**2,353**	**2,954**	**3,722**	**2,353**	**2,954**	**2,233**	**2,803**	**3,545**
WAS	*MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§*	**1,395**		**1,395**	**1,395**		**1,395**	**1,395**		**1,395**
IS	*MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§*	**1,395**	**1,395**	**1,395**	**1,395**	**1,395**	**1,395**	**1,395**	**1,395**	**1,395**
WAS	*# Mask Levels—MPU*	**35**		**35**	**35**		**37**	**39**		**39**
IS	*# Mask Levels—MPU*	**35**	**35**	**35**	**35**	**37**	**37**	**39**	**39**	**39**
WAS	*# Mask Levels—DRAM*	**26**		**26**	**26**		**26**	**26**		**26**
IS	*# Mask Levels—DRAM*	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**

Notes for Tables 5a and 5b:
D_0 — defect density
§ DRAM Model—Cell factor (design/process improvement) targets are as follows:
1999–2004/8×: 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2×.
DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:
1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

Table 6a Power Supply and Power Dissipation—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
	MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
	MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
	Power Supply Voltage (V)							
	V_{dd} (high-performance)	**1.2**	**1.2**	**1.1**	**1.1**	**1.1**	**1**	**1**
	V_{dd} (Low Operating Power, high V_{dd} transistors)	**1**	**0.9**	**0.9**	**0.9**	**0.8**	**0.8**	**0.8**
	Allowable Maximum Power [1]							
WAS	High-performance with heatsink (W)	**149**	**158**	**167**	**180**	**189**	**200**	**210**
IS	High-performance with heatsink (W)	**149**	**158**	**167**	**180**	**189**	**198**	**198**
	Cost-performance (W)	**80**	**84**	**91**	**98**	**104**	**109**	**114**
	Battery (W)—(low-cost/hand-held)	**2.1**	**2.2**	**2.3**	**2.4**	**2.5**	**2.6**	**2.7**

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 6b Power Supply and Power Dissipation—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**54**		**42**	**38**		**30**	**27**		**21**
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**45**		**35**	**32**		**25**	**22**		**18**
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	MPU Printed Gate Length (nm) ††	**25**		**20**	**18**		**14**	**13**		**10**
IS	MPU Printed Gate Length (nm) ††	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**
WAS	MPU Physical Gate Length (nm)	**18**		**14**	**13**		**10**	**9**		**7**
IS	MPU Physical Gate Length (nm)	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
	Power Supply Voltage (V)									
WAS	Vdd (high-performance)	**1**		**0.9**	**0.9**		**0.8**	**0.8**		**0.7**
IS	Vdd (high-performance)	**1**	**1**	**0.9**	**0.9**	**0.9**	**0.8**	**0.8**	**0.7**	**0.7**
WAS	Vdd (Low Operating Power, high Vdd transistors)	**0.7**		**0.7**	**0.6**		**0.6**	**0.5**		**0.5**
IS	Vdd (Low Operating Power, high Vdd transistors)	**0.7**	**0.7**	**0.7**	**0.6**	**0.6**	**0.6**	**0.5**	**0.5**	**0.5**
	Allowable Maximum Power [1]									
WAS	High-performance with heatsink (W)	**218**		**240**	**251**		**270**	**288**		**300**
IS	High-performance with heatsink (W)	**198**	**198**	**198**	**198**	**198**	**198**	**198**	**198**	**198**
	Cost-performance (W)	**120**		**131**	**138**		**148**	**158**		**168**
	Battery (W)—(hand-held)	**2.8**		**3**	**3**		**3**	**3**		**3**

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 7a Cost—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**10.5**	**7.4**	**5.3**	**3.7**	**2.6**	**1.9**	**1.3**
DRAM cost/bit at (packaged microcents) at production §	**3.8**	**2.7**	**1.9**	**1.4**	**0.96**	**0.7**	**0.5**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**88**	**62**	**44**	**31**	**22**	**15.6**	**11.0**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**53**	**38**	**27**	**19**	**13.3**	**9.4**	**6.7**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**49**	**34**	**24**	**17**	**12**	**8.6**	**6.1**
Cost-Per-Pin							
Test Cost							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	**1**	**1**	**1**	**1**	**1**	**1**	**2**

Notes for Tables 7a and 7b:

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—Cell factor (design/process improvement) targets are as follows:

1999–2004/8×: 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4× /five years (2×/two–three years).

InTER-generation chip size growth rate model target for Production-phase DRAMs is now "flat" at less than 140 mm^2, similar to the MPU model. This new flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Tables 1c and d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63%, which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above). The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 7b Cost—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Affordable Cost per Function ++									
WAS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93		0.46	0.33		0.16	0.12		0.06
IS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93	0.66	0.46	0.33	0.23	0.16	0.12	0.08	0.06
WAS	DRAM cost/bit (packaged microcents) at production §	0.34		0.17	0.12		0.06	0.042		0.021
IS	DRAM cost/bit (packaged microcents) at production §	0.34	0.24	0.17	0.12	0.08	0.06	0.04	0.03	0.02
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78		3.89	2.75		1.38	0.97		0.49
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78	5.50	3.89	2.75	1.94	1.38	0.97	0.69	0.49
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71		2.35	1.66		0.83	0.59		0.29
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71	3.33	2.35	1.66	1.18	0.83	0.59	0.42	0.29
WAS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.305		2.15	1.52		0.76	0.54		0.27
IS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.30	3.04	2.15	1.52	1.08	0.76	0.54	0.38	0.27
	Cost-Per-Pin									
	Test Cost									
WAS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4		4	4		4	4		4
IS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4	4	4	4	4	4	4	4	4
WAS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	2		2	3		3	4		4
IS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	2	2	2	3	3	3	4	4	4

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

Technology Node—The minimum half-pitch of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated circuits and is selected to define an ITRS Technology Node. For each Node, this defining metal half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other parameters are also important for characterizing IC technology. For example, in the case of microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. Each technology node step represents the creation of significant technology progress in metal half-pitch — approximately 70% of the preceding node, 50% of two preceding nodes.

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

An official *2003 ITRS* metal half-pitch node indicator, "hpXX," has been added to differentiate the ITRS definition from commercial technology generation numbers .

Moore's Law—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore's Law, there is a historically-based "corollary" to the "law," which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the *2003 ITRS*, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1Mbytes/2001). Logic functionality and L2 cache typically double every three-year generation.

High-performance MPU—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25Mt cores in 2001) with a large (example 4Mbyte/2001) level-two (L2) SRAM. Logic functionality and L2 cache typically double every three-year technology generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology-node scaling (.7× linear, .5× area) is every three years, an additional device/process design improvement of .8× per two years must be achieved. This requirement represents a design-related (cell-area-factor) area-reduction improvement of at least -11% per year, and this design-related productivity improvement is in addition to the basic lithography-based area reduction of -21% per year (three-year node cycle).

The present *2003 ITRS* consensus target for the rate of increase of DRAM bits/chip has increased from 2× bits/chip every two years to 2×/chip every two and half years average. This slower bits/chip growth is required due to the new consensus *2003 ITRS* forecast of cell-area-factor improvement of only negative 4–6% per year on average rather than the *2001 ITRS* target of -7% per year average. This results in an average DRAM inTER-generation approximately flat chip-size growth. Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the *2003 ITRS* MPU inTER-generation functionality model target is 2× transistors/chip every technology node, in order maintain a flat chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The *2003 ITRS* consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The *ITRS* targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every four years at the leading-edge process technology node, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM, versus *ITRS* 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every two years (every technology node, in the case of MPUs). In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturer begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume

production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready 12–24 months prior to Production Ramp “Time Zero” [see Figure 2 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1Gb/production, 4G/introduction, plus 512Mb/256Mb/128Mb/64Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the *ITRS* consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the *2003 ITRS*, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified *ITRS*-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 1999: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.37e-6 mm^2/bit = 397 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, 1.6×1.6=2.5, etc.).

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density

calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

Chip and Package—Physical and Electrical Attributes

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

Chip Frequency (MHz)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

Other Attributes

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

Fabrication Attributes and Methods

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

Maximum Substrate Diameter (mm)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The *ITRS* timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.