YIELD ENHANCEMENT

Table 88 Yield Enhancement Difficult Challenges

Difficult Challenge ≥ 65 nm, Through 2007	*Summary of Issues*
Develop and Validate Systematic Yield Models—Process induced defects, equipment generated particles, product/processing measurements, and design/layout sensitivities have to be correlated to yield.	Correlate process-induced defects (PID), particles per wafer pass (PMP), product inspections, and *in situ* measurements. Develop parametric and process-to-design mismatch yield-loss models. Address sampling and statistical issues with ultra-small populations. Increase Yield Model accuracy.
High Aspect Ratio Inspection—High-speed cost-effective tools must be developed that rapidly detect defects associated with high-aspect-ratio contacts/vias/trenches, and particularly defects near/at the bottom of these features.	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
Defect/Fault Sourcing for Rapid Yield Learning—Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test and WIP data must be developed to enable rapid root cause analysis of yield limiting conditions.	Circuit complexity grows exponentially and the ability to rapidly isolate failures on non-arrayed chips is needed. Automated data/image mining and reduction algorithms must be developed to source defects from multiple data sources (facility, design, process and test.)
Correlation of Impurity Level to Yield—Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product.	Establish an employment methodology for each material type. Define a standard test for yield/parametric effect.
Difficult Challenge < 65 nm, Beyond 2007	*Summary of Issues*
Develop Yield Models that Include New Materials and Integration—Models must comprehend greater parametric sensitivities, complex integration issues, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology nodes. Address complex integration issues. Model ultra-thin film integrity issues. Improve scaling methods for front-end processes including increased transistor packing density.
D*efect Detection*—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size may not exist.
Non-visual Defect Sourcing and Design for Manufacture and Test—Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected. Also, IC designs must be optimized for a given process capability and must be testable/diagnosable.	Many defects that cause electrical faults are not detectable inline. Tools are needed that enable design to process matching for optimum yields. Also, testability/diagnose-ability must be designed into the IC for rapid electrical failure sourcing.
Precursors for New Materials—Required purity levels for delivered dielectric pre-cursors are not known or well understood.	Establish methodology for establishing purity standards for new dielectric pre-cursors.

Table 89 Defect Budget Technology Requirement Assumptions

	Product	MPU	DRAM
	Yield Ramp Phase	Volume Production	Volume Production
	$Y_{OVERALL}$	**75%**	**85%**
	Y_{RANDOM}	**83%**	**89.50%**
	$Y_{SYSTEMATIC}$	**90%**	**95%**
Was	Cluster Parameter	**5**	**5**
Is	Cluster Parameter [A]	**5**	**5**

Add Notes for Table 89:

It is the consensus of the Yield Enhancement ITWG members that the cluster parameter of 5 as indicated in Table 89 should be changed to a value of 2 for defect budget calculations. This issue will be addressed in the 2003 revision of the Yield Enhancement chapter of the ITRS.

Table 90 Yield Model and Defect Budget MPU Technology Requirements

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	*45*	*32*	*22*
MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	*50*	*35*	*25*
MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	*25*	*18*	*13*
MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	*18*	*13*	*9*
MPU										
MPU ½ metal one Pitch (nm) [A]	**150**	**130**	**107**	**90**	**80**	**70**	**65**	**45**	**32**	**22**
Critical Defect Size (nm)	**75**	**65**	**54**	**45**	**40**	**35**	**33**	**23**	**16**	**11**
Chip Size (mm^2) [B]	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Overall Electrical D_0 (faults/m^2) at critical defect size or greater [C]	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**	**2115**
Random D_0 (faults/m^2) [D]	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**	**1356**
# Mask Levels [E]	**25**	**25**	**25**	**25**	**25**	**27**	**27**	**27**	**29**	**29**
Random Faults/Mask	**54**	**54**	**54**	**54**	**54**	**50**	**50**	**50**	**47**	**47**
MPU Random Particles per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type scaled to 75nm critical defect size or greater										
CMP Clean	**448**	**337**	**228**	**161**	**127**	**90**	**78**	**37**	**18**	**8**
CMP Insulator	**1084**	**814**	**552**	**390**	**308**	**219**	**189**	**90**	**43**	**20**
CMP Metal	**1225**	**920**	**623**	**441**	**348**	**247**	**213**	**102**	**48**	**23**
Coat/Develop/Bake	**196**	**147**	**100**	**70**	**56**	**39**	**34**	**16**	**8**	**4**
CVD Insulator	**963**	**772**	**523**	**370**	**292**	**207**	**179**	**86**	**40**	**19**
CVD Oxide Mask	**1267**	**950**	**644**	**455**	**360**	**255**	**220**	**105**	**50**	**23**
Dielectric Track	**308**	**232**	**157**	**111**	**88**	**62**	**54**	**26**	**12**	**6**
Furnace CVD	**549**	**412**	**279**	**198**	**156**	**111**	**95**	**46**	**22**	**10**
Furnace Fast Ramp	**497**	**373**	**253**	**179**	**141**	**100**	**86**	**41**	**19**	**9**
Furnace Oxide/Anneal	**321**	**241**	**164**	**116**	**91**	**65**	**56**	**27**	**13**	**6**
Implant High Current	**430**	**323**	**219**	**155**	**122**	**87**	**75**	**36**	**17**	**8**
Implant Low/Med Current	**392**	**295**	**200**	**141**	**112**	**79**	**68**	**33**	**15**	**7**
Inspect PLY	**400**	**300**	**203**	**144**	**114**	**81**	**70**	**33**	**16**	**7**
Inspect Visual	**429**	**323**	**219**	**155**	**122**	**87**	**75**	**36**	**17**	**8**
Litho Cell	**332**	**250**	**169**	**120**	**95**	**67**	**58**	**28**	**13**	**6**
Litho Stepper	**315**	**237**	**160**	**113**	**90**	**64**	**55**	**26**	**12**	**6**
Measure CD	**374**	**281**	**190**	**135**	**106**	**75**	**65**	**31**	**15**	**7**
Measure Film	**321**	**241**	**164**	**116**	**91**	**65**	**56**	**27**	**13**	**6**
Measure Overlay	**298**	**224**	**152**	**107**	**85**	**60**	**52**	**25**	**12**	**6**
Metal CVD	**585**	**439**	**298**	**211**	**166**	**118**	**102**	**49**	**23**	**11**
Metal Electroplate	**302**	**227**	**154**	**109**	**86**	**61**	**52**	**25**	**12**	**6**
Metal Etch	**1300**	**976**	**661**	**468**	**370**	**262**	**226**	**108**	**51**	**24**
Metal PVD	**667**	**501**	**339**	**240**	**190**	**135**	**116**	**56**	**26**	**12**
Plasma Etch	**1183**	**889**	**602**	**426**	**336**	**239**	**206**	**99**	**46**	**22**
Plasma Strip	**547**	**411**	**278**	**197**	**156**	**110**	**95**	**46**	**21**	**10**
RTP CVD	**357**	**268**	**181**	**128**	**101**	**72**	**62**	**30**	**14**	**7**
RTP Oxide/Anneal	**234**	**175**	**119**	**84**	**66**	**47**	**41**	**19**	**9**	**4**
Test	**91**	**69**	**47**	**33**	**26**	**18**	**16**	**8**	**4**	**2**
Vapor Phase Clean	**822**	**617**	**418**	**296**	**234**	**166**	**143**	**68**	**32**	**15**
Wafer Handling	**37**	**28**	**19**	**13**	**10**	**7**	**6**	**3**	**1**	**1**
Wet Bench	**535**	**402**	**272**	**192**	**152**	**108**	**93**	**45**	**21**	**10**

White–Manufacturable Solutions Exist, and Are Being Optimized	⬜
Yellow–Manufacturable Solutions are Known	🟨
Red–Manufacturable Solutions are NOT Known	🟥

Notes for Table 90:

Was	*[A] As defined in the ORTC Table 1a*
Is	*[A] As defined in the ORTC Table 1a****+1b***
Was	*[B] As defined in the ORTC Table 2a*
Is	*[B] As defined in the ORTC Table* ***1g+1h***
Was	*[C] As defined in the ORTC Table 5a)*
Is	***[C] Based on assumption of 75% overall volume production yield.***
Was	*[D] Based on assumption of 89.5% Random Defect Limited Yield (RDLY*
Is	***[D] As defined in the ORTC Table 5a+5b. Based on assumption of 83% Random Defect Limited Yield (RDLY).***
Was	*[E] As defined in the ORTC Table 5a*
Is	*[E] As defined in the ORTC Table 5a****+5b***

Table 91 Yield Model and Defect Budget DRAM Technology Requirements

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	*18*	*13*	*9*
	DRAM										
	DRAM ½ Pitch (nm) [A]	**130**	**115**	**100**	**90**	**80**	**70**	**65**	**45**	**32**	**22**
	Critical Defect Size (nm)	**65**	**58**	**50**	**45**	**40**	**35**	**33**	**23**	**16**	**11**
	Chip Size (mm^2) [B]	**127**	**100**	**118**	**93**	**147**	**116**	**183**	**181**	**240**	**238**
Was	*Cell Array Area (%) @ Production*	**55%**	**55%**	**56%**	**56%**	**56%**	**57%**	**57%**	**58%**	**58%**	**58%**
Is	*Cell Array Area (%) @ Production [B]*	**55%**	**55%**	**56%**	**56%**	**56%**	**57%**	**57%**	**58%**	**58%**	**58%**
	Non-Core Area (mm^2)	**57**	**45**	**52**	**41**	**64**	**50**	**79**	**77**	**101**	**99**
	Overall Electrical D_0 (faults/m^2) at critical defect size or greater [C]	**2890**	**3671**	**3163**	**4047**	**2580**	**3293**	**2100**	**2155**	**1643**	**1670**
	Random D_0 (faults/m^2) [D]	**1963**	**2493**	**2148**	**2748**	**1752**	**2236**	**1426**	**1464**	**1116**	**1134**
	# Mask Levels [E]	**21**	**22**	**24**	**24**	**24**	**24**	**24**	**26**	**26**	**26**
	Random Faults/Mask	**93**	**113**	**89**	**115**	**73**	**93**	**59**	**56**	**43**	**44**
	DRAM Random Particle per Wafer pass (PWP) Budget (defects/m^2) for Generic Tool Type scaled to 75nm critical defect size or greater										
	CMP Clean	**1076**	**1021**	**610**	**632**	**318**	**311**	**171**	**78**	**30**	**14**
	CMP Insulator	**833**	**790**	**472**	**489**	**246**	**241**	**132**	**60**	**23**	**11**
	CMP Metal	**1276**	**1211**	**723**	**750**	**378**	**369**	**203**	**92**	**36**	**17**
	Coat/Develop/Bake	**333**	**316**	**188**	**195**	**98**	**96**	**53**	**24**	**9**	**4**
	CVD Insulator	**923**	**876**	**523**	**542**	**273**	**267**	**147**	**67**	**26**	**12**
	CVD Oxide Mask	**1133**	**1075**	**642**	**665**	**335**	**327**	**180**	**82**	**32**	**15**
	Dielectric Track	**467**	**443**	**264**	**274**	**138**	**135**	**74**	**34**	**13**	**6**
	Furnace CVD	**638**	**605**	**361**	**374**	**189**	**184**	**101**	**46**	**18**	**9**
	Furnace Fast Ramp	**601**	**571**	**341**	**353**	**178**	**174**	**96**	**43**	**17**	**8**
	Furnace Oxide/Anneal	**481**	**456**	**272**	**282**	**142**	**139**	**76**	**35**	**13**	**6**
	Implant High Current	**559**	**530**	**316**	**328**	**165**	**161**	**89**	**40**	**16**	**7**
	Implant Low/Med Current	**533**	**506**	**302**	**313**	**158**	**154**	**85**	**38**	**15**	**7**
	Inspect PLY	**729**	**691**	**413**	**428**	**216**	**211**	**116**	**53**	**20**	**10**
	Inspect Visual	**752**	**713**	**426**	**441**	**222**	**217**	**119**	**54**	**21**	**10**
	Litho Cell	**624**	**592**	**354**	**367**	**185**	**180**	**99**	**45**	**17**	**8**
	Litho Stepper	**415**	**394**	**235**	**244**	**123**	**120**	**66**	**30**	**12**	**6**
	Measure CD	**623**	**591**	**353**	**366**	**184**	**180**	**99**	**45**	**17**	**8**
	Measure Film	**586**	**556**	**332**	**344**	**173**	**169**	**93**	**42**	**16**	**8**
	Measure Overlay	**570**	**541**	**323**	**335**	**169**	**165**	**91**	**41**	**16**	**8**
	Metal CVD	**587**	**557**	**333**	**345**	**174**	**170**	**93**	**42**	**16**	**8**
	Metal Electroplate	**446**	**423**	**253**	**262**	**132**	**129**	**71**	**32**	**12**	**6**
	Metal Etch	**1080**	**1025**	**612**	**634**	**320**	**312**	**172**	**78**	**30**	**14**
	Metal PVD	**644**	**611**	**365**	**378**	**191**	**186**	**102**	**46**	**18**	**9**
	Plasma Etch	**1144**	**1085**	**648**	**672**	**338**	**331**	**182**	**83**	**32**	**15**
	Plasma Strip	**878**	**833**	**497**	**516**	**260**	**254**	**140**	**63**	**24**	**12**
	RTP CVD	**574**	**545**	**325**	**337**	**170**	**166**	**91**	**41**	**16**	**8**
	RTP Oxide/Anneal	**420**	**398**	**238**	**247**	**124**	**121**	**67**	**30**	**12**	**6**
	Test	**82**	**78**	**46**	**48**	**24**	**24**	**13**	**6**	**2**	**1**
	Vapor Phase Clean	**1215**	**1152**	**688**	**713**	**359**	**351**	**193**	**88**	**34**	**16**
	Wafer Handling	**34**	**33**	**20**	**20**	**10**	**10**	**5**	**2**	**1**	**0**
	Wet Bench	**870**	**825**	**493**	**511**	**257**	**251**	**138**	**63**	**24**	**12**

White–Manufacturable Solutions Exist, and Are Being Optimized	⬜
Yellow–Manufacturable Solutions are Known	🟨
Red–Manufacturable Solutions are NOT Known	🟥

Notes for Table 91:

Was	*[A] As defined in the ORTC Table 1a*
Is	*[A] As defined in the ORTC Table 1a**+1b***
Was	*[B] As defined in the ORTC Table 2a*
Is	*[B] As defined in the ORTC Table **1c+1d***
Was	*[C] As defined in the ORTC Table 5a)*
Is	*[C] As defined in the ORTC Table 5a**+5b. Based on assumption of 89.5% Random Defect Limited Yield (RDLY)***
Was	*[D] Based on assumption of 89.5% Random Defect Limited Yield (RDLY*
Is	***[D] As defined in the ORTC Table 5a+5b. Based on assumption of 89.5% Random Defect Limited Yield (RDLY). Variations from node to node in both overall electrical D_0 and random D_0 values for DRAM are driven predominantly by DRAM chip size variation. Chip size in turn is heavily influenced by a) the DRAM cell area factor and b) projected number of required functions per chip. The interaction of these two variables results in chip size increasing and decreasing with subsequent technology nodes (see ORTC Table 5a+5b). It is the consensus of the Yield Enhancement ITWG members that this variation of D_0 values and the subsequent variation of tool defect budget must addressed in the 2003 revision of the Yield Enhancement chapter of the ITRS to provide a consistent message of defect budget improvement out in time to process tool manufacturers.***
Was	*[E] As defined in the ORTC Table 5a*
Is	*[E] As defined in the ORTC Table 5a**+5b***

Table 93a Defect Detection Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*Driver*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	
	Patterned Wafer Inspection, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [A, B]*								
	Process R&D at 300 cm^2/hr (1 wafer/hr)	**78**	**72**	**66**	**54**	**48**	**42**	**39**	*0.6 x DR*
	Yield ramp at 1200 cm^2/hr (4 wafer/hr)	**104**	**96**	**88**	**72**	**65**	**56**	**52**	*0.8 x DR*
	Volume production at 3000 cm^2/hr (10 wafer/hr)	**130**	**120**	**110**	**90**	**80**	**70**	**66**	*1.0 x DR*
	*High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter (nm) at 90% Capture Rate *[C]*								
	All stages of manufacturing	**130**	**120**	**110**	**90**	**80**	**70**	**65**	*1.0 x DR*
	Process verification (1 wafer/hr)	**130**	**120**	**110**	**90**	**80**	**70**	**65**	*1.0 x DR*
	Volume manufacturing (4 wafer/hr)	**130**	**120**	**110**	**90**	**80**	**70**	**65**	*1.0 x DR*
	Cost of Ownership :volume manufacturing, non-HARI ($/wafer scanned, 10/hr)	**2–5**	**2–5**	**2–5**	**3–7**	**3–7**	**3–7**	**3–7**	
	CoO HARI	**20–50**	**20–50**	**20–50**	**20–50**	**20–50**	**20–50**	**20–50**	
	*Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[D, E, I]*								
Was	Metal film	**91**	**85**	**77**	**32**	**56**	**35**	**33**	*0.5 x DR*
Is	Metal film	**65**	**60**	**55**	**45**	**40**	**35**	**33**	*0.5 x DR*
Was	Nonmetal films	**70**	**65**	**59**	**49**	**43**	**35**	**33**	*0.5 x DR*
Is	Nonmetal films	**65**	**60**	**55**	**45**	**40**	**35**	**33**	*0.5 x DR*
Was	Bare silicon	**70**	**65**	**59**	**49**	**43**	**35**	**33**	*0.5 x DR*
Is	Bare silicon	**65**	**60**	**55**	**45**	**40**	**35**	**33**	*0.5 x DR*
Was	Wafer backside 200mm (# events flip method)	**2500**	**2000**	**2000**	**2000**	**2000**	**2000**	**1000**	
Is	Wafer backside 200mm (# events flip method)	**2500**	**2000**	**2000**	**2000**	**1000**	**1000**	**1000**	
	Wafer backside 200mm (defect size nm)	**200**	**200**	**200**	**200**	**100**	**100**	**100**	
	Defect Review (Patterned wafer)								
	Resolution (nm) *[F]	**7**	**7**	**6**	**5**	**5**	**4**	**3**	*0.05 x DR*
	Coordinate accuracy (µm) at resolution	**2**	**2**	**1**	**1**	**1**	**1**	**1**	*(J)*
	Coordinate accuracy (µm) at size	**15**	**12**	**12**	**10**	**10**	**7**	**7**	
	*Automatic Defect Classification at Defect Review Platform *[G, H]*								
	Redetection: minimum defect size (nm)	**52**	**48**	**44**	**36**	**30**	**28**	**26**	*0.4 x DR*
	Number of defect types	**10**	**10**	**10**	**15**	**15**	**15**	**15**	*[K]*
	Speed (seconds/defect)	**7**	**5**	**5**	**5**	**5**	**5**	**5**	
	Speed w/elemental (seconds/defect)	**20**	**15**	**13**	**10**	**10**	**10**	**10**	

White–Manufacturable Solutions Exist, and Are Being Optimized	⬜
Yellow–Manufacturable Solutions are Known	🟨
Red–Manufacturable Solutions are NOT Known	🟥

Table 93b Defect Detection Technology Requirements—Long-term

Year of Production	*2010*	*2013*	*2016*	*DRIVER*
DRAM ½ Pitch (nm)	*45*	*32*	*22*	
MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*	
MPU Printed Gate Length (nm)	*25*	*18*	*13*	
MPU Physical Gate Length (nm)	*18*	*13*	*9*	
Patterned Wafer Inspection, PSL Spheres at 90% Capture				
Process R&D at 300 cm^2/hr (1 wafer/hr)	**27**	**19**	**13**	*0.6 x DR*
Yield ramp at 1200 cm^2/hr (4wafer/hr)	**36**	**26**	**18**	*0.8 x DR*
Volume production at 3000 cm^2/hr (10wafer/hr)	**46**	**32**	**22**	*1.0 x DR*
High Aspect Ratio Feature Inspection: Defects other than Residue				
All stages of manufacturing	**45**	**32**	**22**	*1.0 x DR*
Process verification (1 wafer/hr)	**45**	**32**	**22**	*1.0 x DR*
Volume manufacturing (4 wafer/hr)	**45**	**32**	**22**	*1.0 x DR*
Cost of Ownership volume manufacturing, non-HARI ($/wafer scanned, 10 /hr)	**3 - 7**	**3 - 5**	**3 - 5**	
CoO HARI	**20 - 50**	**20 - 50**	**20 - 50**	
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [D, E]				
Metal film	**23**	**16**	**11**	*0.5 x DR*
Nonmetal films	**23**	**16**	**11**	*0.5 x DR*
Bare silicon	**23**	**16**	**11**	*0.5 x DR*
Wafer backside 200mm (# events flip method)	**1000**	**1000**	**500**	
Wafer backside 200mm (defect size nm)	**100**	**60**	**50**	
Defect Review (Patterned wafer)				
Resolution (nm) *[F]	**3**	**2**	**2**	*0.05 x DR*
Coordinate accuracy (µm) at resolution	**0.5**	**0.5**	**0.5**	*[J]*
Coordinate accuracy (µm) at size	**5**	**5**	**5**	
Automatic Defect Classification at Defect Review Platform				
Re-detection minimum defect size (nm)	**18**	**13**	**9**	*0.4 x DR*
Number of defect types	**20**	**20**	**25**	*[K]*
Speed (seconds/defect)	**5**	**5**	**5**	
Speed w/elemental (seconds/defect)	**10**	**10**	**10**	

White–Manufacturable Solutions Exist, and Are Being Optimized ⬜
Yellow–Manufacturable Solutions are Known 🟨
Red–Manufacturable Solutions are NOT Known 🟥

Notes for Table 93a and b:

[A] Patterned wafer scan speed is required to be at least 300 cm^2 /hour for process R&D mode, 1,200 cm^2 /hour for yield ramp mode, and, at least, 3,000 cm^2 /hour for volume production mode. Existing solutions do not achieve these targets at the above mentioned sensitivity requirement. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435. (Example-- 3000 cm^2 /hr is about 10, 200 mm wafers and 4.3, 300 mm wafers).

[B] Patterned wafer nuisance defect rate shall be lower than 5% in all process phases. False counts in the R&D phase less than 5%, and less than 1% in the yield ramp and volume production phase. Nuisance is defined as an event indicated and a defect is present, just not the type of interest. These maybe significant and could be studied at a later date. The defect classifier must consider the defect type and assign significance. False is defined at an event is indicated, but no defect can be seen using the review optics path of the detection tool, which supports recipe setup validation.

[C] HARI defects are already considered "killers" at any process stage, but defined at the contact/via levels for full feature size capture. Hence, minimum defect sensitivity was stipulated as 1.0× technology node at all stages of production. Physically uninterrupted coverage of the bottom of a contact by a monolayer of material or more is the model to be detected. If in the future, detection tools can determine size, shape, or remaining material on the order of 0.3× technology node, this will more adequately match known experience for resistance changes. Scan speed for HARi tools have been broken out into process verification and volume production types. Process verification usually refers to SEM-type tools (but not necessarily in the future) and includes voltage contrast capability. The table indicates the approximate number of 200 mm wafers per hour. To obtain the approximate 300 mm wafers per hour, multiple the wafers/hour rate by .435.

Cost of Ownership is derived from the elements found in the International SEMATECH Metrology Tool Model.

Was	*[D] Unpatterned wafer defect detection tools will be required to scan 150 (200 mm or equivalent) wafers per hour at nuisance and false defect rates lower than 5%, for each individually.*
Is	*[D] Un-patterned wafer defect detection tools will be required to scan 150 (200 mm or equivalent) wafers per hour at nuisance and false defect rates lower than 5%, for each individually.* ***Must meet haze and crystal originated pit (COP) requirements specified in the starting material section of the roadmap.***

[E] Metal films inspection tools must detect defects greater than half the minimum contacted pitch (Interconnect chapter technology requirements) × 0.6 (process R&D requirement for patterned wafer defects) for non-grainy films and × 0.6 for rough or grainy films. Nonmetal films and bare Si detection sensitivity must be at least as good as that for patterned wafer inspection to justify monitor wafer usage.

Backside wafer particles are specified as events found at the size indicated. The yellow indication is due to only some inspection tools being capability of meeting this added particle spec.

[F] Resolution corresponds to 10% of patterned wafer detection sensitivity for volume production.

[G] ADC: Detectability, as % of defects redetected, should be greater than 95; Accuracy, as the % of defects correctly classified as per a human expert, should be greater than 95; Repeatability should be greater than 95%; and Reproducibility, as COV%, should be no greater than 5%.

Was	*[H] Assumptions: 5,000 wafer starts per month, defects per wafer based on surface preparation at FEOL, leading to defects per hour that need review, 100% ADC.*
Is	*[H] Assumptions: 5,000 wafer starts per* ***week****, defects per wafer based on surface preparation at FEOL, leading to defects per hour that need review, 100% ADC.*

[I] Backside defects for 300 mm wafers is approximated by multiplying the 200 mm table values by 2.373. The defect sizes remain the same.

[J] Driver is redetection by SEM ADC instrument at a 5000× field of view.

[K] The trend of increasing numbers of defect types, read across the table, is also to indicate decreasing defect size.

Table 94a Yield Learning Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	Wafer size (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**
	Number of mask levels	**25**	**25**	**25**	**27**	**27**	**27**	**29**
Was	*Number of processing steps (simple logic)*	**490**	**503**	**516**	**530**	**543**	**556**	**570**
Is	*Number of processing steps*	**490**	**503**	**516**	**530**	**543**	**556**	**570**
Was	*Cycle time during ramp (# days)*	**25**	**25**	**25**	**27**	**27**	**27**	**29**
Is	*Cycle time during ramp (# days)*	38	38	38	41	41	41	44
	Defect/Fault Sourcing Complexity [A], [G]							
	Logic transistor density/cm^2 (1E6)	**14**	**19**	**26**	**35**	**47**	**63**	**85**
	Defect sourcing complexity factor (1E9) [B]	**7**	**10**	**13**	**18**	**25**	**35**	**49**
	Defect sourcing complexity trend [C]	**1**	**1**	**2**	**3**	**4**	**5**	**7**
	Data Analysis for Rapid Defect/Fault Sourcing							
	Patterned wafer inspection sensitivity (nm) during yield ramp	**104**	**96**	**88**	**72**	**64**	**56**	**52**
Was	Average # of inspections/wafer during full flow	**5**	**5**	**5**	**5.4**	**5.4**	**5.4**	**5.8**
Is	Average # of inspections/wafer during full flow	2.5	2.5	2.5	2.7	2.7	2.7	2.9
Was	Defect data volume (DV) (# data items/wafer) (1E13) [D]	**5.5**	**7.1**	**9.4**	**12.5**	**15.8**	**20.7**	**25.7**
Is	Defect data volume (DV) (# data items/wafer) (1E13) [D]	2.75	3.55	4.7	6.25	7.9	10.35	12.85
	Defect data volume (DV) trend [E]	**1**	**1**	**2**	**2**	**3**	**4**	**5**
	Yield Learning During Ramp from 30% to 80% Sort Yield [F]							
Was	# of yield learning cycles/year based on full flow cycle time	**14.6**	**14.6**	**14.6**	**13.5**	**13.5**	**13.5**	**12.6**
Is	# of yield learning cycles/year based on full flow cycle time	9.7	9.7	9.7	9.0	9.0	9.0	8.4
Was	Required yield improvement rate per learning cycle	**3.4**	**3.4**	**3.4**	**3.7**	**3.7**	**3.7**	**4**
Is	Required yield improvement rate per learning cycle	5.1	5.1	5.1	5.5	5.5	5.5	6.0
Was	Time to identify and fix new defect/fault source during ramp	**12.5**	**12.5**	**12.5**	**13.5**	**13.5**	**13.5**	**14.5**
Is	Time to identify and fix new defect/fault source during ramp	38	38	38	41	41	41	44
Was	# of learning cycles/year for 1 defect/fault sources/month	**8.6**	**8.6**	**8.6**	**7.5**	**7.5**	**7.5**	**6.6**
Is	# of learning cycles/year for 4 defect/fault source/year [I]	5.7	5.7	5.7	5.0	5.0	5.0	4.4
Was	Required yield improvement rate/learning cycle for 1 defect/fault source/month	**5.8**	**5.8**	**5.8**	**6.7**	**6.7**	**6.7**	**7.6**
Is	Required yield improvement rate/learning cycle for 4 defect/fault sources/year [I]	8.7	8.7	8.7	10.0	10.0	10.0	11.4
	Excursion Control							
	Time to recognize defect trend $T_{RT} = f(T_{MP}, N, T_C, V)$ [H]	*	*	*	*	*	*	*
	Time to recognize electrical fault signature	*	*	*	*	*	*	*
	Time to identify defect mechanism $T_{ID} = f(T_{RT}, N, M, R)$ [H]	*	*	*	*	*	*	*
	Time to fix defect mechanism	*	*	*	*	*	*	*

Table 94b Yield Learning Technology Requirements—Long-term

	Year of Production	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	Wafer size (mm)	**450**	**450**	**450**
	Number of mask levels	**31**	**33**	**35**
	Number of processing steps	**610**	**650**	**690**
Was	*Cycle time during ramp (# days)*	**31**	**33**	**35**
Is	*Cycle time during ramp (# days)*	**46.5**	**49.5**	**52.5**
	Defect/Fault Sourcing Complexity [A], [G]			
	Logic transistor density/cm^2 (1E6)	**210**	**519**	**1279**
	Defect sourcing complexity factor (1E9) [B]	**128**	**337**	**883**
	Defect sourcing complexity trend [C]	**18**	**48**	**126**
	Data Analysis for Rapid Defect/Fault Sourcing			
	Patterned wafer inspection sensitivity (nm) during yield ramp	**18**	**13**	**9**
Was	Average # of inspections/wafer during full flow	**6.2**	**6.6**	**7**
Is	Average # of inspections/wafer during full flow	**3.1**	**3.3**	**3.5**
Was	(# data items/wafer) (1E13) [D]	**57.4**	**120.8**	**271.2**
Is	(# data items/wafer) (1E13) [D]	**28.7**	**60.4**	**135.6**
	Defect data volume (DV) trend [E]	**10**	**22**	**49**
	Yield Learning During Ramp from 30% to 80% sort yield [F]			
Was	# of yield learning cycles/year based on full flow cycle time	**11.8**	**11.1**	**10.4**
Is	# of yield learning cycles/year based on full flow cycle time	**7.8**	**7.4**	**7.0**
Was	Required yield improvement rate per learning cycle	**4.2**	**4.5**	**4.8**
Is	Required yield improvement rate per learning cycle	**6.4**	**6.8**	**7.2**
Was	Time to identify and fix new defect/fault source during ramp	**15.5**	**16.5**	**17.5**
Is	Time to identify and fix new defect/fault source during ramp	**46.5**	**49.5**	**52.5**
Was	# of learning cycles/year for 1 defect/fault source/month	**5.8**	**5.1**	**4.4**
Is	# of learning cycles/year for 4 defect/fault sources/year [I]	**3.8**	**3.4**	**3.0**
Was	Required yield improvement rate/learning cycle for 1 defect/fault source/month	**8.7**	**9.9**	**11.3**
Is	Required yield improvement rate/learning cycle for 4 defect/fault sources/year [I]	**13.0**	**14.8**	**16.9**
	Excursion Control During Manufacturing			
	Time to recognize defect trend $T_{RT} = f(T_{MP}, N, T_C, V)$ [H]	*	*	*
	Time to recognize electrical fault signature	*	*	*
	Time to identify defect mechanism $T_{ID} = f(T_{RT}, N, M, R)$ [H]	*	*	*
	Time to fix defect mechanism	*	*	*

White–Manufacturable Solutions Exist, and Are Being Optimized	⬜
Yellow–Manufacturable Solutions are Known	🟨
Red–Manufacturable Solutions are NOT Known	🟥

Notes for Table 94a and b

[A] Defect/Fault sourcing means identifying the point of occurrence (identify process tool, design, test or process integration issue causing a visible or non-visual defect, parametric problem or electrical fault).

[B] Defect sourcing complexity factor = (logic transistor density #/ cm^2)× (# processing steps)

[C] Defect sourcing complexity trend is normalized to 130nm technology node.

Was *[D] Defect data volume (DV) = (# of inspection/wafer in process flow)(wafer area)/patterned wafer sensitivity during ramp Assumes 20% of wafers are inspected on average at each mask step during ramp.*

Is *[D] Defect data volume (DV) = (# of inspection/wafer in process flow)(wafer area)/patterned wafer sensitivity during ramp Assumes* ***10%*** *of wafers are inspected on average at each mask step during ramp.*

[E] DV trend is normalized to 130nm technology node.

Was *[F] Assumes cycle time of one day per mask level. Also, assumes linear reduction in yield learning time based on time to identify and fix each defect/fault source.*

Is *[F] Assumes cycle time of* ***1.5*** *days per mask level. Also, assumes linear reduction in yield learning time based on time to identify and fix each defect/fault source.*

[G] Rapid defect sourcing and yield learning assumptions as follows

- *Keep yield ramp constant (30% intro yield to 80% mature yield) for successive technology nodes.*

Was
- *Keep time to source new yield detractors to 50% of process cycle time.*

Is
- *Keep time to source new yield detractors to* ***1X process*** *cycle time.*

- *New material introduction should not increase defect/fault sourcing time.*
- *Focus defect/fault sourcing on ramp portion of yield learning curve.*
- *Data collection, retention and retrieval will go up exponentially and significant improvement will be required in the IDM tools to enable the above assumptions.*

[H] T_{MP}, N, T_C, V, M and R, respectively represent time between measurement points, number of process steps, cycle time, process variability, number of possible defect mechanisms and resources.

Add ***[I] Metric changed for 2002 from 1 defect/fault sources/month to 4 defect/fault sources/year.***

Table 95a Wafer Environmental Contamination Control Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	Wafer Environment Control							
	Critical particle size (nm) [A]	**65**	**58**	**52**	**45**	**38**	**35**	**33**
	# Particles > critical size (/m^3) [B]	**5**	**4**	**3**	**2**	**2**	**1**	**1**
Was	*Airborne Molecular Contaminants (ppt)) [C]*							
Is	*Airborne Molecular Contaminants (pptM)) [C] [I]*							
	Lithography—bases (as amine, amide, or NH$_3$)	**750**	**750**	**750**	**750**	**750**	**<750**	**<750**
Was	Gate—metals (as Cu, E=2 × $^{10-5}$) [C]	**0.2**	**0.2**	**0.15**	**0.1**	**0.1**	**0.07**	**<0.07**
Is	Gate—metals (as Cu, E=2 × 10^{-5}) ~~[C]~~	**0.2**	**0.2**	**0.15**	**0.1**	**0.1**	**0.07**	**<0.07**
Was	Gate—organics (as molecular weight greater than or equal to 250, E=1 ´ 10-3) [D]	**100**	**90**	**80**	**70**	**60**	**60**	**50**
	Organics (as CH$_4$)	**1800**	**1620**	**1440**	**1260**	**1100**	**900**	**<900**
Is	Gate—organics (as molecular weight greater than or equal to 250, E=1 × 10^{-3}) [D]	**100**	**90**	**80**	**70**	**60**	**60**	**50**
	Organics (as CH$_4$)	**1800**	**1620**	**1440**	**1260**	**1100**	**900**	**<900**
Was	Salicidation contact—acids (as Cl-, E=1 × $^{10-5}$)	**10**	**10**	**10**	**10**	**10**	**<10**	**<10**
Is	Salicidation contact—acids (as Cl-, E=1 × 10^{-5})	**10**	**10**	**10**	**10**	**10**	**<10**	**<10**
Was	Salicidation contact—bases (as NH$_3$, E=1 ×$^{10-6}$)	**20**	**16**	**12**	**10**	**8**	**4**	**<4**
Is	Salicidation contact—bases (as NH$_3$, E=1 ×10^{-6})	**20**	**16**	**12**	**10**	**8**	**4**	**<4**
	Dopants (P or B) [E]	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**	**<10**
	Process Critical Materials [I]							
	Critical particle size (nm) [A]	**65**	**58**	**52**	**45**	**38**	**35**	**33**

White–Manufacturable Solutions Exist, and Are Being Optimized	⬜
Yellow–Manufacturable Solutions are Known	🟨
Red–Manufacturable Solutions are NOT Known	🟥

Table 95a Wafer Environmental Contamination Control Technology Requirements—Near-term (continued)

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	Ultrapure Water							
	Total oxidizable carbon (ppb)	**1**	**1**	**<1**	**<1**	**<1**	**<1**	**<1**
	Bacteria (CFU/liter)	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**	**<1**
	Total silica (ppb)	**0.1**	**0.1**	**0.1**	**0.1**	**0.05**	**0.05**	**0.05**
Add	**Reactive silica (ppb)**	**0.05**	**0.05**	**0.05**	**0.05**	**0.05**	**0.05**	**0.05**
Was	# Particles>critical size (/ml)	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**	**<0.2**
Is	# Particles>critical size (/ml) [A]	**<0.2**	**<0.2**	<0.2	<0.2	**<0.2**	**<0.2**	**<0.2**
Add	**Dissolved Oxygen (ppb) (contaminant based)**	**10**	**7**	**3**	**1**	**1**	**1**	**1**
Add	**Dissolved Oxygen (%value) (process variable based)**	**+/- 20**	**+/- 20**	**+/- 20**	**+/- 20**	**+/- 20**	**+/- 20**	**+/- 20**
Was	Critical cation, anion, metals (ppt, each)	**<20**	**<20**	**<20**	**10**	**10**	**10**	**10**
Is	Critical cation, anion, metals (ppt, each) [G]	**<10**	**<10**	**<10**	**<5**	**<5**	**<5**	**<1**
Add	**Boron (ppt, each)**	**50**	**50**	**50**	**50**	**50**	**50**	**50**
Add	**Temperature Stability (deg C)**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**	**+/- 1**
	Liquid Chemicals [F]							
Was	Particles—critical size (ml)	**<10**	**<10**	**<10**	**<10**	**<1**	**<1**	**<1**
Is	**# Particles>critical size (/ml) [A]**	**<10**	**<10**	**<10**	**<10**	**<1**	**<1**	**<1**
	HF-, H_2O_2, NH_4OH: Fe, Cu (ppt, each)	**<150**	**<135**	**<110**	**<100**	**<90**	**<50**	**<50**
Was	Critical cation, anion, metals (ppt, each)	**<10**	**<10**	**<10**	**<5**	**<5**	**<5**	**<1**
Is	Critical cation, anion, metals (ppt, each) [G]	**<10**	**<10**	**<10**	**<5**	**<5**	**<5**	**<1**
Was	HF-only, TOC (ppb)	**<30**	**<30**	**<25**	**<20**	**<15**	**<10**	**<10**
Is	HF-only, TOC (ppb) [H]	**<30**	**<30**	**<25**	**<20**	**<15**	**<10**	**<10**
	HCl, H_2SO_4: All impurities (ppt)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
	BEOL Solvents, Strippers K, Li, Na, (ppt, each)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**
	ILD CVD Precursors (e.g., TEOS)							
	Metals (ppb)	**<1**	**<1**	**<1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
	H_2O (ppmV)	**<10**	**<10**	**<10**	**<5**	**<5**	**<5**	**<1**
	Bulk Gases							
	N_2, O_2, Ar, H_2: H_2O, O_2, CO_2, CH_4 (ppt, each)	**<1000**	**<1000**	**<1000**	**<1000**	**<1000**	**<100**	**<100**
	# Particles > critical size (/liter)	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**
	Specialty Gases							
	# POU particles > critical size (/liter) [F]	**2**	**2**	**2**	**2**	**2**	**2**	**2**
	Inerts—Oxide/Photoresist Etchants/Strippers							
	O_2 (ppbV)	**<1000**	**<1000**	**<1000**	**<500**	**<500**	**<500**	**<100**
	H_2O (ppbV)	**<1000**	**<1000**	**<1000**	**<500**	**<500**	**<500**	**<100**
	Individual specified metals (ppbWT)	**<10**	**<10**	**<10**	**<10**	**<10**	**<1**	**<1**

White–Manufacturable Solutions Exist, and Are Being Optimized	⬜
Yellow–Manufacturable Solutions are Known	🟨
Red–Manufacturable Solutions are NOT Known	🟥

Table 95b Wafer Environmental Contamination Control Technology Requirements—Long-term

	Year of Production	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	Wafer Environment Control			
	Critical particle size (nm) [A]	**23**	**16**	**11**
	# Particles > critical size ($/m^3$) [B]	**1**	**<1**	**<1**
Was	*Airborne Molecular Contaminants (ppt) [C]*			
Is	*Airborne Molecular Contaminants (pptM)) [C]*			
	Lithography—bases (as amine, amide, or NH$_3$)	**<750**	**<750**	**<750**
Was	Gate—metals (as Cu, E=2 × $^{10-5}$) [C]	**<0.07**	**<0.07**	**<0.07**
Is	Gate—metals (as Cu, E=2 × 10^{-5}) ~~[C]~~	**<0.07**	**<0.07**	**<0.07**
Was	Gate—organics (as molecular weight greater than or equal to 250, E=1 ´ 10-3) [D]	**40**	**30**	**20**
Is	Gate—organics (as molecular weight greater than or equal to 250, E=1 × 10^{-3}) [D]	**40**	**30**	**20**
	Organics (as CH$_4$)	**<900**	**<900**	**<900**
Was	Salicidation contact—acids (as Cl-, E=1 × $^{10-5}$)	**<10**	**<10**	**<10**
Is	Salicidation contact—acids (as Cl-, E=1 × 10^{-5})	**<10**	**<10**	**<10**
Was	Salicidation contact—bases (as NH$_3$, E=1 × $^{10-6}$)	**<4**	**<4**	**<4**
Is	Salicidation contact—bases (as NH$_3$, E=1 × 10^{-6})	**<4**	**<4**	**<4**
	Dopants (P or B) [E]	**<10**	**<10**	**<10**
	Process Critical Materials			
	Critical particle size (nm) [A]	**23**	**16**	**11**
	Ultrapure Water			
	Total oxidizable carbon (ppb)	**<1**	**<1**	**<1**
	Bacteria (CFU/liter)	**<1**	**<1**	**<1**
	Total silica (ppb)	**0.01**	**<0.01**	**<0.01**
Was	Reactive silica (ppb)	**blank**	**blank**	**blank**
Is	Reactive silica (ppb)	**0.01**	**0.01**	**0.01**
Was	Particles—critical size (ml)	**<0.2**	**<0.2**	**<0.2**
Is	**# Particles>critical size (/ml)**	**<0.2**	**<0.2**	**<0.2**
Was	Dissolved Oxygen (ppb) (contaminant based)	**blank**	**blank**	**blank**
Is	Dissolved Oxygen (ppb) (contaminant based)	**1**	**1**	**1**
Was	Dissolved Oxygen (%value) (process variable based)	**blank**	**blank**	**blank**
Is	Dissolved Oxygen (%value) (process variable based)	**+/- 10**	**+/- 10**	**+/- 10**
Was	Critical cation, anion, metals (ppt, each)	**<10**	**<10**	**<10**
Is	Critical cation, anion, metals (ppt, each) [G]	**≤1**	**≤1**	**≤1**
Was	Boron (ppt, each)	**blank**	**blank**	**blank**
Is	Boron (ppt, each)	**50**	**50**	**50**
Was	Temperature Stability (deg C)	**blank**	**blank**	**blank**
Is	Temperature Stability (deg C)	**+/- 1**	**+/- 1**	**+/- 1**

White–Manufacturable Solutions Exist, and Are Being Optimized ⬜
Yellow–Manufacturable Solutions are Known 🟨
Red–Manufacturable Solutions are NOT Known 🟥

Table 95b Technology Requirements for Wafer Environmental Contamination Control—Long-term (continued)

	Year of Production	*2010*	*2013*	*2016*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU / ASIC ½ Pitch (nm)	*50*	*35*	*25*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	Liquid Chemicals [F]			
	# Particles > critical size (/ml)	**<1**	**<1**	**<1**
	HF-, H_2O_2, NH_4OH: Fe, Cu (ppt, each)	**<50**	**<40**	**<40**
Was	Critical cation, anion, metals (ppt, each)	**<1**	**<1**	**<1**
Is	Critical cation, anion, metals (ppt, each) [G]	**<1**	**<1**	**<1**
Was	HF-only, TOC (ppb)	**<8**	**<6**	**<4**
Is	HF-only, TOC (ppb) [H]			
	HCl, H_2SO_4: All impurities (ppt)	**<1000**	**<1000**	**<1000**
	BEOL Solvents, Strippers K, Li, Na, (ppt, each)	**<1000**	**<1000**	**<1000**
	ILD CVD Precursors (e.g., TEOS)			
	Metals (ppb)	**<0.1**	**<0.1**	**<0.1**
	H_2O (ppmV)	**<1**	**<1**	**<1**
	Bulk Gases			
	N_2, O_2, Ar, H_2: H_2O, O_2, CO_2, CH_4 (ppt, each)	**<100**	**<100**	**<100**
	# Particles > critical size (/liter)	**<0.1**	**<0.1**	**<0.1**
	Specialty Gases			
	# POU particles > critical size (/liter) [F]	**2**	**2**	**2**
	Inerts—Oxide/Photoresist Etchants/Strippers			
	O_2 (ppbV)	**<100**	**<50**	**<50**
	H_2O (ppbV)	**<100**	**<50**	**<50**
	Individual specified metals(ppbWT)	**<1**	**<1**	**<1**

White–Manufacturable Solutions Exist, and Are Being Optimized	⬜
Yellow–Manufacturable Solutions are Known	🟨
Red–Manufacturable Solutions are NOT Known	🟥

Notes for Table 95a and b

Was	*[A] Critical particle size is based on ½ design rule. All defect densities are "normalized" to critical particle size. Critical particle size does not necessarily mean "killer" particles. For UPW water and liquid chemicals (see text), particle measurements at critical particle size is not possible with existing metrology, but is inferred from assumed particle size distributions and measurements of particles at sizes greater than critical particle dimension.*
Is	*[A] Critical particle size is based on ½ design rule. All defect densities are "normalized" to critical particle size. Critical particle size does not necessarily mean "killer" particles.* ***Because of instrumentation limitations, particle densities at the critical dimension for nodes < 90 nm will need to be estimated from measured densities of larger particles and an assumed particle size distribution. Although the particle size distribution will depend on the fluid (e.g. water, clean room air, gases), $f(x)=K*1/X^{2.2}$ is a reasonable approximation for the fluids of interest. (References: Cooper, D. W. , "Comparing Three Environmental Particle Size Distributions", Journal of the IES, Jan/Feb 1991, pages 21-24; and Pui, D. Y. H. and Liu, B. Y. H., "Advances in Instrumentation for Atmospheric Aerosol Measurement", TSI Journal of Particle Instrumentation, Vol. 4, Number 2, Jul-Dec 1989, pages 3-20)***
	[B] Airborne particle requirements are based on an assumed value for deposition velocity of 0.01 cm/second, resulting in 1 particle/m^2/hr. for a ambient concentration of 3 particles/m^3. (This value represents an approximate value at atmospheric conditions.)
Was	*[C] Ion indicated is basis for calculation. Exposure time is 60 minutes with starting surface concentration of zero. Basis for lithography is defined by lithography roadmap. Gate metals and organics scale as surface preparation roadmap metallics and organics. All airborne molecular contaminants calculated as S=E*(N*V/4); where S is the arrival rate (molecules/second/cm^2), E is the sticking coefficient (between 0 and 1, N is the concentration in air (molecules/cm^3); and V is the average thermal velocity (cm/second)*
Is	*[C] Ion/**species** indicated is basis for calculation. Exposure time is 60 minutes with starting surface concentration of zero. Basis for lithography **projections** is defined by lithography roadmap. Gate metals and organics scale as **defined in the** surface preparation roadmap **for** metallics and organics. All airborne molecular contaminants **are** calculated as S=E*(N*V/4); where S is the arrival rate (molecules/second/cm^2), E is the sticking coefficient (between 0 and 1), N is the concentration in air (molecules/cm^3); and V is the average thermal velocity (cm/second).*
Was	*[D] The sticking coefficients for organics vary greatly with molecular structure and are also dependent on surface termination. In general molecular weights < 250 not considered detrimental due to the higher volatility of these compounds.* *[E] Includes P, B, As, Sb*
Is	*[D] The sticking coefficients for organics vary greatly with molecular structure and are also dependent on surface termination. In general, molecular weights < 250 **are** not considered detrimental due to the higher volatility of these compounds.* *[E] Includes P, B, As, Sb*
Was	*[F] Particle targets apply at POU, not incoming chemical. Point-of-tool connection chemical metallic targets are based on Epi starting material, sub-ppb contribution from bulk distribution system, 1:1:5 standard clean 1 (SC-1) and elevated temperature 1:1:5 standard clean 2 (SC-2) final clean step. "HF last" or "APM last" cleans would require ~10× and ~100× improved purity HF (mostly Cu) and APM chemicals, respectively.*
Is	*[F] Particle targets apply at POU, not incoming chemical. Point-of-tool connection chemical metallic targets are based on Epi starting material, sub-ppb contribution from bulk distribution system, 1:1:5 standard clean 1 (SC-1) and elevated temperature 1:1:5 standard clean 2 (SC-2) final clean step. "HF last" or "APM last" cleans would require ~10× and ~100× improved purity for HF (mostly Cu) and APM chemicals, respectively.*
	[G] Critical metals and ions include: Ca, Co, Cu, Cr, Fe, Mo, Mn, Na, Ni, W
	[H] TOC values are based on best available technology and are not necessarily supported by yield data.
Add	***[I] Units on all contaminants in Table 95 are often given as ppb (or ppm or ppt, we use ppb here solely for demonstration purposes). The reader should be aware that these units of parts per billion (ppb) may be ppb by mass, volume, or molar ratios. Where not designated, the following guidelines apply: Chemicals and UPW are typically ppb by mass, Gases and Clean Room are typically ppb by volume. In the case of the fluid acting as an ideal gas, ppb by volume is equal to ppb molar. The notable exception to the above is metals in gases which are ppb by mass.***