

MODELING AND SIMULATION

Table 102 Modeling and Simulation Difficult Challenges [Update]

	Difficult Challenges ≥ 65 nm, Through 2007	Summary Of Issues
	High-frequency Circuit Modeling (>5 GHz)	<ul style="list-style-type: none"> Efficient simulation of full-chip interconnect delay Accurate 3D interconnect model; inductance, transmission line models High frequency circuit models including non-quasi-static, substrate noise and coupling Parameter extraction without RF measurements
Was	Modeling of Ultra Shallow Dopant Distributions, Junctions, and Silicidation	<ul style="list-style-type: none"> Dopant models and parameters (damage, high- concentration, activation, metastable effects, diffusion, interface and silicide effects) Characterization tools for these ultra shallow geometries and dopant levels
Is	Modeling of Ultra Shallow Dopant Distributions (Junctions, Activation), and Silicidation	<ul style="list-style-type: none"> Dopant models and parameters (damage, high- concentration, activation, metastable effects, diffusion, interface and silicide effects) in Si based substrate, i.e. Si, SiGe:C (incl. strain), SOI and ultra-thin body devices Characterization tools for these ultra shallow geometries and dopant levels
Was	Modeling Deposition and Etch Variations, Feature Variations across a Wafer	<ul style="list-style-type: none"> Fundamental physical data (e.g., rate constants, cross sections, surface chemistry); reduced models for complex chemistry Linked equipment / feature models CMP (full wafer and chip level, pattern dependent effects) Next generation equipment/wafer models
Is	Modeling Deposition and Etch Rate Variations, Feature Geometry Variations across a Wafer	<ul style="list-style-type: none"> Fundamental physical data (e.g., rate constants, cross sections, surface chemistry); reaction mechanisms and reduced models for complex chemistry Linked equipment / feature scale models CMP (full wafer and chip level, pattern dependent effects) MOCVD, PECVD and ALD modeling Next Multi-generation equipment/wafer models
Was	Modeling of Lithography Technology	<ul style="list-style-type: none"> Predictive resist models Resolution enhancement techniques; mask synthesis (OPC, PSM) 248 nm versus 193 nm versus 157 nm evaluation and tradeoffs Next-generation lithography system models
Is	Modeling of Lithography Technology	<ul style="list-style-type: none"> Predictive resist models (incl. mechanical stability and etch resistance) Line-edge roughness and its effect on circuit performance Resolution enhancement techniques; mask synthesis (OPC, PSM) 248 nm versus 193 nm versus 157 nm evaluation and tradeoffs Next Multi-generation lithography system models
Was	Gate Stack Models for Ultra-Thin Dielectrics	<ul style="list-style-type: none"> Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., MeOx) Model dielectric constant, surface states, reliability, breakdown, and tunneling from process/material conditions
Is	Gate Stack Models for Ultra-Thin Dielectrics	<ul style="list-style-type: none"> Electrical and processing models for alternate high-k gate dielectrics, metal gates, and alternative gate materials CMOS structures (e.g., MeOx) Model dielectric constant, bulk polarization charge, surface states, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions

Table 102 Modeling and Simulation Difficult Challenges [Update](continued)

	Difficult Challenges < 65 nm, Beyond 2007	Summary Of Issues
Was	Complementing Continuum Tools with Atomistic Ones.	• A succession of modeling tools that marry atomistic effects with present day continuum software tools
Is	<u>Extend beyond continuum tools</u>	• A succession of modeling tools that marry combine atomistic effects with present day continuum software tools
Was	Ultimate CMOS Simulation Capability	• Methods and algorithms that will allow prediction of CMOS limits • Quantum based simulators
Is	**Ultimate CMOS <u>and nanoscale</u> simulation capability	• Methods and algorithms that will allow which contribute to prediction of CMOS limits • Quantum based simulators • <u>Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS</u> • <u>Models for device impact of statistical fluctuations in structures and dopant distributions</u>
Was	Nano-Scale Device Modeling	• New device concepts beyond traditional CMOS based on silicon technology such as vertical MOS, heterostructures, thin-film transistors, single electron transistors
Is	** <u>Compact modeling including more physical models and statistics</u>	<u>Computer-efficient inclusion of influences of statistics (incl. correlations) before process freeze, quantum/ballistic transport, etc., into compact modeling</u>
Was	Thermo-Mechanical Modeling for Reliability	• Stress voiding, electromigration, piezoelectric effects, fracture, and adhesion simulation tools
Is	Thermal-Mechanical- <u>Electrical</u> Modeling for Reliability <u>interconnections and packaging</u>	• <u>Model thermal-mechanical and electronic properties of Low-k, High-k and conductors and the impact of processing of these properties</u> • <u>Model reliability of packages and interconnects, e.g.</u> stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion simulation tools
Was	Software Module Integration	• Seamless integration of simulation modules with focus on interplay and interfacing of the modules in order to enhance design effectiveness
Is	<u>Development and seamless integration of software modules incl. advanced algorithms</u>	• <u>Development of problem-specific algorithms</u> • Seamless integration of simulation modules with focus on interplay and interfacing of the modules in order to enhance design effectiveness, <u>metrology, by using design of experiment, job farming, Open/standardized formats</u>

****Note—This new information changes the Grand Challenges for the ITRS.**

Table 103a Modeling and Simulation Technology Requirements: Capabilities—Near-term

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
Add	MPU Printed Gate Length (nm)	90	75	65	53	45	35
Add	MPU Physical Gate Length (nm)	65	53	45	37	28	25
<i>Lithography</i>							
Was	Lithography: evaluate wavelength	Evaluate 248 nm versus 193 nm	Evaluate 193 nm Versus VUV	Evaluate VUV versus EUV,EB			
Is	Lithography: evaluate wavelength	Evaluate 248 nm versus 193 nm	Evaluate 193 nm versus VUV, 157 nm	Evaluate 157 nm versus EUV, EPL, maskless lithography			
Was	Resist models	193nm resist models	157 nm resist models	Detailed chemical resist model			
Is	Resist models	193nm resist models *	157 nm resist models including ultra-thin resists	Detailed chemically amplified resist model incl. EUV resists			
<i>Front End Process Modeling</i>							
Was	Gate Stack: evaluate materials	Model alternate dielectrics and gates (interfaces, impurity diffusion, barrier height)			Materials to electrical properties		
Is	Gate Stack: evaluate materials	Model alternative dielectrics and gates (interfaces, impurity diffusion, barriers height)			Materials to electrical properties		
Was	Diffusion and activation models	Interfaces, stress, ultra-shallow junctions, Si:Ge:C, source/drain.		Move from calibrated phenomenological to physically based models			
Is	Diffusion and activation models	Interfaces, stress/strain, ultra-shallow junctions and activation incl. SOI, Si:Ge:C, source/drain.		Move from calibrated phenomenological to physically based models for Si and other Si based materials			
<i>Back End Process/Equipment/Topography Modeling</i>							
	Models for multi-level metal	Mechanical/thermal stress and cycling		Stress voiding, adhesion, and fracture			
Was	Planarization models	CMP/dummy features		Full CMP model			
Is	Planarization models	CMP/dummy features		Full wafer and chip level CMP model			
Was	Equipment/feature scale link	Plasma deposition and etch models		Litho/plasma integrated model to predict within-chip feature variation			
Is	Equipment/feature scale link	Plasma deposition and etch models		Litho/plasma integrated model to predict within-chip feature and its variation			
Was	<i>Device modeling (Numerical)</i>						
Is	Numerical Device Modeling						
Was	Bulk CMOS	Gate current models; gate oxide reliability		Full quantum gate stack models; device models with relevant quantum effects included			
Is	Bulk CMOS	Gate current models; gate oxide reliability		Mobility models including e.g. surface roughness and high-k		Full quantum gate stack models; device models with relevant quantum effects included	
Was	Non-bulk CMOS	Heterostructures; stress dependent mobility model for Si:Ge:C		"What if" capability for non-bulk CMOS devices			
Is	Non-bulk CMOS	Heterostructures; Stress dependent mobility model, also for Si:Ge:C		"What if" capability for non-bulk CMOS devices			
Was	RF Modeling	Noise models		Frequency, noise, parasitic device tradeoffs			
Is	RF Modeling	Noise models		High frequency noise, parasitic device models			

* For 2001-2002, workarounds exist, but research is still needed for predictability

Table 103a Modeling and Simulation Technology Requirements: Capabilities—Near-term (continued)

Year of Production		2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)		130	115	100	90	80	70	65
MPU / ASIC ½ Pitch (nm)		150	130	107	90	80	70	65
Add	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
Add	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
<i>Circuit Element Modeling/ECAD</i>								
Was	New circuit element models	SOI circuit model	Non- bulk CMOS compact models			2D quantum effects / non-quasi-static models		
Is	New circuit element models	SOI circuit model	Non- bulk CMOS (e.g. double gate) compact models/ non-quasi-static models			2D quantum effects non-quasi-static models		
Was	Interconnect models	Full-chip RC	On-chip inductance effects, full chip RLC					
Is	Interconnect models	Full-Chip RLC	On-chip inductance effects, hierarchical full chip RLC, reliability, anomalous width scaling of resistance					
Delete	Design/device links	loff/on link	Best practice analysis for design					
<i>Package Modeling</i>								
Was	Package models	Complex interconnect geometries	Thermo-mechanical-electrical integrated models					
Is	Package models	Complex interconnect geometries	Thermo-mechanical-electrical integrated models incl. (non-bulk and composite) material properties, esp. for reliability					
Was	Unified package/chip models	Co-design package / circuit models (multiple power and ground planes)	Unified RLC extraction for package/chip			Full-wave analysis		
Is	Unified package/chip models	Co-design package / circuit models (multiple power and ground planes)	Unified RLC extraction for package/chips			Full-wave analysis, reduced order models		
<i>Numerics</i>								
Was	Numerical algorithms	Robust, reliable 3D grid generation	Improve usability of 3D simulators			Exploit parallel computation		
Is	Numerical algorithms	◆ Robust, reliable 3D grid generation esp. for process simulation	Exploit parallel computation					

Note: For 2001-2002, interim solutions are known, but research is still needed towards mature commercial solutions

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

Interim Solutions are Known



A definition of interim solutions is included in the Glossary.

Table 103b Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term

Year of Production		2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
Add	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
Add	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Was	Overall technology cost reduction target (due to TCAD)	25%		35%			40%	
Is	Technology-development cost reduction (due to TCAD)	25%		35%			40%	
<i>Lithography Modeling</i>								
Was	Resist profile prediction accuracy	10% (13nm)	10% (11.5nm)	10% (10nm)	10% (9nm)	10% (8nm)	10% (7nm)	10% (6.5nm)
Is	Resist profile prediction accuracy (10 % of printed gate length)	9nm	7.5nm	6.5nm	5.3nm	4.5nm	4nm	3.5nm
Was	OPC model accuracy	5% (6.5nm)	5% (5.8nm)	5% (5nm)	5% (4.5nm)	5% (4nm)	5% (3.5nm)	5% (3.3nm)
Is	OPC model accuracy (2% of OPC features)	3.5nm	3nm	2.5nm	2.5nm	2nm	2nm	1.5nm
<i>Front End Process Modeling</i>								
Was	Vertical junction depth simulation accuracy	5% (6.5nm)	5% (5.8nm)	5% (5nm)	5% (4.5nm)	5% (4nm)	5% (3.5nm)	5% (3.3nm)
Is	Vertical junction depth simulation accuracy	10% (6.5nm)	10% (5.3nm)	10% (4.5nm)	10% (3.7nm)	10% (3.2nm)	10% (2.8nm)	10% (2.5nm)
Was	Lateral junction depth simulation accuracy	5% (6.5nm)	5% (5.8nm)	5% (5nm)	5% (4.5nm)	5% (4nm)	5% (3.5nm)	5% (3.3nm)
Is	Lateral junction depth (and abruptness) simulation accuracy	10% (6.5nm)	10% (5.3nm)	10% (4.5nm)	10% (3.7nm)	10% (3.2nm)	10% (2.8nm)	10% (2.5nm)
Was	Total source/drain series resistance (accuracy)	20%	20%	20%	20%	20%	20%	20%
Is	Total source/drain series resistance (accuracy)	10%	10%	10%	10%	10%	10%	10%
<i>Back end process/Equipment/Topography Modeling</i>								
Was	Etch/deposition cross wafer uniformity (% accuracy of the control spec)	10% (13nm)	10% (11.5nm)	10% (10nm)	10% (9nm)	10% (8nm)	10% (7nm)	10% (6.5nm)
Is	Etch/deposition cross wafer uniformity (10 % accuracy of the MPU physical gate length)	6.5nm	5.3nm	4.5nm	3.7nm	3.2nm	2.8nm	2.5nm
	2D/3D topography accuracy	10% (13nm)	10% (11.5nm)	10% (10nm)	10% (9nm)	10% (8nm)	10% (7nm)	10% (6.5nm)
Was	<i>Device modeling (Numerical)</i>							
Is	Numerical Device Modeling							
	Accuracy of ft at given ft (% of maximum chip frequency)	10%	10%	10%	10%	10%	10%	10%
Was	Gate leakage current accuracy (%) (I_g/I_{off})	70%	70%	40%	40%	40%	30%	30%
Is	Gate leakage current accuracy (%) (I_g/I_{off})	30%	30%	25%	25%	25%	20%	20%
	I_{on} accuracy	5%	5%	5%	5%	5%	3%	3%
	I_{off} accuracy	70%	70%	40%	40%	40%	30%	30%
	Long-channel V_t (accuracy)	4% (48–60mV)	3% (33–42mV)	3% (27–36mV)	3% (24–33mV)	3% (21–30mV)	3% (18–27mV)	3% (17–23mV)
	V_t rolloff accuracy (mV)	20mV	20mV	15mV	15mV	15mV	10mV	10mV
	V_t 3 Φ variation (%)	30%	30%	30%	30%	30%	30%	30%

Table 103b Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term (continued)

Year of Production		2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
Add	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
Add	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
<i>Circuit Element Modeling/ECAD</i>								
	I-V error—compact model accuracy	5%	5%	5%	5%	5%	3%	3%
	Sub-threshold current accuracy model accuracy	50%	20%	10%	10%	10%	7%	7%
	Intrinsic MOS C-V accuracy	<6%	<5%	<5%	<5%	<5%	<3%	<3%
	Parasitic C-V accuracy	5–10%	5%	5%	5%	5%	<3%	<3%
	Accuracy of Gm and r0 at Vt +150mV versus L, Vbs, Vds and T	20%	15%	10%	10%	10%	5%	5%
	Circuit delay accuracy (% of maximum chip frequency)	5%	5%	5%	5%	5%	3%	3%
	RLC delay accuracy (% of maximum chip frequency)	5%	5%	5%	5%	5%	3%	3%
<i>Package Modeling</i>								
	Package delay accuracy (% of off-chip clock frequency)	1%	1%	1%	1%	1%	1%	1%
	Temperature distribution for chip and package (accuracy)	5C	5C	5C	5C	5C	5C	5C
<i>Numerical Method</i>								
Was	Speed-up of algorithms for 3D process/device	2×	3×	4×	5×	6×	7×	8×
Is	Speed-up of algorithms for 3D process/device (compared with year 2000)	2×	3×	4×	5×	6×	7×	8×
	Linear solvers (kilo equations/minute)	250k	300k	600k	650k	700k	750k	800k
Was	Parallel speed-up	2×	3×	4×	6×	8×	12×	16×
Is	Parallel speed-up (compared with year 2000)	2×	3×	4×	6×	8×	12×	16×
	MFLOPS required	1000	2000	4000	5000	6500	8000	10000

* The accuracy numbers in the table are those expected after detailed calibration to experimental data.

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known



Table 103c Modeling and Simulation Technology Requirements: Capabilities—Long-term

Year of Production		2010	2013	2016
DRAM ½ Pitch (nm)		45	32	22
MPU / ASIC ½ Pitch (nm)		50	35	25
Add	MPU Printed Gate Length (nm)	25	18	13
Add	MPU Physical Gate Length (nm)	18	13	9.0
<i>Lithography Modeling</i>				
Was	Next generation lithography	NGL models		
Is	Next generation lithography	NGL models and modeling of materials and components		
	Resist technology	Finite polymer-size effects	Non-conventional photo-resist models	
<i>Front End process Modeling</i>				
Was	Advanced process models	Alternative materials	Atomistic process model	
Is	Advanced process models	Processing and properties of alternative materials	Atomistic process model	
	Advanced doping models	New technology needed		
<i>Back End process/Equipment/Topography Modeling</i>				
Was	Alternative material models	Calculation of dielectric constant	Atomistic material model- materials to electronic properties	
Is	Alternative material models	Calculation of thermal, mechanical and electronic properties dielectric constant	Atomistic material model- materials to electronic properties	
	Equipment simulation	Computer engineered materials and process recipes		
<i>Numerical Device Modeling</i>				
Was	Emerging devices	Trade-off analysis tools	Quantum effect devices	
Is	Emerging devices	Nanoscale simulation capability including accurate quantum effects		
<i>Circuit Element Modeling/ECAD</i>				
Was	Advanced circuit models	Circuit models for alternative devices	New technology needed	
Is	Advanced circuit models	Circuit models for alternative CMOS devices incl. influences of statistics	Circuit models for nanoscale devices and interconnects	
<i>Package Modeling</i>				
Was	Electrical/optical models	Mixed electrical/-optical analysis	New technology needed	
Is	Electrical/optical models	Mixed electrical/-optical analysis	Reliability prediction in coupled modeling	
<i>Numerics</i>				
	Numerical algorithms	Efficient atomistic/quantum methods	Multi-scale simulation (atomistic-continuum)	

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

