INTERCONNECT

Table 61 Interconnect Difficult Challenges [Update]

	Five Difficult Challenges ≥65 nm / Through 2007	*Summary Of Issues*
	Introduction of new materials*	The rapid introduction of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Was	Integration of new processes and structures*	Combinations of materials and processes used to fabricate new structures create integration complexity.
Is	Integration of new processes and structures*	Combinations of materials and processes used to fabricate new structures create integration complexity. ***Design and layout solutions are needed. Lack of interconnect/packaging architecture design optimization tool.***
	Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
	Attaining dimensional control	Three-dimensional control (3D CD), with its associated metrology, of interconnect features is necessary for circuit performance and reliability. The multiplicity of levels combined with new materials, reduced feature size and pattern dependent processes create this challenge.
	Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
	Five Difficult Challenges <65 nm / Beyond 2007	***Summary Of Issues***
	Dimensional control and metrology	Multi-dimensional control and metrology of interconnect features is necessary for circuit performance and reliability.
	Patterning, cleaning, and filling high aspect ratios features	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low κ dual-Damascene metal structures and DRAM.
	Integration of new processes and structures	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
	Continued introductions of new materials and size effects	Further introductions of materials/processes are expected. Microstructure and dimensional effects become important when Cu/low κ interconnect is extended to smaller features.
	Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

Table 62a MPU Interconnect Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
	MPU/ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	Number of metal levels	8	8	8	9	10	10	10
	Number of optional levels—ground planes/capacitors	2	2	4	4	4	4	4
	Total interconnect length (m/cm^2)—active wiring only, excluding global levels [1]	4086	4843	5788	6879	9068	10022	11169
	FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	1.22	1.03	0.86	0.73	0.55	0.5	0.45
	Jmax (A/cm^2)—wire (at 105°C)	9.60E+05	1.10E+06	1.30E+06	1.50E+06	1.70E+06	1.90E+06	2.10E+06
	Imax (mA)—via (at 105°C)	0.32	0.29	0.27	0.24	0.22	0.2	0.18
	Local wiring pitch (nm)	350	295	245	210	185	170	150
	Local wiring A/R (for Cu)	1.6	1.6	1.6	1.7	1.7	1.7	1.7
Add	*Interconnect RC delay 1 mm line (ps)*	86	121	176	198	256	303	342
Add	*Line length where τ = RC delay (µm)*	137	106	80	70	57	50	44
	Cu thinning at minimum pitch due to erosion (nm), 10% ´ height, 50% areal density, 500 µm square array	28	24	20	18	16	14	13
	Intermediate wiring pitch (nm)	450	380	320	275	240	215	195
	Intermediate wiring dual Damascene A/R (Cu wire/via)	1.6/1.4	1.6/1.4	1.7/1.5	1.7/1.5	1.7/1.5	1.7/1.6	1.8/1.6
Add	*Interconnect RC delay 1 mm line (ps)*	53	75	101	127	155	191	198
Add	*Line length where τ = RC delay (µm)*	174	135	106	88	73	63	58
	Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	36	30	27	23	20	18	18
	Minimum global wiring pitch (nm)	670	565	475	410	360	320	290
Add	*Ratio range (global wiring pitches/intermediate wiring pitch)*	1.5 - 5.0	1.5 - 5.0	1.5 - 5.0	1.5 - 6.7	1.5 - 6.7	1.5 - 6.7	1.5 - 8.0
	Global wiring dual Damascene A/R (Cu wire/via)	2.0/1.8	2.0/1.8	2.1/1.9	2.1/1.9	2.2/2.0	2.2/2.0	2.2/2.0
Add	*Interconnect RC delay 1 mm line (ps) at minimum pitch*	21	29	40	37	59	74	79
Add	*Line length where τ = RC delay (µm) minimum pitch*	280	216	168	163	118	100	92
Delete	~~Cu thinning global wiring due to dishing and erosion (nm), 10% × height, 80% areal density, 15 mm wide wire~~	~~67~~	~~57~~	~~50~~	~~48~~	~~40~~	~~35~~	~~32~~
Add	*Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density*	225	190	168	193	176	158	172
	Cu thinning global wiring due to dishing (nm), 100 µm wide feature	40	34	30	29	24	21	19
	Conductor effective resistivity (µΩ-cm) Cu intermediate wiring	2.2	2.2	2.2	2.2	2.2	2.2	2.2
	Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	16	14	12	10	9	8	7
	Interlevel metal insulator (minimum expected) —effective dielectric constant (κ)	3.0-3.6	3.0–3.6	3.0–3.6	2.6–3.1	2.6–3.1	2.6–3.1	2.3–2.7
	Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ)	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4	<2.1

Notes for Table 62a and b

[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for local and semiglobal wiring levels are populated. The wiring lengths for each level are then summed to calculate the total interconnect length per square centimeter of active area.

[2] This metric is calculated by assuming that a 5 FIT reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.

[3] Calculated for a conformal layer in intermediate wiring to meet minimum effective conductor resistivity

Table 62b MPU Interconnect Technology Requirements—Long-term

	Year of Production	2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU/ASIC ½ Pitch (nm)	45	32	22
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Number of metal levels	10	11	11
	Number of optional levels – ground planes/capacitors	4	4	4
	Total interconnect length (m/cm^2) – active wiring only, excluding global levels [1]	16063	22695	33508
	FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	0.31	0.22	0.15
	Jmax (A/cm^2)—wire (at 105°C)	2.70E+06	3.30E+06	3.90E+06
	Imax (mA)—via (at 105°C)	0.1	0.07	0.04
	Local wiring pitch (nm)	105	75	50
	Local A/R (for Cu)	1.8	1.9	2
Add	Interconnect RC delay 1 mm line (ps)	565	970	2008
Add	Line length where τ = RC delay (µm)	26	15	9
	Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	5	4	3
	Intermediate wiring pitch (nm)	135	95	65
	Intermediate wiring dual Damascene A/R (Cu wire/via)	1.8/1.6	1.9/1.7	2.0/1.8
Add	Interconnect RC delay 1 mm line (ps)	348	614	1203
Add	Line length where τ = RC delay (µm)	33	19	11
	Cu thinning at minimum intermediate pitch due to erosion (nm), 10% ´ height, 50% areal density, 500 µm square array	12	9	7
	Minimum global wiring pitch (nm)	205	140	100
Add	Ratio range(global wiring pitches/intermediate wiring pitch)	1.5 - 10	1.5 - 13.0	1.5 - 16
	Global wiring dual-Damascene A/R (Cu wire/via)	2.3/2.1	2.4/2.2	2.5/2.3
Add	Interconnect RC delay 1 mm line (ps) at minimum pitch	131	248	452
Add	Line length where τ = RC delay (µm) minimum pitch	54	30	19
Delete	~~Cu thinning global wiring due to dishing and erosion (nm), 10% ´ height, 80% areal density, 15 mm wide wire~~	~~24~~	~~17~~	~~13~~
Add	Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% areal density	155	148	130
	Cu thinning global wiring due to dishing (nm), 100 µm wide feature	14	10	8
	Conductor effective resistivity (µΩ-cm) Cu intermediate wiring	2.2	2.2	2.2
	Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3]	5	3.5	2.5
	Interlevel metal insulator—effective dielectric constant (κ)	2.1	1.9	1.8
	Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ)	<1.9	<1.7	<1.6

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Table 63a DRAM Interconnect Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
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	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
	Number of metal levels	**3**	**3–4**	**4**	**4**	**4**	**4**	**4**
Was	Contact A/R—stacked capacitor	**11.4**	**11.9**	**12.4**	**13**	**13.6**	**14.3**	**15.2**
Is	Contact A/R—stacked capacitor	**11**	**12**	**13**	**15**	**15**	**16**	**16**
	Local wiring pitch (nm) non-contacted	**260**	**230**	**200**	**180**	**160**	**150**	**130**
Was	Specific contact resistance (Ω-cm^2)	**1.50E-07**	**1.30E-07**	**1.00E-07**	**8.00E-08**	**7.00E-08**	**6.00E-08**	**5.00E-08**
Is	Specific contact resistance (Ω-cm^2)	**1.7E-07**	**1.4E-07**	**1.0E-07**	**8.5E-08**	**7.0E-08**	**5.0E-08**	**4.0E-08**
Was	Specific via resistance (Ω-cm^2)	**2.00E-09**	**1.40E-09**	**1.00E-09**	**9.00E-10**	**7.00E-10**	**6.00E-10**	**5.00E-10**
Is	Specific via resistance (Ω-cm^2)	**2.0E-09**	**1.5E-09**	**1.1E-09**	**9.0E-10**	**7.5E-10**	**5.8E-10**	**5.0E-10**
	Conductor effective resistivity (μΩ-cm)	**3.3**	**3.3**	**3.3**	**2.2**	**2.2**	**2.2**	**2.2**
	Interlevel metal insulator—effective dielectric constant (κ)	**4.1**	**3.0–4.1**	**3.0–4.1**	**3.0–4.1**	**3.0-4.1**	**2.6–3.1**	**2.6–3.1**

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Table 63b DRAM Interconnect Technology Requirements—Long-term

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	DRAM ½ Pitch (nm)	*45*	*32*	*22*
	MPU/ASIC ½ Pitch (nm)	*45*	*32*	*22*
	MPU Printed Gate Length (nm)	*25*	*18*	*13*
	MPU Physical Gate Length (nm)	*18*	*13*	*9*
	Number of metal levels	**4**	**4**	**4**
Was	Contact A/R—stacked capacitor	**16.1**	**19.3**	**23.2**
Is	Contact A/R—stacked capacitor	**> 20**	**> 20**	**> 20**
	Local wiring pitch (nm) non-contacted	**90**	**64**	**44**
Was	Specific contact resistance (Ω-cm^2)	**4.00E-08**	**2.00E-08**	**1.00E-08**
Is	Specific contact resistance (Ω-cm^2)	**2.3E-08**	**1.2E-08**	**5.5E-09**
Was	Specific via resistance (Ω-cm^2)	**5.00E-10**	**3.00E-10**	**1.00E-10**
Is	Specific via resistance (Ω-cm^2)	**3.2E-10**	**1.6E-10**	**7.6E-11**
	Conductor effective resistivity ($\mu\Omega$-cm)	**2.2**	**2.2**	**2.2**
	Interlevel metal insulator—effective dielectric constant (κ)	**2.3–2.7**	**2.3–2.7**	**2.1**

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