

# GLOSSARY

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## KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

### CHARACTERISTICS OF MAJOR MARKETS

*Technology Node*—The ground rules of process governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. For logic, such as microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first polysilicon or metal layer and lags behind DRAM half-pitch, which may also refer either first layer metal or polysilicon. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology node step represents the creation of significant technology progress—approximately 70% of the preceding node, 50% of two preceding nodes. Example: DRAM half pitches of 180, 130, 90, 65, 45, 32 nm, and 22 nm. For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

*Moore's Law*—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a “self-fulfilling” prophecy, “Moore's Law” has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

*Cost-per-Function Manufacturing Productivity Improvement Driver*—In addition to Moore's Law, there is a historically-based “corollary” to the “law,” which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every two years, as suggested by consensus DRAM and MPU models of the 1999 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

*Affordable Packaged Unit Cost/Function*—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market “top-down” needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

*DRAM Generation at (product generation life-cycle level)*—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

*MPU Generation at (product generation life-cycle level)*—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

*Cost-Performance MPU*—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1Mbytes/2001). Logic functionality and L2 cache typically double every two-year generation.

*High-performance MPU*—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example 2@ 25Mt cores in 2001) with a large (example 4Mbyte/2001) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two-year generation by doubling the number of on-chip CPU cores and associated memory.

*Product inTER-generation*—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore’s Law ( $2\times$ /two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is  $-29\%$  per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology-node scaling ( $.7\times$  linear,  $.5\times$  area) is every three years, an additional device/process design improvement of  $.8\times$  per two years must be achieved. This requirement represents a design-related (cell-area-factor) area-reduction improvement of at least  $-11\%$  per year, and this design-related productivity improvement is in addition to the basic lithography-based area reduction of  $-21\%$  per year (three-year node cycle). The present 2001 ITRS consensus target for the rate of increase of DRAM is  $2\times$ /chip every two years. However, the 2001 ITRS forecast of cell-area-factor improvement is only  $-7\%$  per year on average. This results in an average DRAM inTER-generation chip-size growth of  $4.5\%$ /year or about  $1.2\times$  every four years. Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the 2001 ITRS MPU inTER-generation functionality model target is  $2\times$  transistors/chip every technology node, in order maintain a flat chip size growth throughout the roadmap period.

*Product inTRA-generation*—Chip size shrink trend within a given constant functions-per-chip product generation. The 2001 ITRS consensus-based model targets reduce chip size (by shrinks and “cut-downs”) utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus  $50\%$  per technology node.

*Year of Demonstration*—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration-level manufacturing tools and processes. Historically, DRAM products have been demonstrated at  $4\times$  bits-per-chip every three years at the leading-edge process technology node, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be “stitched” together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2003 Production-level targets.

*Year of INTRODUCTION*—Year in which the leading chip manufacturer supplies small quantities of engineering samples ( $<1K$ ). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at  $2\times$  functionality per chip every two years (every technology node, in the case of MPUs). In addition, manufacturers will delay production until a chip-size shrink or “cut-down” level is achieved which limits the inTER-generation chip-size growth to be flat, or at the most,  $1.2\times$  every four years.

*Year Of PRODUCTION*—Year in which leading chip manufacturers begin shipping volume quantities ( $10K$ /month) of product manufactured with qualified production tooling and processes and is followed within three months by a second manufacturer. As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly “copied” into multiple modules of manufacturing capacity. For high-demand products, volume production typically continues to ramp to fab design capacity within 12 months. Alpha-level manufacturing tools and research technology papers are typically delivered 24 months prior to volume production ramp. Beta-level tools are typically delivered 12 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1Gb/production, 4G/introduction, plus 512Mb/256Mb/128Mb/64Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

*Functions/Chip*—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

*Chip Size (mm<sup>2</sup>)*—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the *ITRS* consensus models).

*Functions/cm<sup>2</sup>*—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the *2001 ITRS*, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

*DRAM Cell Array Area Percentage*—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 55% at the production level, and less than 50% at the ramp level).

*DRAM Cell Area (μm<sup>2</sup>)*—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified *ITRS*-consensus Cell Area Factor target (A) times the square of the minimum half-pitch feature (f) size, that is:  $C = Af^2$ . To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C<sub>AVE</sub>) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is:  $C_{AVE} = C/E$ . The total chip area can then be calculated by multiplying the total number of bits/chip times the C<sub>AVE</sub>. Example: 1999: A=8; square of the half-pitch,  $f^2 = (180 \text{ nm})^2 = .032 \text{ μm}^2$ ; cell area,  $C = Af^2 = 0.26 \text{ μm}^2$ ; for 1Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the  $C_{AVE} = C/E = 0.37 \text{ μm}^2$ ; therefore, the 1Gb Chip Size Area =  $2^{30} \text{ bits} * 0.37 \text{ e-6 mm}^2/\text{bit} = 397 \text{ mm}^2$ .

*DRAM Cell Area Factor*—A number (A) which expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, 1.6×1.6=2.5, etc.).

*SRAM Cell Area Factor*—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

*Logic Gate Cell Area Factor*—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

*Usable Transistors/cm<sup>2</sup> (High-performance ASIC, Auto Layout)*—Number of transistors per cm<sup>2</sup> designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

## **CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES**

*Number of Chip I/Os—Total (Array) Pads*—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

*Number of Chip I/Os—Total (Peripheral) Pads*—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

*Pad Pitch*—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

*Number of Package Pins/Balls*—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

*Package Cost (Cost-performance)*—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

### **CHIP FREQUENCY (MHZ)**

*On-Chip, Local Clock, High-Performance*—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

*Chip-To-Board (Off-chip) Speed (High-Performance, Peripheral Buses)*—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

### **OTHER ATTRIBUTES**

*Lithographic Field Size (mm<sup>2</sup>)*—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

*Maximum Number of Wiring Levels*—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

### **FABRICATION ATTRIBUTES AND METHODS**

*Electrical D<sub>0</sub> Defect Density (d/m<sup>-2</sup>)*—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

*Minimum Mask Count*—Number of masking levels for mature production process flow with maximum wiring level (Logic).

### **MAXIMUM SUBSTRATE DIAMETER (MM)**

*Bulk or Epitaxial or Silicon-on-Insulator Wafer*—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

### **ELECTRICAL DESIGN AND TEST METRICS**

#### **POWER SUPPLY VOLTAGE (V)**

*Minimum Logic V<sub>dd</sub>*—Nominal operating voltage of chips from power source for operation at design requirements.

*Maximum Power High-performance with Heat Sink (W)*—Maximum total power dissipated in high-performance chips with an external heat sink.

*Battery (W)*—Maximum total power/chip dissipated in battery operated chips.

### **DESIGN AND TEST**

*Volume Tester Cost/Pin (\$K/pin)*—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

### **Add**

### **TECHNOLOGY REQUIREMENTS SOLUTIONS**

**“Interim Solutions are Known”— Limitations of available solutions will not delay the start of production. In some cases, work-arounds will be initially employed. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity.”**

### *Contact Information for the ITRS*

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