

# 2002 UPDATE TABLES

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## DESIGN

*Table 13 Design Difficult Challenges*

<i>Difficult Challenges</i>	<i>Summary of Issues</i>
Productivity	To avoid exponentially increasing design cost, overall productivity of designed functions on chip must scale at $> 2\times$ per node. Reuse productivity (including migration) of design, verification and test must also scale at $> 2\times$ per node.
Power	Non-ideal scaling of planar CMOS devices, together with the roadmap for interconnect materials and package technologies, presents a variety of challenges related to power management and current delivery.
Manufacturing Integration	“Red bricks”—technology requirements for which no known solutions exist—are increasingly common throughout the <i>ITRS</i> . On the other hand, challenges that are impossible to solve within a single technology area of the <i>ITRS</i> may be solvable (more cost-effectively) with appropriate intervention from, or partnership with, DT. Feasibility of future technology nodes will come to depend on such “sharing of red bricks.”
Interference	Resource-efficient communication and synchronization, already challenged by global interconnect scaling trends, are increasingly hampered by noise and interference. Prevailing signal integrity methodologies in logical, circuit and physical design, while apparently scalable through the 100 nm node, are reaching their limits of practicality.
Error Tolerance	Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test. Such a paradigm shift is likely forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.

## OVERVIEW

The Design ITWG has not changed any tables in either the Design or Systems Drivers chapters for the 2002 update. One figure has been updated in the System Drivers chapter, as described below. The remainder of this update describes planned changes (New Material, and Improvements and Corrections to Existing Material) for the 2003 renewal.

For the 2003 renewal, the Design ITWG anticipates continued emphasis on core messages: (1) the increasing level of risk that design cost and design quality present to continuation of the semiconductor industry roadmap; (2) the role of Design Technology in reducing overall cost and risk of future *ITRS* nodes by “sharing red bricks” with other technologies; (3) the role of Design Technology as the semiconductor industry’s interface to systems and applications markets; and (4) the need for continued identification of interdependencies between *ITRS* technologies, so as to create a more well-linked, “living roadmap.” Improvements to the System Drivers chapter, in collaboration with other ITWGs, are also anticipated.

## SYSTEM DRIVERS CHAPTER

### New Material

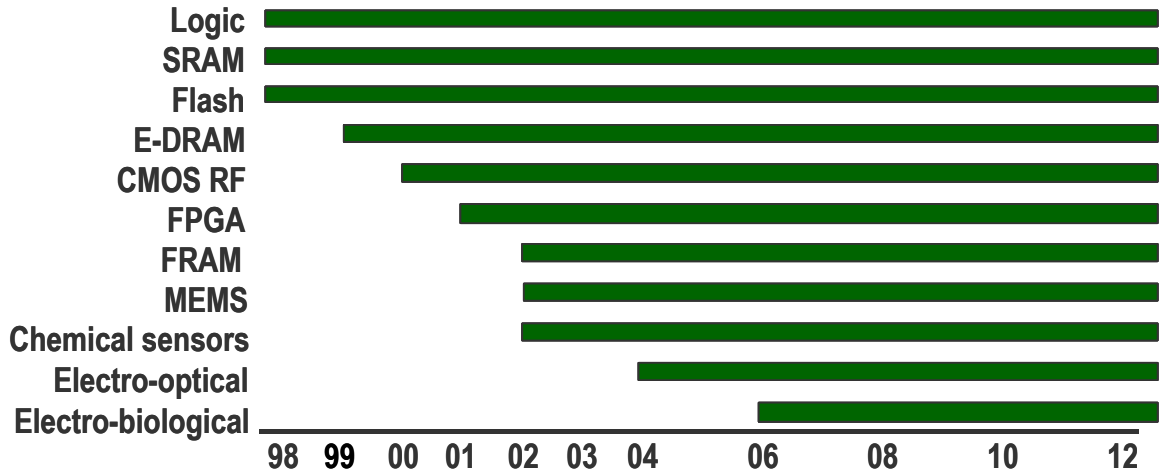
The following new material is being developed toward the 2003 renewal.

- Models, figures of merit, and discussion of embedded and standalone memories.
- Models, figures of merit, and discussion of a DSP subcategory for processors.

### Improvements and Corrections to Existing Material

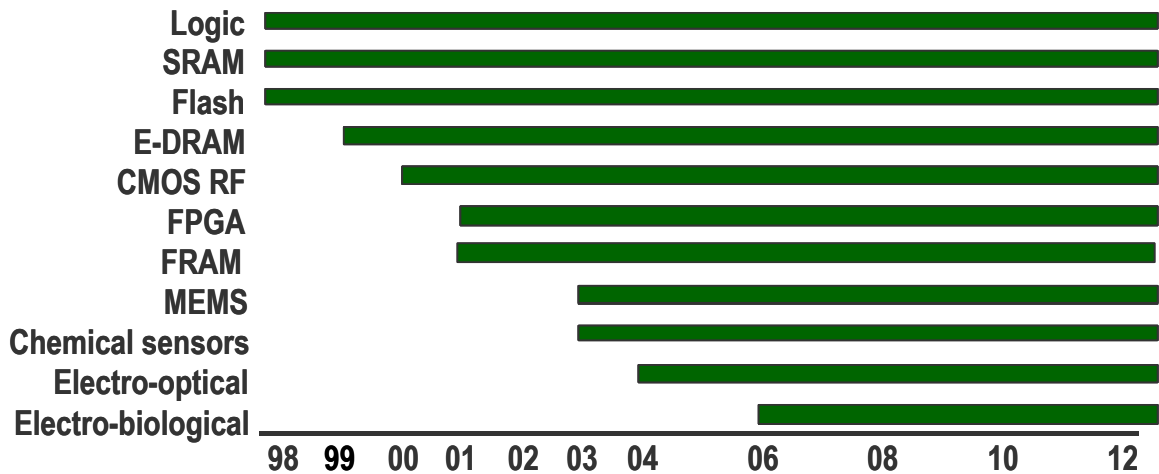
The SOC-MT integration roadmap (Figure 10) has been reviewed for accuracy of its timeline, as well as economic constraints and multi-die system-in-package integration alternatives. Three changes have been made to Figure 10 from the 2001 ITRS.

- (1) Since FRAM was integrated from 2001, the FRAM starting point has been shifted earlier by one year.
- (2) MEMS have not yet been integrated with CMOS in 2002. While there are products in which MEMS and CMOS are integrated, the quantity of CMOS logic is not large enough to call these products systems. Therefore, the starting point for MEMS integration has been delayed by one year.
- (3) Chemical sensors have not yet been integrated with SOC in 2002. Therefore, the starting point for integration has been delayed by one year.



Was

Figure 10 First Integration of Technologies on SOC with Standard CMOS Process



Is

Figure 10 First Integration of Technologies on SOC with Standard CMOS Process

- Table 11 and the corresponding PIDS table will be reconciled, and subthreshold current projections reassessed, in collaboration with the PIDS ITWG.

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- The SOC-LP low-power PDA model will be reviewed for potential clarification of several attributes: (1) mixed-signal content, (2) performance demand in out years, (3) device (HP, LOP, LSTP) and memory (SRAM, eDRAM) composition, (4) technology baseline (2001 ITRS), (5) die size, and (6) assumed battery technology.
- Whether to define a distinct technology that explicitly supports low-cost, low-metal layer count blocks (driven by cost and integrability) will be discussed with other ITWGs.
- Off-chip signaling bandwidths and package pin counts will be reviewed in collaboration with the Test ITWG and the Assembly and Packaging ITWG.
- The MPU model will be reviewed for clarification of low-power requirements.
- Overall, the System Drivers chapter will undergo an SOC-centered reorganization, which will provide a unifying context for various types of blocks and fabrics: processor, memory, and mixed-signal.

## DESIGN CHAPTER

### New Material

The following new material is being developed toward the 2003 renewal.

- Standalone analog and circuits content.
- Metrics for design technology: cost/value = ROI, quality (e.g., ASIC vs. full-custom), and design productivity.
- Additional discussion of silicon-on-insulator technology.
- Additional discussion of single-event upset (soft error rate) and other reliability challenges.

### Improvements and Corrections to Existing Material

The following improvements are under way toward the 2003 renewal.

- The SOC design cost model presentation will be reviewed for improved clarity, and all regions will collaborate on calibration versus recent design projects.
- Increased discussion of roadmaps for “design system architecture” will be considered.
- The Design chapter sections and organization will be reviewed for opportunities to increase and highlight standalone analog / mixed-signal content, to complement the addition of new analog material.
- Other improvements to existing material extend beyond the scope of the Design chapter. For example, (1) an updated definition of logic node (as opposed to DRAM node) arrival may be needed in the 2003 renewal, given the rapid divergence of half-pitch and minimum feature size; (2) future back end of line (BEOL) interconnect architecture and technology requirements may require joint specification by the Design and Interconnect ITWGs; and (3) application domain, cost, manufacturability and testability may together require joint specification of off-chip signaling speeds, system power limits, and other requirements by the Design, Assembly and Packaging, PIDS and Test ITWGs.