

# PIDS TWG Report on the ITRS Roadmap issues July 10, 2000 Participants

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International Technology Roadmap for Semiconductors

*July 11, 2000 Work In Progress Not for Publication*

# Contributors to the PID&S TWG 2000

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## Outline:

- **One Year Gate Pull-In Discussion and Recommendation**
- **Review Tables and Updates**
- **Recommendations for 2001 effort**
- **Review New Structures Table**



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One year acceleration proposal increases need for gate oxide solutions

Grey rows show effect of one year pull-in

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
1	DRAM 1/2 Pitch (nm)	180	165	150	130	120	110	100	
2	MPU Gate Length (nm)	140	120	100	85-90	80	70	65	
NEW	MPU Physical Gate Length	120	100	90	80	70	65	60	
3	MPU/ ASIC 1/2pitch (nm)	230	210	180	160	145	130	115	
4	ASIC Gate Length (nm)	180	165	150	130	120	110	100	
5 WAS	Minimum logic Vdd (V) (desktop)	1.5-1.8	1.5-1.8	1.2-1.5	1.2-1.5	1.2-1.5	0.9-1.2	0.9-1.2	M GATE
5 IS	Minimum logic Vdd (V) (desktop)	1.5-1.8	1.2-1.5	1.2-1.5	1.2-1.5	0.9-1.2	0.9-1.2	0.8-1.1	
6 WAS	Tox equivalent (nm)	1.9-2.5	1.9-2.5	1.5-1.9	1.5-1.9	1.5-1.9	1.2-1.5	1.0-1.5	M GATE
6 IS	Tox equivalent (nm)	1.9-2.5	1.5-1.9	1.5-1.9	1.5-1.9	1.2-1.5	1.0-1.5	?	M GATE
7 WAS	Nominal Ion at 25 °C (μA/μm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	M GATE
7 IS	Nominal Ion at 25 °C (μA/μm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	M GATE
8 WAS	Maximum Ioff at 25 °C (nA/μm) (For minimum L device) high performance	5	7	8	10	13	16	20	M GATE
8 IS	Maximum Ioff at 25 °C (nA/μm) (For minimum L device) high performance	7	8	10	13	16	20	25	M GATE
9 WAS	Gate delay metric CVI (ps) high-performance	11	9.4	8.6	7.3	6.9	6.1	5.7	
9 IS	Gate delay metric CVI (ps) high-performance	9.4	8.6	7.3	6.9	6.1	5.7		
10 WAS	Percent static power reduction necessary due to innovative circuit/system design	0	33	48	55	71	77	81	M GATE M & A 1/2
10 IS	Percent static power reduction necessary due to innovative circuit/system design	33	48	55	71	77	81		M GATE M & A 1/2
11	Nominal Ion at 25 °C (μA/μm) [NMOS/PMOS] low power	490/230	490/230	490/230	490/230	490/230	490/230	490/230	A GATE
12 WAS	Maximum Ioff at 25 °C (pA/μm) (For minimum L device) low power	5	7	8	10	13	16	20	A GATE



# One Year Gate Pull-In Recommendation

- 1 year pull-in creates too many issues for gate dielectrics between 2001-2003
- Recommend 2000 column to use 2001 numbers with note indicating that 2001-2004 numbers need much work for the 2001 ITRS



# One year acceleration proposal for 2000 Only

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
1	DRAM 1/2 Pitch (nm)	180	165	150	130	120	110	100	
2	MPU Gate Length (nm)	140	120	100	85-90	80	70	65	
<b>NEW</b>	MPU Physical Gate Length	120	100	90	80	70	65	60	
3	MPU/ ASIC 1/2pitch (nm)	230	210	180	160	145	130	115	
4	ASIC Gate Length (nm)	180	165	150	130	120	110	100	
5 <b>WAS</b>	Minimum logic Vdd (V) (desktop)	1.5-1.8	1.5-1.8	1.2-1.5	1.2-1.5	1.2-1.5	0.9-1.2	0.9-1.2	M GATE
5 <b>IS</b>	Minimum logic Vdd (V) (desktop)	1.5-1.8	1.2-1.5	1.2-1.5	1.2-1.5	0.9-1.2	0.9-1.2	0.8-1.1	
6 <b>WAS</b>	Tox equivalent (nm)	1.9-2.5	1.9-2.5	1.5-1.9	1.5-1.9	1.5-1.9	1.2-1.5	1.0-1.5	M GATE
6 <b>IS</b>	Tox equivalent (nm)	1.9-2.5	1.5-1.9	1.5-1.9	1.5-1.9	1.2-1.5	1.0-1.5	?	M GATE
7 <b>WAS</b>	Nominal Ion at 25 °C (μA/μm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	M GATE
7 <b>IS</b>	Nominal Ion at 25 °C (μA/μm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	M GATE
8 <b>WAS</b>	Maximum Ioff at 25 °C (nA/μm) (For minimum L device) high performance	5	7	8	10	13	16	20	M GATE
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10 <b>WAS</b>	Percent static power reduction necessary due to innovative circuit/system design								M GATE M & A 1/2
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11	Nominal Ion at 25 °C (μA/μm) [NMOS/PMOS] low power	490/230	490/230	490/230	490/230	490/230	490/230	490/230	A GATE
12 <b>WAS</b>	Maximum Ioff at 25 °C (pA/μm) (For minimum L device) low power	5	7	8	10	13	16	20	A GATE



## Near Term Issues:

- No gate dielectric available for <65nm devices
- Meeting device requirements at Low  $V_{DD}$
- Management of reliability issues with many new materials
- Need for precision passive elements



# PIDS Update Summary

- 2000 ITRS Table 28, 29, and 30 updates
  - Mainly minor updates, correction--*EXCEPT FOR 1-YEAR PULL IN ISSUES*
- Key issues for 2001
  - Logic and memory
    - Review ASIC gate length
    - Dynamic, circuit implications of gate leakage on logic
    - Review gate sheet resistance with Design
    - Review Vdd, Tox
    - Review low power spec's, perhaps add wireless
    - DRAM cell size, Tox dependent on IRC chip size, chip storage area decisions
  - Analog
    - General review to understand process/integration issues
  - Reliability
    - Review possible burn-in requirements and SOC requirements
- Novel devices table: what to do with it?



# PIDS Cross-TWG Meetings

- **Strong interest in novel device impact**
- **General: cross-TWG issues important**
- **Design**
  - 2001: Static power dissipation is important unresolved issue: impacts systems, devices, and gate stack module
  - 2001: Strong interaction on circuit and system issues needed
- **Modeling & simulation**
  - 2001: gate stack and SOC modeling important
- **FEP**
  - Strong joint efforts needed and planned
    - Flash
    - Expanded logic low power requirements
    - FERAM
- **Interconnect**
  - Minor adjustment of shortwire pitch
  - Important joint issues with high K coupling, bypass, and other cap's



PIDS&FEP Meeting at VLSI Symp. 2000 (June 15,  
Honolulu)

Attendants: J.Y. Sun (TSMC), C.S.Wang(TSMC), G. Badenes (IMEC), L.C.Tran(Micron), T.Sugii(Fujitsu), J.Ida(Oki), K.Shibahara(HiroshimaUniv.)M.Yoshimi(Toshiba), S.Kawamura (Fujitsu), Otuka(Oki), M.Niwa(Matsushita)

Discussed:

1. ORTC Matters
  - (1) Technology node definition
  - (2) MPU gate length x 0.9
  - (3) DRAM chip size model

---Explained Japanese TWG's view



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# PIDS&FEP Meeting at VLSI Symp. 2000 (June 15, Honolulu)

## 2. Confirmation of new activities in 2001 ITRS

Making Roadmap rows for:

- (1) Flash (EU / Taiwan)
- (2) FeRAM (Japan / Taiwan)
- (3) Gate dielectrics in Low Stand-by Power and Low Operational Power Applications (Japan)
- (4) MRAM (US?) ---- Proposed



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# Novel Devices Table

## “New for 2000”

- “MOS” are MOS type devices
- “Novel devices” are electronic devices, but beyond MOS type
- “Novel storage” are novel storage devices
- “New systems” are new systems, requiring novel architectures



# Non - Bulk MOS Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
SOI (PD)	180	Low power especially. Performance.	OK	OK	Low power, high speed, low voltage operation, reduced SER	Cost, Dynamic body charge
SOI (FD)	130	“	“	“	Low power, high speed, low voltage operation, reduced SER	Cost, Control of very thin Si layer
Multi-value logic	≤100	Cost	Very difficult	Difficult	Density	Vt control, speed.
Dynamic Vt logic (gate tied to body)	≤100 (0.6V restriction on Vdd drives this choice.)	“	“. (Note: 0.6V restriction on Vdd is less than ITRS's Vdd for 100 nm node.)	“	High speed @ relatively low power	Cost, Junction leakage. Restricted to Vdd≤0.6 V. For bulk, isolation is an issue.
Vertical MOSFET	≤130 (DRAM) ≤70 (logic)	Performance	Issues. (Only one Lg =>no good for analog.)	Difficult issues	Litho independence, high Idrive	Processing, Process integration. Standard CMOS needed on same chip.
Double Gate SOI	≤ 70	Performance	“	Difficult issues	Improved short channel, high Idrive	Cost, how to fabricate self-aligned double gate
Epi channels, including SiGe	≤70	Performance	OK	OK	High mobilities for electrons and holes	Process complexity, novel materials and processes
Delta-Type MOSFET	≤70	Performance	OK	Difficult issues	Performance, improved	Process complexity



# Novel Logic Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
MEMS	100 (dependent on solving difficult problems, not on 100 nm node CDs)	-Cost, Sys on Chip (RF resonators, imaging, sensors) -ULSI switching (open and close) -Microelectronic chem. sensors	Difficult issues	Difficult issues	Great SOC flexibility, possible speed, lower power, and low crosstalk (optical interconnect)	Integration of MEMS and Si systems; reliability
Resonant Tunneling IC	≤35	Performance, RF	Difficult issues	Difficult issues	Density, performance, RF	Entirely new IC device
3D Stack Structures	≤35	Cost, power	Issues, especially with interconnect	Difficult Issues	Very high density & Short interconnects	Process complexity, Heat dissipation
Organic Transistors (could be on plastic substrate)	<35	cost, power	Difficult issues	Difficult Issues	Cost, power	Entirely new IC device. Temperature limitations during processing
CHINTS (chan. hot electron injection transistor)	<35	Performance, power	Difficult issues	Issues	Density, power, performance (multi-value logic)	Entirely new IC device
Carbon Nanotube transistor	<35	Performance, power	Difficult issues	Difficult issues	Density, power	New device & system



# Novel Logic Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
Single Electron Transistor	$\leq 35$	Cost	Difficult issues	Difficult issues	Density	New devices & system, Room temp operation questionable, noise (offset charge). Lack of drive current



# Novel Storage Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
FERAM	180	Cost, performance for nonvolatile	OK	OK	high capacitance, nonvolatile, low voltage and power (nonvolatile)	Cost, fab., reliability, esp. for highly scaled technology
Multi level Flash	180	Cost	OK	OK	High density - ==>cost reduction	Accurately placing charge on gate, process control, material and reliability
MRAM	≤ 100	Cost	Issues	Difficult issues	Density, power, performance, nonvolatility	Reliability and integration. Material quality.
Quantum Dot Memories, including Single Electron	<35	Cost	Difficult issues	Difficult issues	Density, power, , nonvolatile capability	New device & system. Room temperature operation difficult.



# Novel Systems Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
Cryoelectronics, esp. device optimization for reduced temp. operation	180 (modest cooling); ≤50 (≤ liq. nitrogen temp.)	Performance	OK (180 nm) -Packaging and cooling issues	Some issues	Speed, Power	<b>Cost</b>
Molecular Electronics	<35	Cost	Difficult issues	Difficult issues	Density	Entirely new device, system.
DNA and Biological Computing	<35	Cost, performance	Difficult issues	Difficult issues	Density, power, performance	Entirely new device, systems
Quantum Computing -Spin State Structures - Tunneling Phase Logic	<35	Performance, power	Difficult issues	Difficult issues	Density, power, performance	Entirely new device, system (NMR readout?)
Quantum devices: Josephson Junction Tunneling devices	<35	Performance	Difficult issues	Difficult issues	Speed and relatively low power	Entire new device, system. Room temp. operation.
All-optical integrated computing and swithing	<35	Performance	Difficult issues	Difficult issues	Performance crosstalk reduction	Entirely new device and system.



## Summary:

- **One year gate pull-in recommendation made**
- **Minor updates for tables**
- **Recommendations for 2001 effort**
- **New structures table presented**

