Modeling and Simulation TWG

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Modeling and Simulation TWG:
Scope

Topical Areas

- Equipment/Topography Modeling
- Lithography Modeling
- Front End Process Modeling
- Numerical Device Modeling
- Circuit Element Modeling
- Package Modeling
- Numerical Methods and Algorithms

Developers

- Universities
- Laboratories (government, industry)
- CAD Vendors

Strategy

Adequate research funds for universities and laboratories are indispensable, because new modeling capability requires long-range research.

Modeling and Simulation TWG:
Key Messages

- High frequency circuit models
- Models to reduce cross-die variation (OPC, CMP, equipment modeling)
- Model alternative lithography technology tradeoffs
- Gate stack modeling for ultra-thin/alternative dielectrics
- Modeling limits of MOS; models for innovative MOS and beyond
- Goals for cost reduction due to TCAD

Difficult Challenges:

High frequency circuit modeling (>1GHz)

DIFFICULT CHALLENGES ³100 nm / THROUGH 2005	*SUMMARY OF ISSUES*
High frequency circuit modeling (>1GHz)	Efficient simulation of full-chip interconnect delay High frequency circuit models including non-quasi-static, gate RLC, substrate noise, QM effects Accurate 3-D interconnect model; inductance effects
Modeling of ultra-shallow junctions	Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge Interface effects on point defects and dopants Activation models (In, As, B) Implant damage, amorphization, re-crystallization
Package models	Unified package/chip-level circuit models Integrated treatment of thermal, mechanical, electrical effects
Equipment/topography modeling: cross-die, cross wafer thin film control	Reaction paths and rate constants Plasma models; linked equipment/feature models CMP (full wafer and die level) Pattern dependent effects
Lithography modeling	Resolution enhancement effects and mask synthesis (e.g., OPC, PSM) 248 vs 193 vs157 evaluation and tradeoffs Next-generation lithography system models
Reliability Simulation	Circuit and device level transistor reliability: oxide TDDB, hot carrier, electromigration, NVM reliability
Interconnect materials and interfaces	Electromigration (physical), grain structure, diffusion barriers, metallurgy
DIFFICULT CHALLENGES <100 nm / BEYOND 2005	*SUMMARY OF ISSUES*
Gate stack models for ultra-thin dielectrics	Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal) Predict epsilon, surface states, reliability, breakdown and tunneling from process conditions
Nano-scale device modeling	New device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.
Atomistic process modeling	Develop models to model processing steps at the atomic scale with atomic scale accuracy

•Efficient simulation of full-chip interconnect delay

•Accurate 3-D interconnect model; inductance effects

•High frequency circuit models including non-quasi-static, substrate noise, QM effects

- Efficient, accurate interconnect modeling critical for future high speed circuits

Difficult Challenges:

Unified Package/die-level models

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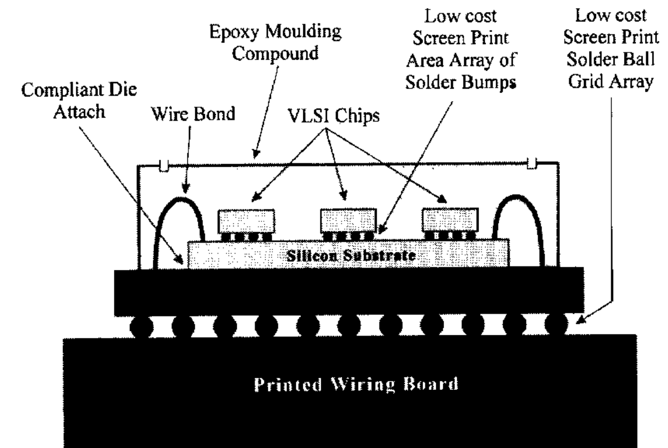
- **Unified package/chip-level circuit models**
- **Integrated treatment of thermal, mechanical, electrical effects**

- Packages becoming increasingly complex electrical devices
- High frequency interaction of package and die must be modeled together
- Thermo-mechanical effects must be understood
- Long-range: mixed electrical/optical analysis



Difficult Challenges:

Modeling of ultra-shallow junctions

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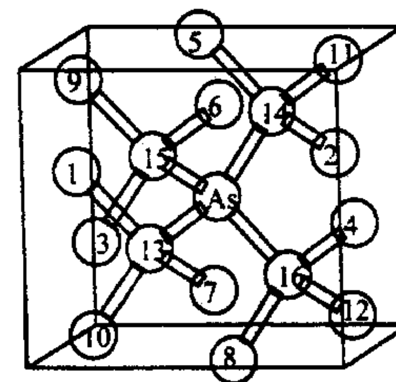
- **Diffusion parameters needed (e.g., from first principles calculations) for As, B, P, Sb, In, Ge**
- **Interface effects on point defects and dopants**
- **Activation models (In, As, B); metastable states**
- **Implant damage, amorphization, re-crystallization**

- Significant progress recently using <u>quantum calculations</u> for diffusion parameters
- <u>Interface</u> interactions dominate
  - ➢ Shallow junctions: all dopants are next to surface
- <u>Activation</u> issues become important
  - ➢ Scaled devices need low resistivity source/drain



Difficult Challenges: Equipment/topography modeling: Model thin film and etch control across die/wafer

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- **Reaction paths and rate constants**
- **Plasma models; linked equipment/feature models**
- **CMP (full wafer and die level)**
- **Pattern dependent effects**

•Within-die variation becoming key performance limiter; reduction is a source of performance gain

•300mm wafer transition imminent

Difficult Challenges:

Model Alternative Lithography Tradeoffs

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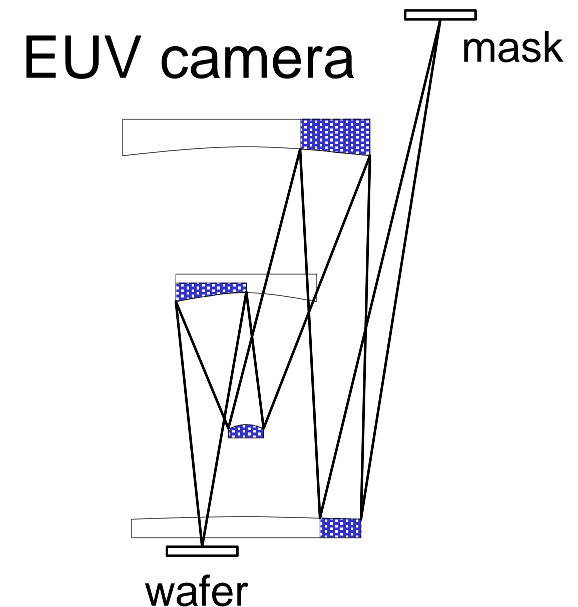
- **Resolution enhancement effects and mask synthesis (e.g., OPC, PSM)**
- **Predictive resist models**
- **248 vs 193 vs 157 evaluation and tradeoffs**
- **Next-generation litho system models**

- <u>Near term:</u> resolution enhancement techniques, OPC
- <u>Long term:</u> evaluation of competing Next Generation Litho approaches (EUV, Scalpel, …)



Difficult Challenges:

Reliability models for circuit design and technology development

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- **Circuit and device level transistor reliability: oxide TDDB, SER, hot carrier, electromigration,**
- **NVM reliability**
- **ESD, latchup**

- <u>Device level</u>: need predictive models for transistor reliability issues
- <u>Circuit level</u>: empirical models to guard-band designs

Difficult Challenges:

Gate stack modeling for ultra-thin dielectrics

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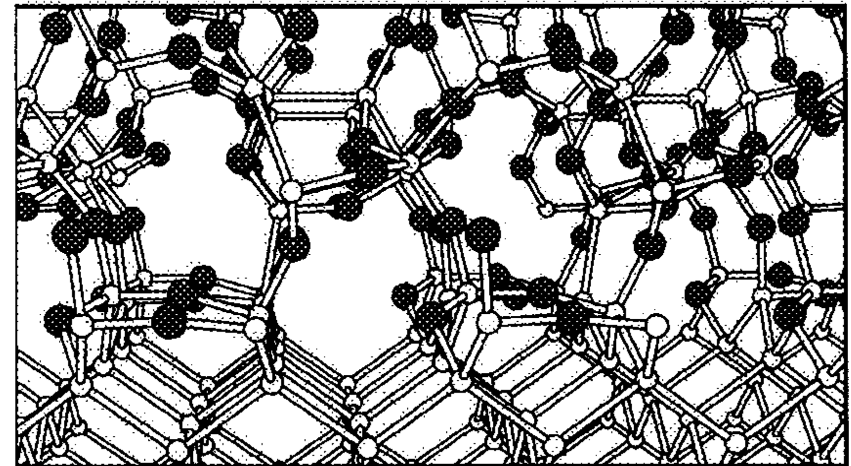
- **Electrical and processing models for alternate gate dielectrics, and alternate gate materials (e.g., metal)**
- **Model epsilon, surface states, reliability, breakdown and tunneling from process conditions**

- Detailed process modeling of gate dielectric to optimize the thinnest SiO2/SiO_xN_y systems, metal gate
- Modeling of alternative gate dielectric materials (atomic scale)
- Rigorous quantum treatment of gate stack



Simulated Si/SiO2 interface

(K. Ng, D. Vanderbilt, PRB 59 April 1999)

Difficult Challenges (beyond 2005):

Nano-scale device modeling

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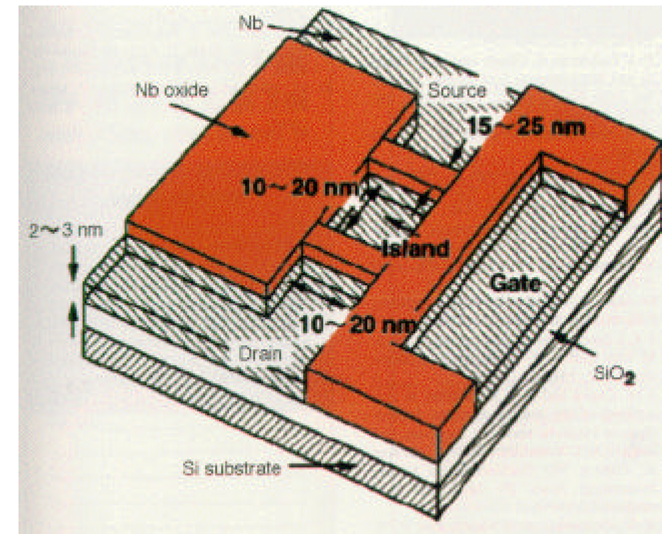
- **Model new device concepts (using quantum effect) beyond traditional MOS; single electron transistors, effect of single dopants, etc.**

- Possibility: scaling of traditional MOS device slows or ends

- Advanced research needed: exploration of innovative MOS concepts and devices beyond MOS

- Emphasize system performance modeling of new devices



Single electron transistor
(J. Shirakashi, ETL, Tsukuba)

Difficult Challenges (beyond 2005):

Atomistic process modeling

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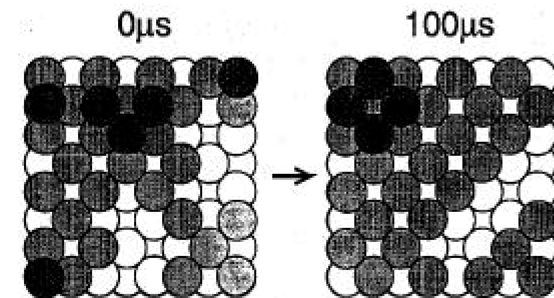
- **Develop models to model processing steps at the atomic scale with atomic scale accuracy**

- Whatever direction technology takes, manipulation of atomic layer dimensions needed near end of the roadmap.
- Development of theoretical, simulation and instrumental infrastructure should start now



Atomistic simulation of copper diffusion (A. Voter, LANL)

Technology Requirements: Cost Reduction

YEAR OF INTRODUCTION	1999 180nm	2000	2001	2002 130nm	2003	2004	2005 100nm	Driver
OVERALL COST REDUCTION TARGET (DUE TO TCAD)	20%			25%			35%	

- Goal of TCAD Technology Requirements: overall development cost reduction
- High volume 300mm wafer production in 2001: increased cost and fewer wafers for development
- Successful TCAD role in development of derivative processes
- More effort needed in predictive modeling, backend models

Technology Requirements:
Process TCAD (Accuracy)

YEAR OF INTRODUCTION	*1999* *180nm*	*2000*	*2001*	*2002* *130nm*	*2003*	*2004*	*2005* *100nm*	*Driver*
PROCESS TCAD								
Vertical and lateral junction depth simulation accuracy	**18nm (10%)**			**13nm (10%)**			**10nm (10%)**	
Total source/drain series resistance (accuracy)	**20%**			**20%**			**20%**	
Long-channel Vt (accuracy)	**3% (45-54mV)**			**3% (36-45mV)**			**3% (27-36mV)**	

- Thermal processes: lower temperature, shorter time
- Increased impact of interfaces, defects
- Experimental evaluation of dopant profiles still an issue
- Calibration is necessary for effective use

Technology Requirements:

Front End Process Modeling (Capabilities)

Short Term

YEAR OF INTRODUCTION	1999 180 NM	2000	2001	2002 130 NM	2003	2004	2005 100 NM
PROCESS TCAD							
Gate Stack: evaluate materials		**Model alternate dielectrics**		**Model metal vs. poly gate**			
Diffusion and activation coefficients		**Kinetics of diffusion and activation including interface interactions with point defects and dopants**					
Stress/extended defects		**Front end stress model**		**Extended defects and disloactions**			

Long Term

YEAR TECHNOLOGY NODEN	2008 70 NM	2011 50 NM	2014 35 NM
PROCESS TCAD			
Advanced process models	**Metastable activation (>solid solubility)**	**Alternative materials (e.g., SiGe)**	**Atomistic process model**
Advanced doping models	**Solid source**		

Atomistic-level models required for new gate materials
Point-defects issues still important
Extended defects to be modeled properly in view of mechanical stresses and generation/recombination of point defects

Technology Requirements:
Device Simulation (Accuracy)

YEAR OF INTRODUCTION	1999 180nm	2000	2001	2002 130nm	2003	2004	2005 100nm	Driver
DEVICE MODELING (NUMERICAL)								
Accuracy of ft at given ft (% of maximum chip frequency)	10%			10%			10%	
Gate leakage current accuracy (%) (decreases due to increase of Ig/Id)	100%			70%			40%	
Ioff accuracy	100%			70%			40%	
Vt rolloff accuracy (mV)	25mV			20mV			20mV	

- <20nm gate oxides increases importance of gate current modeling
- Off current modeling and cut-off frequency modeling remain important issues

Technology Requirements:

Device Modeling (Capabilities)

Short term

YEAR OF INTRODUCTION	1999 180 NM	2000	2001	2002 130 NM	2003	2004	2005 100 NM
NUMERICAL DEVICE MODELING							
Gate stack models		Gate current tunneling models			Full quantum gate stack models		
Reliability models		Transistor reliability models (gate oxide)			Interconnect reliability models (electromig., stress)		
Noise/variation		Dopant fluctuation			Noise models		

Long Term

YEAR TECHNOLOGY NODE	2008 70 NM	2011 50 NM	2014 35 NM
NUMERICAL DEVICE MODELING			
Alternative device models	2D quantum models for MOS	Single electron transistor	Quantum effect devices

- Quantum models needed for new gate stack materials
- Predictive models needed for reliablity issues: gate oxide (thinner oxide, new gate materials…), interconnects (electro/stress migration…)
- Smaller devices more susceptible to EMS

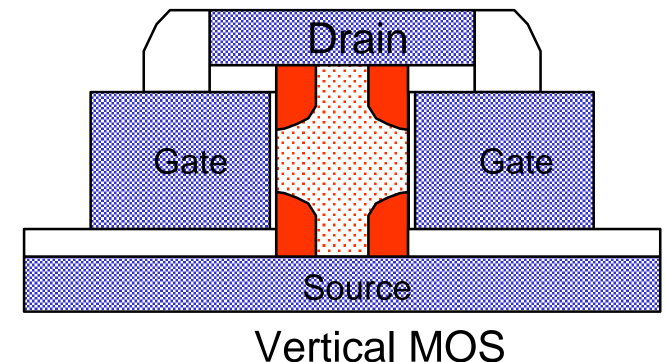
Long term device modeling

Modeling limits of MOS devices

- Noise margins
- Atomic-level fluctuations
- Reduction of yield due to statistical variation

Modeling for innovative MOS and beyond

- dual-gate MOS
- SOI
- vertical MOS
- quantum effect devices? Others?



Vertical MOS

Potential Solutions:

Interconnect models

First Year of IC Production: 1999, 2001, 2003, 2005, 2007, 2009, 2011, 2013, 2015

CIRCUIT ELEMENT MODELING

Interconnect models:
- Reduced order
- Transmission line
- Full EM Wave

Substrate models:
- Interconnect eddy currents
- Capacitative coupling
- Substrate current injection

DEVICE MODELING (NUMERICAL)

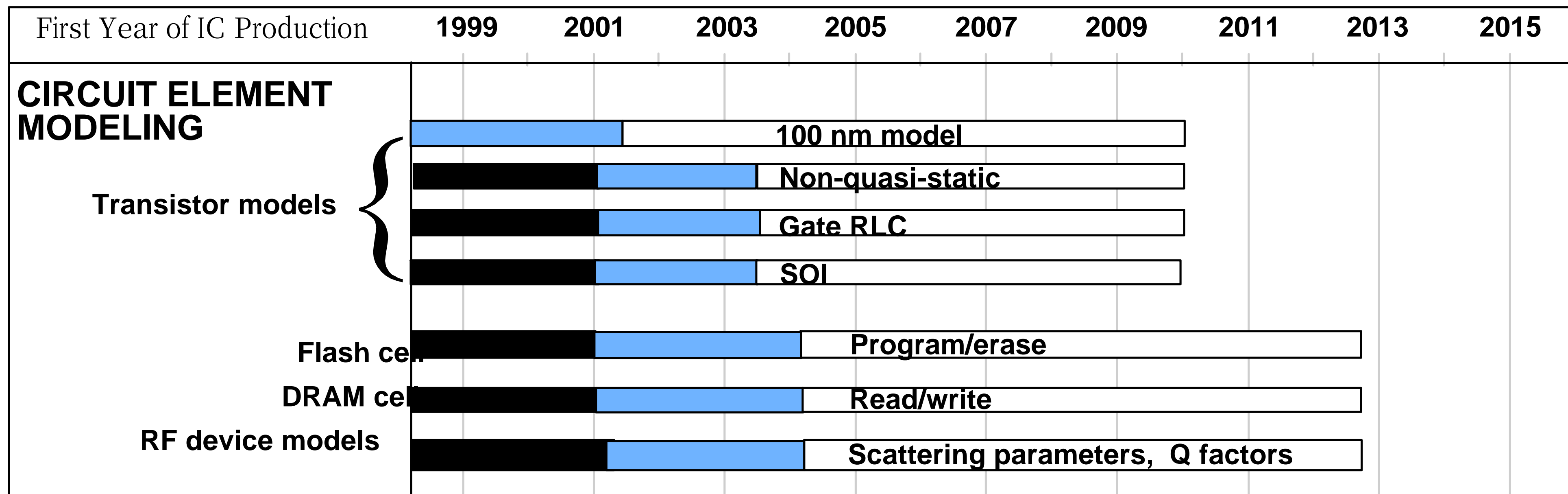
Interconnect models
- RLC, transmission line
- Full EM wave solutions

More accurate interconnect parasitic models are critical for high frequency design:

- Improved analytic capacitance models
  - 2D and 3D
  - cross-talk
- On-chip inductance modeling
  - substrate models
- Transmission line; full EM wave solvers

Potential Solutions:

Circuit models: Transistor, Device



- 100nm transistor model
- SOI models (floating body effect)
- Flash (program/erase)
- DRAM (read/write)
- RF device models:
  - active devices, passive devices

Potential Solutions:

Reliability modeling

First Year of IC Production	1999	2001	2003	2005	2007	2009	2011	2013	2015
Reliability modeling:									
Oxide TDDB Hot carrier Electromigration ESD, latchup									

Gate dielectric degradation (circuit, numerical)
Electromigration (circuit)
ESD, Latchup (circuit, numerical)
SER (circuit, numerical)
DRAM and logic
alpha and neutrons

Potential Solutions:
New ITWG Recommendations (2000)

- Equipment Modeling:

  Equipment suppliers should supply physical models and modeling information with equipment

- Device Modeling:

  Focus efforts on limits to MOS, and alternatives beyond MOS

  Increase modeling efforts in opto-electronics

- Circuit Modeling:

  Communication of process effects to designers (within-die variation, more detailed interconnect parasitics)

  Increased effort on industry standard circuit models

Summary

- Next two generations (130nm, 100nm) provide many modeling challenges:
  - High frequency circuit models (RLC, transistor)
  - Model cross-die variation due to litho, etch, thin film (e.g., OPC, CMP, equipment modeling)
  - Model lithography technology tradeoffs (resolution enhancement techniques, wavelength, PSM)
  - Goals for cost reduction due to TCAD
- Beyond 100nm, basic theoretical research needed:
  - Gate stack process and electrical model (atomic level)
  - Limits of MOS devices, innovative MOS devices and beyond
- University research funding necessary