Interconnect Working Group

Preview 2000
San Francisco, CA
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Agenda

- Review of 1999 difficult challenges
- Key issues
  - Technology Requirements
  - Potential Solutions
  - Other/unresolved
- Updated tables
- 2001 preview
- Summary

Typical Chip Cross-section of Hierarchical Scaling

Passivation
Dielectric
Etch Stop Layer
Dielectric Diffusion Barrier
Copper Conductor with Metal Barrier Liner
Pre Metal Dielectric
Tungsten Contact Plug

Wire
Via

Global
Intermediate
Local

Difficult Challenges

> 100 nm

- New materials
- Reliability
- Process integration
- Dimensional control
- Interconnect process with low/no device impact

<100 nm

- New materials and size effects
- Process integration
- Dimensional control
- Aspect ratios for fill and etch
- Solutions beyond copper and low k

Technology Requirement Issues

- Reliability requirements
- SoC global wiring pitch
- Usage of “Optional Levels”
- Planarization requirements
- Dielectric metrics including effective κ
- Is aggressive barrier thickness requirement (*i.e.* 0) needed for global wiring level - all 3 tables

Issue - reliability

- Ids *vs.* operating temperature - what temp to spec
  - 105 degrees C
- Via shape
  - Round
- AC or other operating conditions including pulse/width specs
  - Not completed
- Include "work" *i.e.* calculations
  - Appendix item
- Add back FITS/unit length

Issue - Optional Levels

- Further clarification of optional levels and role as bypass capacitor, ground plane and use for integrated MIM etc. elements.
  - Add text in appendix for MPU table - Optional Levels - use of ground planes and decoupling caps
  - Add in appendix for SOC table - Optional Levels - use of MIM caps, all passive elements

Issue - Planarization

- Issue - lack of consensus on metrics
  - Dishing metric eliminated from local and intermediate levels and replaced by thinning metric
  - Combined dishing and erosion metrics created for global levels
  - Global dishing in isolated features revised

Issue - OK Low k?

- Never-ending issue
  - Review effective κ range proposals from regions
    - done
  - Added adjacent requirement line which is the bulk κ value
  - Correctly verify κ needs against RC performance in ORTC table
    - deferred to 2001
    - Even if nodes are pulled in keep κ as listed in original year

MPU Near Term Years

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
MPU ½ pitch	230	210	180	160	145	130	115
MPU gate length (nm)	140	120	100	90	80	70	65
Number of metal levels	6-7	6–7	7	7–8	8	8	8–9
Number of optional levels—ground planes/capacitors	0	0	0	2	2	2	2
Total interconnect length (m) – active wiring only (footnote for calculation) *IS*	10836	12632	14654	18624	21546	25249	31659
FITS/m X 10E-3 (fitting footnote) *IS*	0.46	0.40	0.34	0.27	0.23	0.20	0.16
Jmax (A/cm^2)—wire (at 105°C)	5.8E5	7.1E5	8.0E5	9.6E5	1.1E6	1.3E6	1.4E6
Imax (mA)—via (at 105°C)	0.36	0.36	0.33	0.32	0.29	0.27	0.24
Local wiring pitch (nm)	500	450	405	365	330	295	265
Local wiring A/R (for Al)	2	2	2.1	2.1	2.2	**	**

Constant reliability still requires improvement in defect density - based on 5 FITS and high performance MPU

MPU Near Term Years

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
MPU ½ pitch	**230**	**210**	**180**	**160**	**145**	**130**	**115**
MPU gate length (nm)	**140**	**120**	**100**	**90**	**80**	**70**	**65**
Cu local dishing (nm), 5% × height *WAS*	**18**	**16**	**15**	**14**	**13**	**12**	**11**
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array *IS*	**36**	**32**	**30**	**28**	**26**	**24**	**22**
Intermediate wiring pitch (nm)	**640**	**575**	**520**	**465**	**420**	**375**	**340**
Intermediate wiring A/R (Al)	**2.2**	**2.3**	**2.4**	**2.5**	**2.6**	**	**
Intermediate wiring dual damascene A/R (Cu wire/via)	**2.0/2.1**	**2.1/2.1**	**2.2/2.1**	**2.2/2.1**	**2.2/2.2**	**2.3/2.2**	**2.4/2.2**
Cu intermediate dishing (nm), 15 micron wide wire, 10% × height *WAS*	**64**	**60**	**57**	**51**	**46**	**43**	**41**
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array *IS*	**64**	**60**	**57**	**51**	**46**	**43**	**41**

No significant dishing at local levels - thinning due to erosion over large areas (50% areal coverage)

MPU Near Term Years

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Minimum global wiring pitch (nm)	**1050**	**945**	**850**	**765**	**690**	**620**	**560**
Global wiring A/R (Al)	**2**	**2.1**	**2.2**	**2.3**	**2.4**	**	**
Global wiring dual damascene A/R (Cu wire/via)	**2.2/2.4**	**2.3/2.6**	**2.4/2.7**	**2.5/2.7**	**2.6/2.8**	**2.7/2.8**	**2.7/2.8**
Cu thinning global wiring due to dishing and erosion (nm), 10% × height, 80% areal density, 15 micron wide wire *IS*	**116**	**109**	**102**	**95**	**90**	**84**	**76**
Cu global wiring dishing (nm), 15 micron wide wire, 10% × height *WAS*	**116**	**109**	**102**	**95**	**90**	**84**	**76**
Cu thinning global wiring due to dishing (nm), 100 micron wide isolated feature *IS*	**80**	**72**	**65**	**59**	**53**	**48**	**43**

New combined dishing/erosion metric for global wire

Cu thinning due to dishing for isolated lines/pads

MPU Near Term Years

YEAR TECHNOLOGY NODE	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
Conductor effective resistivity (µΩ-cm) Al wiring	**3.3**	**3.3**	**3.3**	**3.3**	**3.3**	**	**
Conductor effective resistivity (µΩ-cm) Cu wiring*	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Barrier/cladding thickness (for Cu wiring) (nm)***	**17**	**16**	**14**	**13**	**12**	**11**	**10**
Interlevel metal insulator —effective dielectric constant (κ) *WAS*	**3.5—4.0**	**3.5—4.0**	**2.7—3.5**	**2.7—3.5**	**2.2—2.7**	**2.2—2.7**	**1.6—2.2**
Interlevel metal insulator —effective dielectric constant (κ) *IS*	**3.5—4.0**	**3.5—4.0**	**2.9—3.5**	**2.9—3.5**	**2.2—2.9**	**2.2—2.9**	**1.6—2.2**
Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ) *IS*	**2.9**	**2.9**	**2.7**	**2.7**	**2.0**	**2.0**	**1.3**

Expanded range of dielectric constants

Return of bulk dielectric constant target specification

MPU Long Term Years

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Total interconnect length (m) – active wiring only (footnote for calculation) *IS*	51730	91532	148835
FITS/m X 10E-3 (fitting footnote) *IS*	0.10	0.05	0.03
Cu local dishing (nm), 5% × height *WAS*	9	7	5
Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array *IS*	18	14	10
Cu intermediate wiring dishing (nm), 15 micron wide wire, 10% × height *WAS*	30	22	17
Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array *IS*	30	22	17
Cu thinning global wiring due to dishing and erosion (nm), 10% × height, 80% areal density, 15 micron wide wire *IS*	55	38	29
Cu global wiring dishing (nm), 15 micron wide wire, 10% × height *WAS*	55	38	29
Cu thinning global wiring due to dishing (nm), 100 micron wide isolated feature *IS*	30	21	15
Conductor effective resistivity (µΩ-cm) Cu wiring *WAS*	2.2	<1.8	<1.8
Conductor effective resistivity (µΩ-cm) Cu wiring *IS*	2.2	2.2	2.2
Barrier/cladding thickness (nm) *WAS*	0	0	0
Barrier/cladding thickness (nm) *IS*	7	5	4
Interlevel metal insulator—effective dielectric constant (κ) *WAS*	1.5	<1.5	<1.5
Interlevel metal insulator—effective dielectric constant (κ) *IS*	1.6	<1.6	<1.3
Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ) *IS*	1.3	<1.3	1.1

Conductor effective resistivity relaxed along with barrier targets

Similar changes proposed to SoC table

International Technology Roadmap for Semiconductors

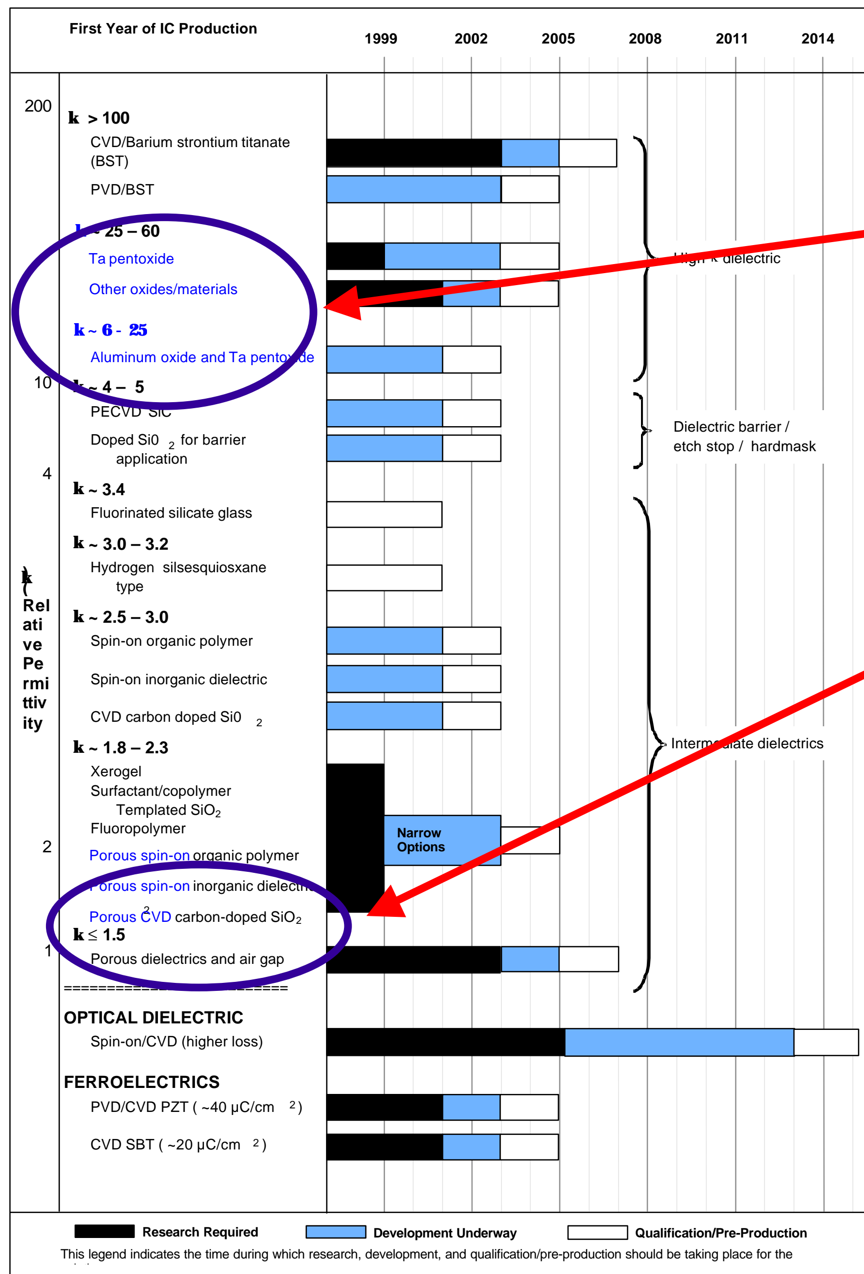
Potential solutions issues

- ALD atomic layer deposition line was deleted in error -
  - reinserted
- Terminology "CEP" - define chemically enhanced planarization
  - added in appendix
- Define second and third generation ECD
  - added in appendix

FEP Cross Cut Issues

- Need to agree on high κ between *FEP* (both DRAM capacitor and gate dielectric) and interconnect (decoupling and MIM caps). Are the two uses and processes sufficiently different to be included in both TWG potential solutions?
    - Yes, Interconnect will own BEOL high κ
- Pre - Metal Dielectric
    - *FEP* will own PMD and its planarization

Dielectric Potential Solutions



Minor Corrections

High k and terminology for porous

Challenges

- High κ and ferroelectrics materials development
- Development and integration of ultra low κ materials with acceptable mechanical/thermal properties
- Fabricating low-temp low-loss SiO_2 optical interconnect
- Addressing turning radius of higher loss polymer optics

Barrier Potential Solutions

First Year of IC Production	1999	2002	2005	2008	2011	2014

TiN FOR HIGH A/R CVD W
- Long throw PVD, ionized PVD, CVD

TiN FOR ENHANCED Al FILL
- Long throw PVD, ionized PVD, CVD

BARRIERS FOR Cu
- CVD Ta, TaN, TaSiN, TiN, TiSiN, WN, WSiN
- Long throw or ionized PVD Ta, TaN, TaSiN, TiN, TiSiN, WN, WSiN
- Electroless barriers (CoP, CoWP)
- *In situ* dielectric formation modification
- Metal dopant surface segregation
- Atomic layer deposition

Narrow Options

BARRIERS FOR ALTERNATE CONDUCTORS
- Barriers compatible with cooled conductors
- Barriers for RF
- Barriers compatible with optical transmission
- Barriers compatible with conducting polymers

Narrow Options

Research Required | Development Underway | Qualification/Pre-Production

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Correction

Addition of Atomic Layer Deposition

Challenges

- Solutions for high A/R DRAM contacts
- Conformal barriers for dual damascene Cu - thin, effective diffusion barrier for low via resistance

International Technology Roadmap for Semiconductors

Nucleation Potential Solutions

First Year of IC Production: 1999 | 2002 | 2005 | 2008 | 2011 | 2014

NUCLEATION LAYERS FOR Al FILL

(Enhanced PVD – long throw PVD, ionized PVD) Ti/TiN, CVD Al for Al fill

NUCLEATION LAYERS FOR CONTACT FILL

(Enhanced PVD, CVD) TiN for high A/R CVD W contact fill for DRAM

Other nucleation layer for high A/R contact fill for DRAM

NUCLEATION LAYERS FOR Cu

ECD Cu Seed repair

CVD Cu Seed for ECD

Electroless Cu Seed for ECD

Seedless ECD

Enhanced PVD Cu seed for ECD

Enhanced PVD Cu for PVD Cu fill

CVD Cu for PVD Cu fill

Alternate wetting layers for PVD Cu fill

Wetting layers for high pressure Cu fill

Narrow Options

Research Required | Development Underway | Qualification/Pre-Production

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the

Addition

ECD Cu seed repair

Challenges

High A/R Al vias

Nucleation layers other than TiN for high A/R DRAM contacts

Advanced nucleation layers for Cu interconnect which do not degrade conductor effective resistivity

International Technology Roadmap for Semiconductors

Conductor Potential Solutions

First Year of IC Production	1999	2002	2005	2008	2011	2014
W CONDUCTOR						
Low temperature W conductor						
CONTACT FILL						
High A/R CVD W contact fill for DRAM						
Other high A/R contact fill for DRAM						
Al CONDUCTOR						
Enhanced PVD/CVD Al fill						
Cu CONDUCTOR						
Second generation Cu ECD						
Third generation Cu ECD CVD Cu CVD/PVD Cu fill High pressure Cu fill		Narrow Options				
ALTERNATE CONDUCTORS						
Cooled conductors Superconductors RF Optical Other conductors including polymers				Narrow Options		
ELECTRODE CONDUCTORS						
Materials for metal-insulator-metal capacitors						

Research Required — Development Underway — Qualification/Pre-Production

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

NO PROPOSED CHANGES

Challenges

- Low temp CVD W for low κ compatibility
- High A/R contact fill for DRAM
- Cu fill of dual damascene structures with reduced CD and high A/R
- Identifying and implementing solutions after Cu and low κ

Planarization Potential Solutions

First Year of IC Production: 1999, 2002, 2005, 2008, 2011, 2014

PLANARIZATION TECHNOLOGIES
- Chemical Mechanical Polishing (CMP)
- Chemically Enhanced Planarization (CEP)
- Other

PLANARIZATION TOOLS
- Rotary
- Orbital
- Ellipsoidal
- Linear

PLANARIZATION TOOL CONFIGURATION
- Stand-alone planarization and clean
- Integrated planarization and clean

CONSUMABLES ENHANCEMENTS
- Controlled selectivity slurries
- Slurry-free process/abrasive pads
- Low defect density pads and slurries for Cu
- Other

CLEANING TECHNIQUES
- Brush
- Spray
- Immersion with/without megasonic
- Supercritical CO_2 other fluids
- New chemical agents
- Other

Research Required | Development Underway | Qualification/Pre-Production

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

NO PROPOSED CHANGES

Challenges

- Continued development of tools/slurries/pads
- Cleaning technologies
- Many new low and high κ materials - may require new planarization approaches
- Pattern dependent planarization
- Planarization over passive elements for SOC

Etch Potential Solutions

First Year of IC Production: 1999, 2002, 2005, 2008, 2011, 2014

METAL ETCH
- Enhanced RIE/HDP for high A/R Al
- RIE/HDP for Cu
- Electrode materials for high κ

DIELECTRIC ETCH—CONTACT/ VIA/TRENCH
- High κ materials
- Fluorinated silicate glass – RIE/HDP
  HSQ – RIE/HDP
- Organic – RIE/HDP
  Carbon-doped – RIE/HDP
- Porous organics – HDP
  Porous SiO_2 – HDP
  Porous carbon-doped – HDP
  Porous PTFE – HDP
  (Narrow Options)
- Porous κ < 1.5 – HDP
  Porous κ < 1.5 – reduced damage/distortion
  (Narrow Options)

RESIST STRIP
- Chemical downstream
  RIE
  HDP
  Non-conventional
  (Narrow Options)

POST-ETCH RESIDUE CLEAN
- Wet
  Vapor phase
  Dry
  Supercritical fluids
  (Narrow Options)

Legend: Research Required | Development Underway | Qualification/Pre-Production

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

NO PROPOSED CHANGES

Challenges

- Dimensional control with small features and high A/R
- Selectivity to etch stops and hard masks
- Many new low and high k materials - may require new chemistries
- Strip/clean compatibility with these new materials
- Low damage

International Technology Roadmap for Semiconductors

PIDS Cross Cut Issues

- What are issues with high κ used in MIM or other interconnect capacitors
  – consider specs for PIDS Table 29
- What is *PIDS* Maximum Wire Length
  – *PIDS* will change nomenclature to Max Signal Local Wire and share with Interconnect
- First pass on interconnect needs for novel devices
  – start addressing for 2001
- Dielectric leakage and breakdown
  – under *PIDs* consideration
  – under Interconnect review - 2001

Packaging Cross Cut Issues

- Underbump metallurgy for flip chip and wire bond
  - treat in both sections with emphasis on materials compatibility and Cu/low k integration with *Interconnect* and packaging schemes in *Packaging*
- Major issues
  - list of issues for 2000
  - should receive further treatment in 2001

Design Cross Cut Issues

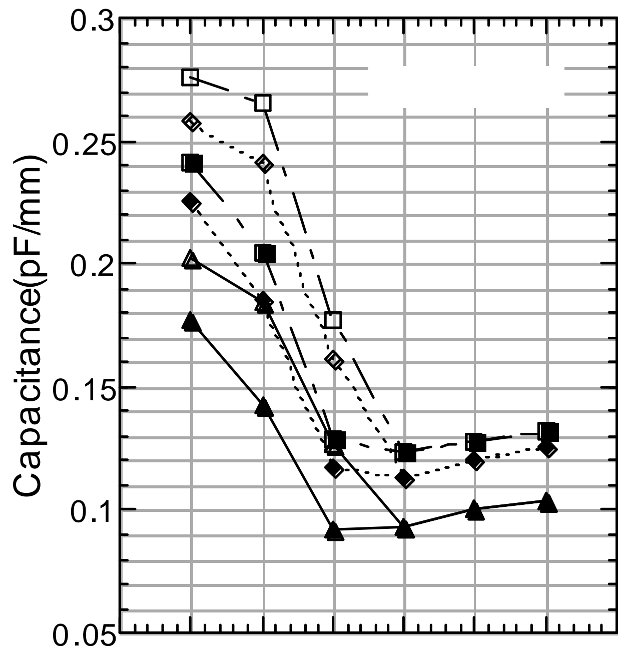
- Can W at contact meet all design needs for all products?
- What is the value of reducing wiring resistivity from 2.2 to 1.8 μ-Ω-cm?
  - Subgroup task beginning with telecon with *Interconnect*, *Design* and *PIDS*
- Please state requirements for dielectric leakage/length @ operating conditions
  - Capacitor requirements

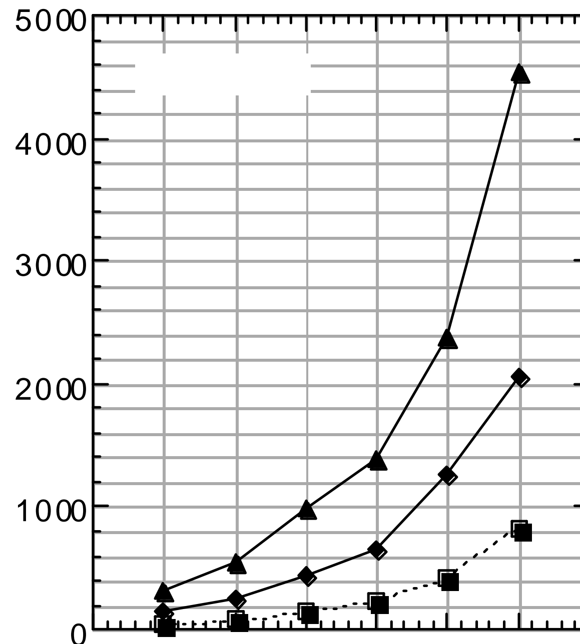
Modeling Cross Cut Issues

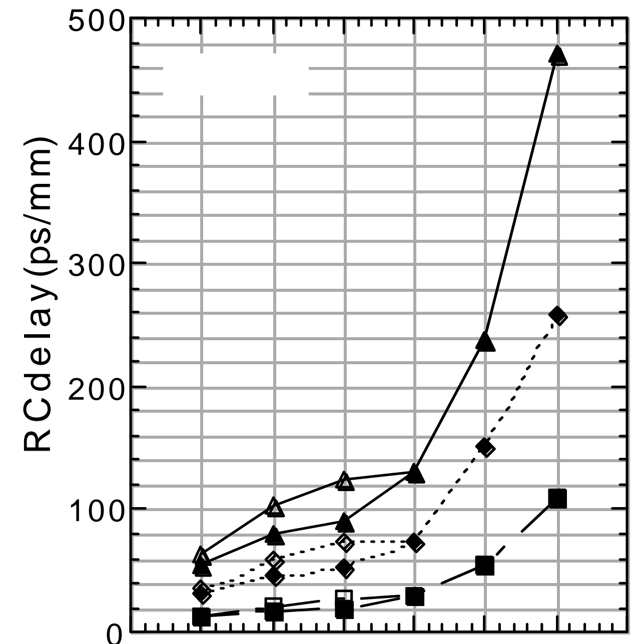
- Design constraints due to process induced variation
- Look at temperature gradient within a level
- Still waiting for global model

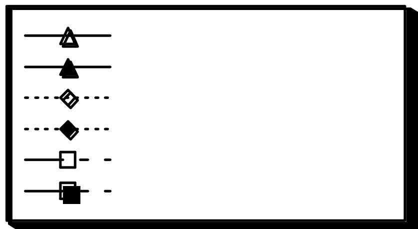
Y2.001 planning

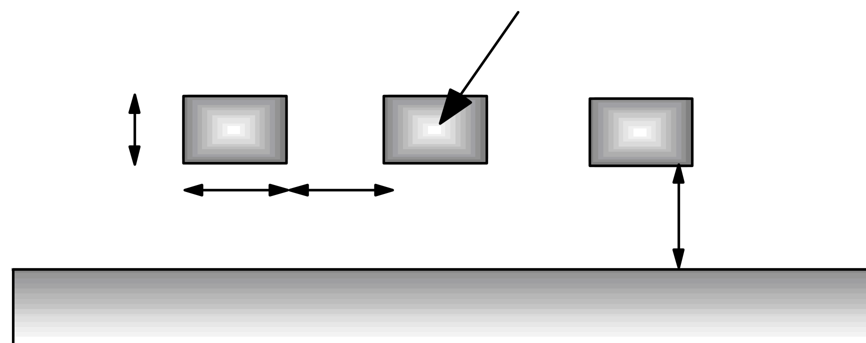
- *Interconnect* needs to address novel devices
- Performance impact of process induced variation
- Parametric performance models
- Can technology metrics be tied to performance limits
  - Trade-off between low κ and metal levels and design rules
- Include crosstalk metric



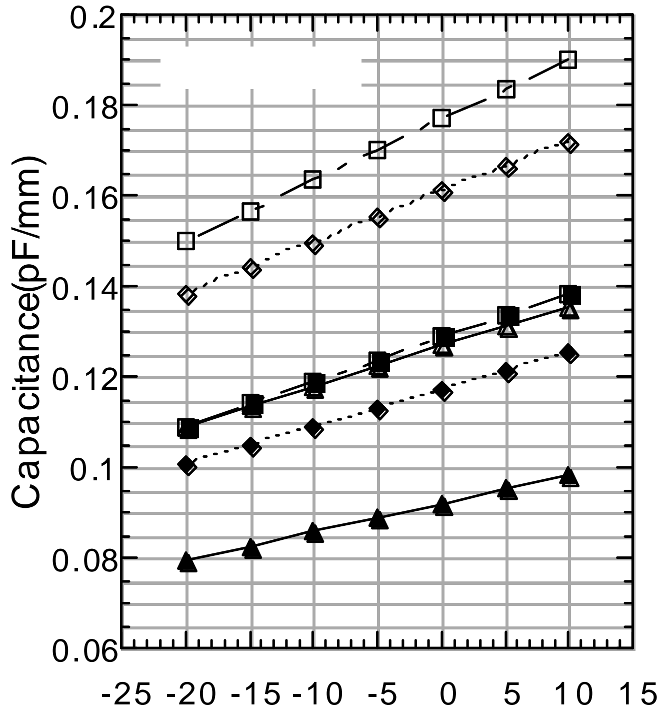


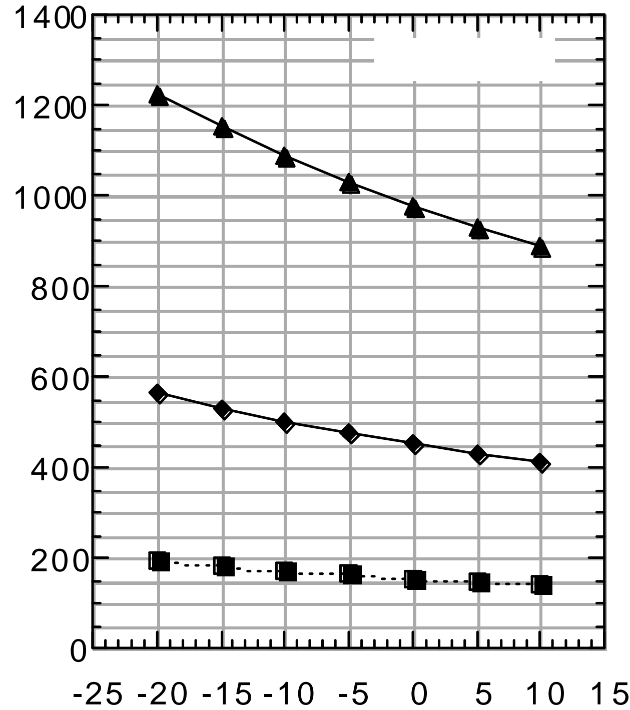


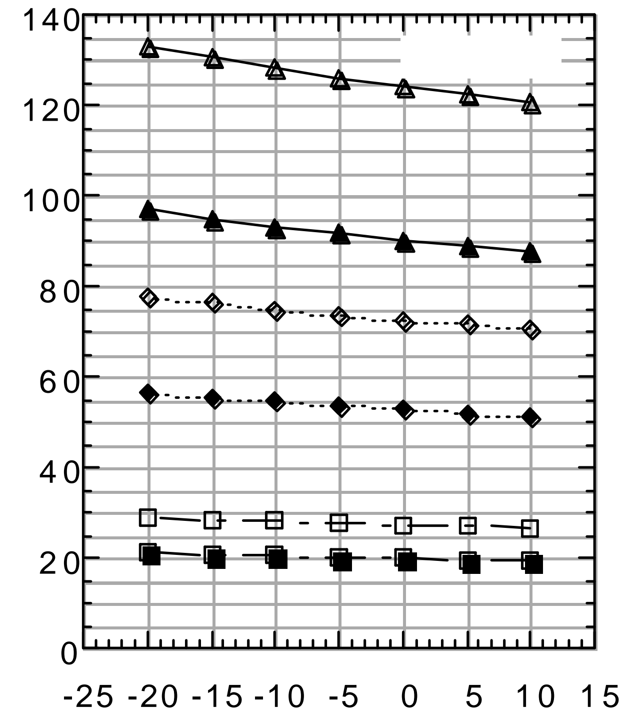


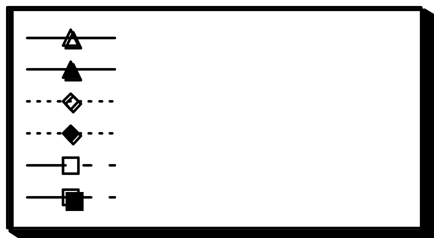


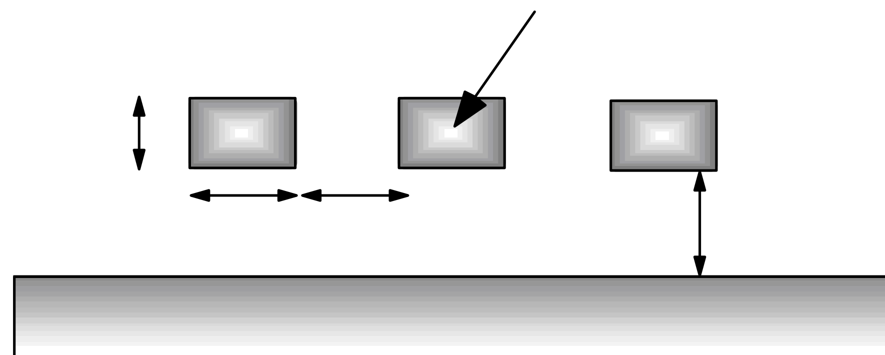
International Technology Roadmap for Semiconductors











International Technology Roadmap for Semiconductors

Summary

- Cu/low k interconnects extendable for local/intermediate wiring
  - Crosstalk must be carefully managed
  - Dimensional effects at < 50 nm may raise effective r of wire
- Global wiring remains the problem
  - Design solutions with repeaters, new architectures - helps
  - Coplanar waveguides and free space RF provide
    - High bandwidth, low frequency dispersion and low loss
    - Modular interconnect including compatibility with traditional on-chip and off-chip interconnect technologies
  - Optical interconnects add
    - No frequency-dependent loss or crosstalk
    - No distance-dependent loss or degradation

Last words

- Rapid changes in materials
- Materials solutions alone cannot deliver performance - end of traditional scaling
- System level solutions must be accelerated
- Optical/rf/waveguide/3D current alternatives
- SoC implementations will propagate
- SoC may change competitive picture - driven by functionality not cost/area