

July 11 ITRS Conference

FEP TWG Report

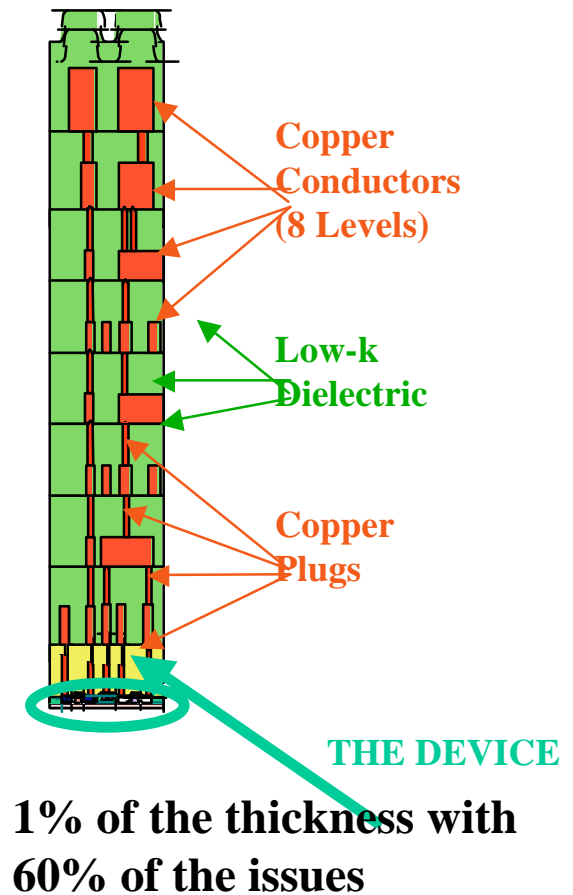
US FEP TWG

Japan FEP TWG

Europe FEP TWG

Korea FEP TWG

Taiwan FEP TWG

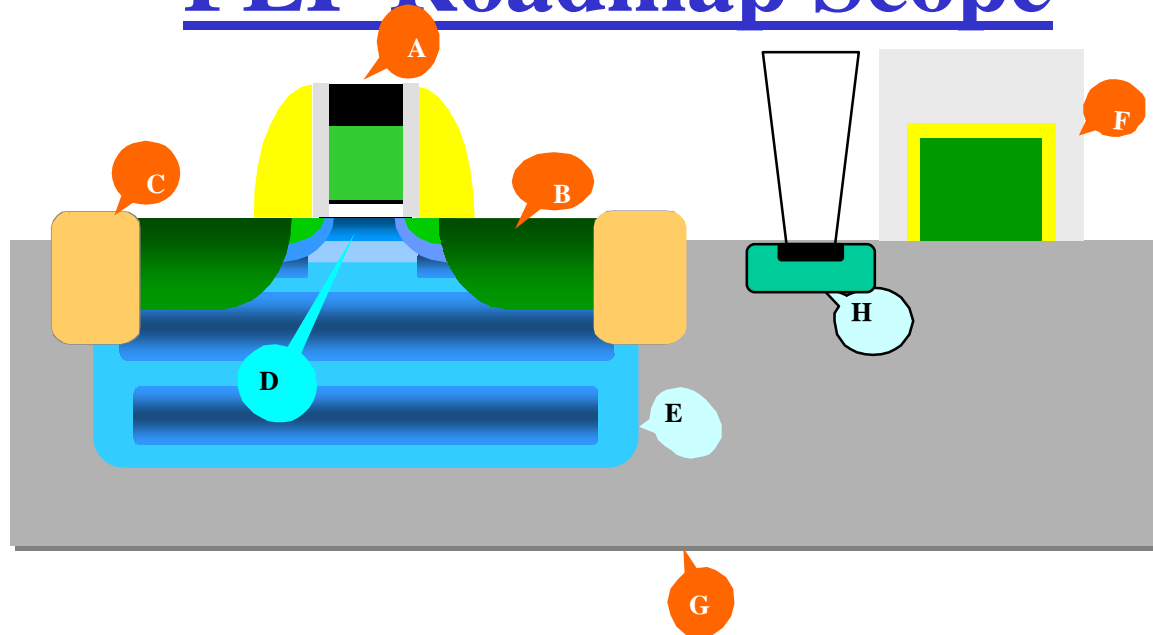


Scope of FEP TWG Activities

- Covers starting silicon wafer through contact silicidation processes and pre-metal dielectric
- Focus on requirements for high performance transistors & storage capacitors for memory and logic products
- Intent is to define comprehensive needs and potential solutions for the key technology areas in the front-end-of-line (FEOL) wafer fabrication processing of integrated circuits



FEP Roadmap Scope



A: Gate Stack B: Source/Drain - Extension
C: Isolation D: Channel
E: Wells F: Capacitor Stack/Trench
G: Starting Material H: Contacts



Thrusts & Sub-TWG Organization

- Starting Materials
- Surface Preparation
- Front End Etch Processes
- Transistor Doping
- Thermal Processing and Thin Films
- Stack Capacitor
- Trench Capacitor
- Device Modeling



Sub-TWG Tasks

- **Using an evolutionary approach, address the following issues:**
 - **Establish evolutionary technical requirements through model-based or physical-based extrapolation**
 - **Identify where barriers exist to evolutionary technology extensions**
 - **Identify if work is underway to optimize known potential solutions to these barriers**
 - **Identify where there is no known solution to these barriers (color code red)**
 - **Identify those known potential solutions which are in R&D or pilot production**
 - **Prepare roadmap documentation**
 - **Collaborate with other sub-TWG's re selection of FEP Difficult Challenges**



Sub-TWG Year 2000 Update Activities

- **Update Color-coded FEP Technology Requirements Tables**
 - **Table 31: FEP Difficult Challenges**
 - **Tables 32a & 32b: Starting Materials**
 - **Tables 33a & 33b: Surface Preparation**
 - **Tables 34a & 34b: Thermal/Thin Films, FEP Etch, and Doping**
 - **Table 35: DRAM Stack Capacitor**
 - **Table 36: DRAM Trench Capacitor**
- **Color Coding Rules:**
 - **No color: known solutions to scaling requirements exist and are being optimized**
 - **Yellow color: scaling barriers exist, good potential solutions are identified, but the optimum solution(s) is not yet known**
 - **Red color: scaling barrier exist and no good potential solution is known**



Contacts for Commentary & Criticism

- **Overall & Table 31:** Mike Jackson- Mike.Jackson@sematech.org
Walter Class- Walter.Class@axcelis.com
- **Tables 32a & 32b:** Howard Huff- howard.huff@sematech.org
David Myers- d-myers@ti.com
- **Tables 33a & 33b:** Scott Becker- sbecker@fsi-intl.com
Glenn Gale- GGale@aus.telusa.com
- **Tables 34a & b Etch:** Pak Leung- pak.leung@sematech.org
Robert Kraft- r-kraft2@ti.com
- **Tables 34a & b Doping:** Larry Larson- larry.larson@sematech.org
Kevin Jones- kjones@eng.ufl.edu
- **Tables 34a&b** Carlton Osburn- osburn@eos.ncsu.edu
Thermal/Films: Howard Huff- howard.huff@sematech.org



Contacts for Commentary & Criticism

- **Table 35: Seiichiro Kawamura - RHD01125@nifty.ne.jp**
- **Table 36: Martin Gutsche - Martin.Gutsche@infineon.com**

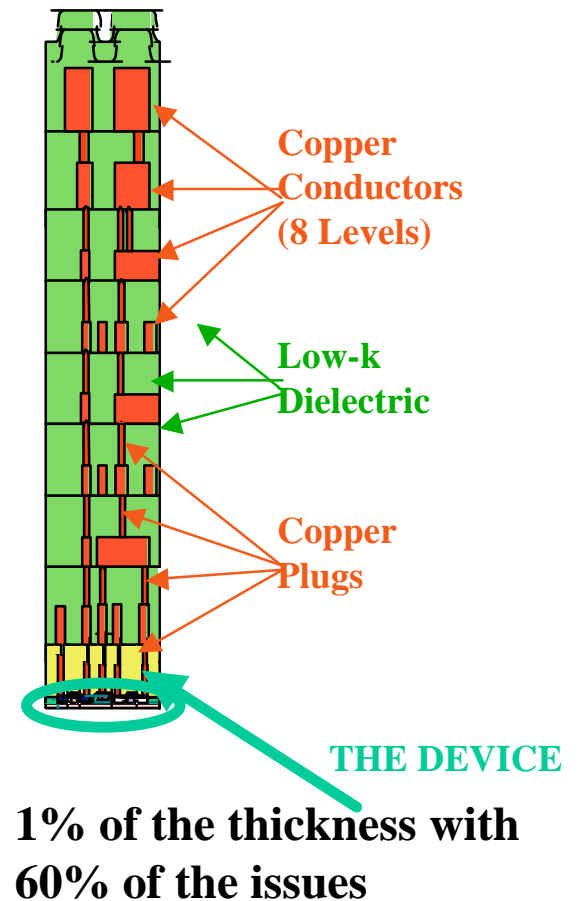


International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

2000 Update--What's Changed vs. What's Unchanged

100 nm High End MPU & ASIC Device



Summary

- **FEP difficult challenges remain, “red walls” may loom sooner**
- **ORTC Changes that effect FEP year 2000 technical requirements updates**
 - **Convergence of MPU and ASIC gate lengths and half-pitches**
 - ASIC and MPU now share common difficult challenges
 - **New DRAM storage cell “a” factor**
 - prior “a” factors deemed too aggressive
 - **New Lithography Field Sizes**
 - Field sizes & new “a” factors drive new DRAM production chip sizes
 - **New MPU Chip Sizes**
 - **New Proposed physical gate length**



FEP Difficult Challenges before 2005

- Gate stack with ultra-thin oxynitride and/or mid- κ dielectric by year 2004
- Stack and Trench DRAM storage capacitor scaling
- Ultra-shallow junctions w/standard processing
- L_{eff} Critical Dimension Control
- Metrology



FEP Difficult Challenges Beyond 2005

- CMOS integration of dual metal high- κ gate stack with L_{eff} CD control
- Ultra-scaled DRAM storage cell
- Beyond CMOS--alternate &/or ultra-scaled transistor structures and materials
- Introduction of new silicon compatible materials, and larger area silicon substrates
- Metrology



The FEP Grand Challenge

**CMOS Compatible, Robust, High-
K Dielectric Gate Stack Process**



International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

High-k Gate Stack Timing & Challenge

Table 34a Thermal/Thin Films, Gate Etch, and Doping Technology Requirements- Near Term

SHORT TERM YEARS

Year of Introduction "Technology Node"	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
Was: MPU Gate Length (nm)	140	120	100	85	80	70	65	M Gate
Is: MPU/ASIC Gate Length (nm)	140	120	100	90	80	70	65	MPU/ASIC
New: Proposed Final Physical Bottom Gate Length after Etch (nm)	120	100	90	80	70	65	60	MPU/ASIC
Equivalent physical Oxide Thickness T_{ox} (nm) (A)	1.9-2.5	1.9-2.5	1.5-1.9	1.5-1.9	1.5-1.9	1.2-1.5	1.0-1.5	MPU/ASIC
Gate Dielectric Leakage @ 100°C (nA/μm) High Performance (B)	5	7	8	10	13	16	20	MPU/ASIC
Gate Dielectric Leakage @ 100°C (pA/μm) Low Power (B)	5	7	8	10	13	16	20	MPU/ASIC

- High K gate stack could be required as early as the year 2005
- MPU and ASIC share this requirement
- New proposed Gate Length may drive year 2004 implementation
- It is a challenge of substantial scope
- Changes of this magnitude have normally taken 10 years to implement



DRAM Scaling Challenges

- **DRAM storage capacitor scaling will require extensive changes in capacitor dielectric materials and electrode materials & structures**
 - High-k and Ultra-high-k Dielectric layers
 - Metal, and conductive oxide electrode structures
- **Significant challenges of CMOS integration are also visible**
 - Storage cell limits process temperatures to $<650^{\circ}\text{C}$
 - Cell last process architectures may be required
- **The DRAM challenge rivals the High-k gate stack challenge in magnitude and scope.**



Summary of FEP Year 2000 Updates & 2001 Plans



International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

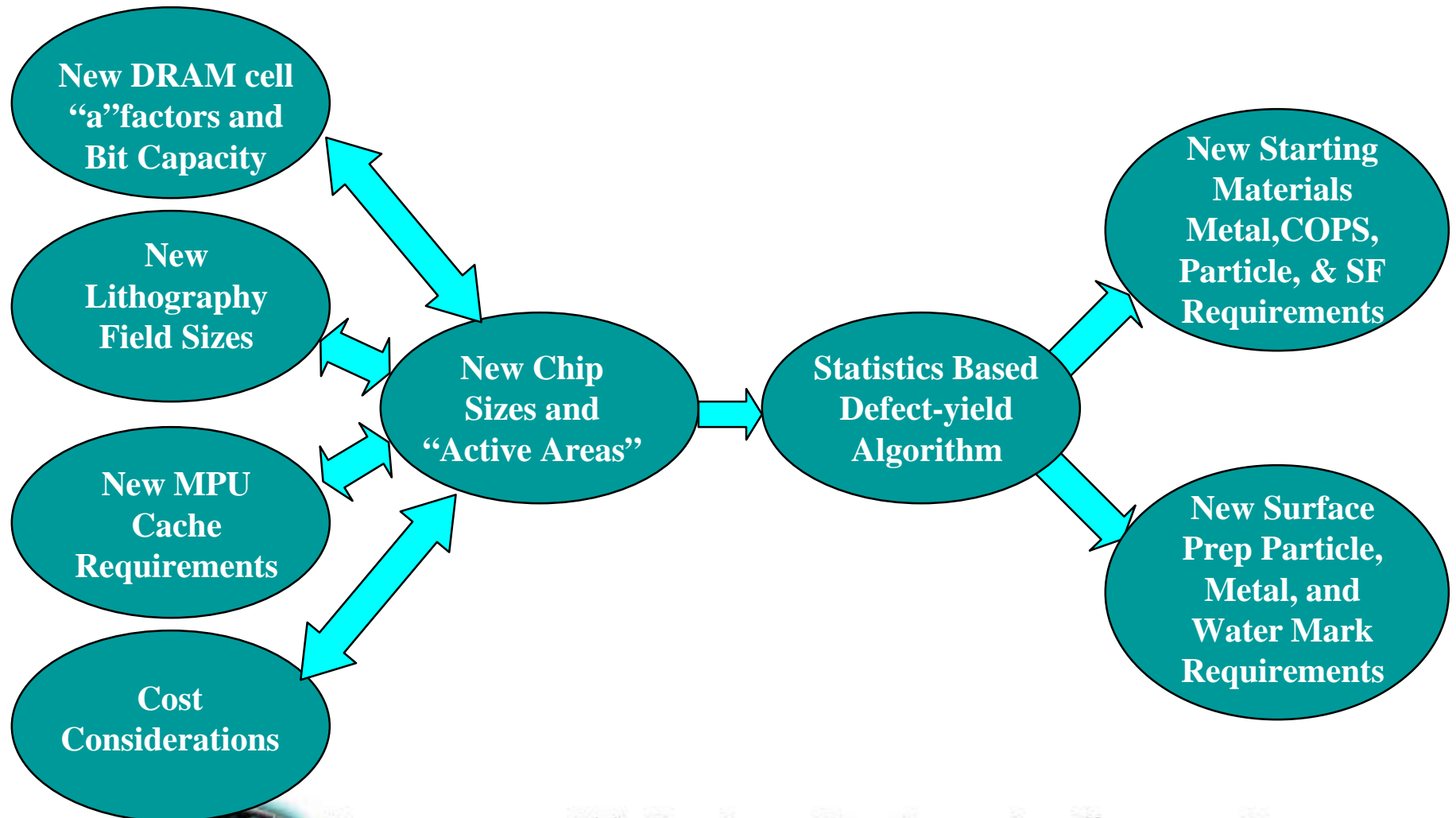
Starting Materials & Surface Preparation Update & 2001 Plans



International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

Chip Size Changes Drive New Defect Requirements for Starting Materials and Surface Preparation



Starting Materials and Surface Preparation 2001 Plans

- **Update and Validate inputs to the the Defect-Yield Algorithms underlie the defect requirements forecasts**



International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

FEP DRAM Update & 2001 Plans

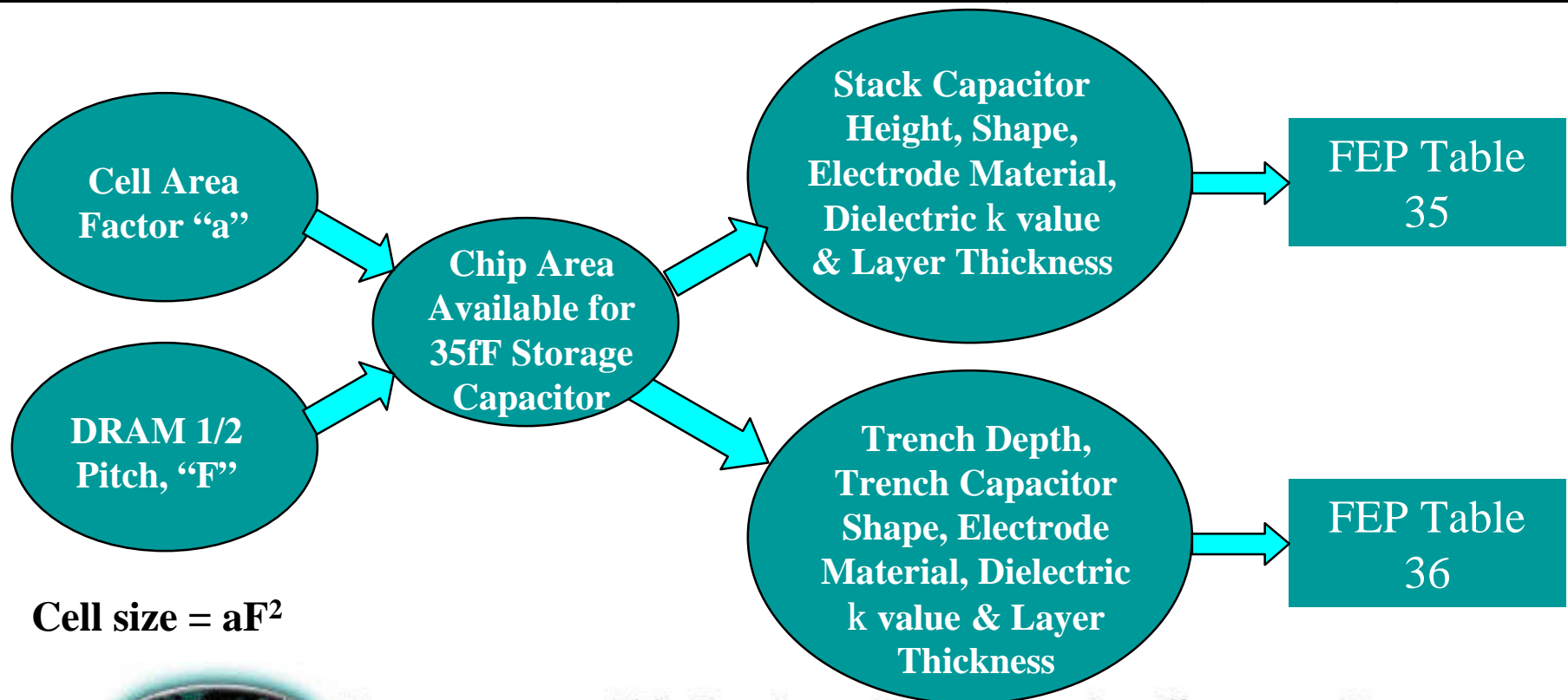


International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

Impact of New DRAM cell ‘a’ Factor

Year of First Product Shipment Technology Node	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
DRAM 1/2 Pitch (nm)						
	8.0	6.0	4.4	3.6	3.0	2.5
	8.0	8.0	6.0	6.0	4.0	4.0
	0.259	0.101	0.044	0.018	0.0075	0.0031
	=0.36*0.72	=0.26*0.39	=0.2*0.22	=0.14*0.13	=0.1*0.08	=0.07*0.04
Cell size [um ²] is	0.259	0.135	0.060	0.029	0.0100	0.0050
Cell Length * Width (um) is	=0.36*0.72	=0.26*0.52	=0.2*0.3	=0.14*0.21	=0.1*0.1	=0.07071*0.07



Memory Year 2000 Update and Year 2001 Plans

- **Tables 35 & 36 Updated to reflect new DRAM cell area factors**
 - Less aggressive “a” factors increase storage area size
 - Impacts future chip sizes and future bits/Chip
- **Year 2001 Plans**
 - Continue to review DRAM chip size, “a” factor and future bits/chip
 - Generate New Requirements for Flash Memory (Europe TWG)
 - Generate New Requirements for Ferroelectric RAM (Japan TWG)



FEP MOS Transistor Update and 2001 Plans



International Technology Roadmap for Semiconductors

July 11, 2000 Work In Progress Not for Publication

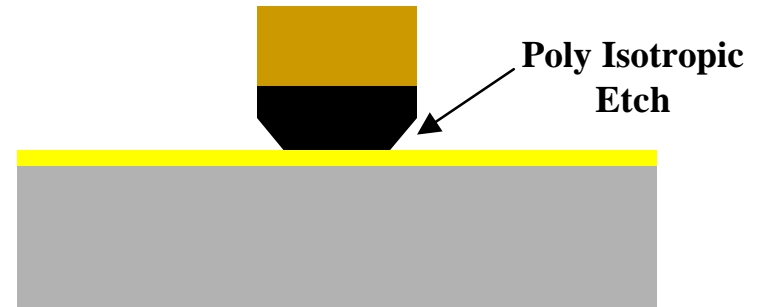
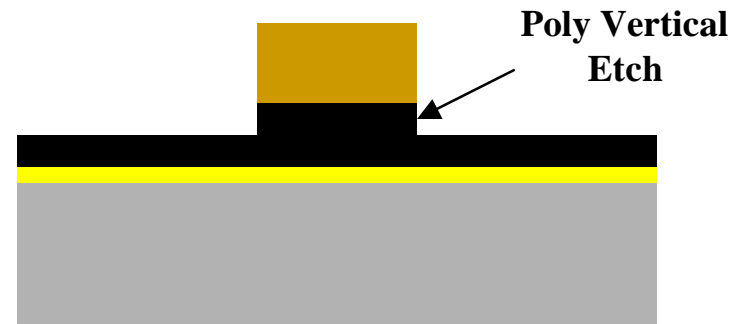
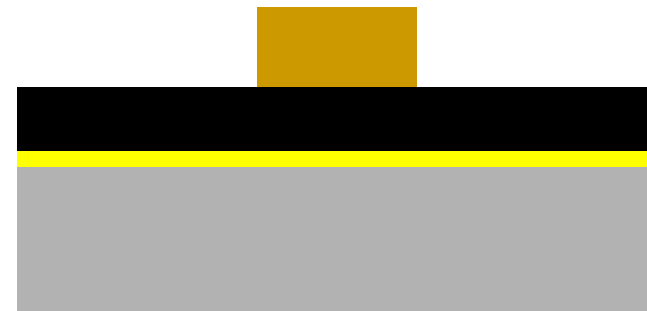
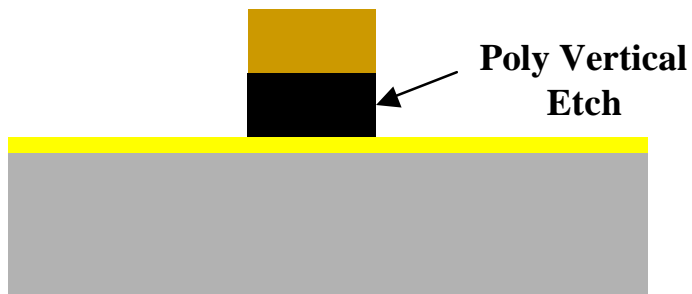
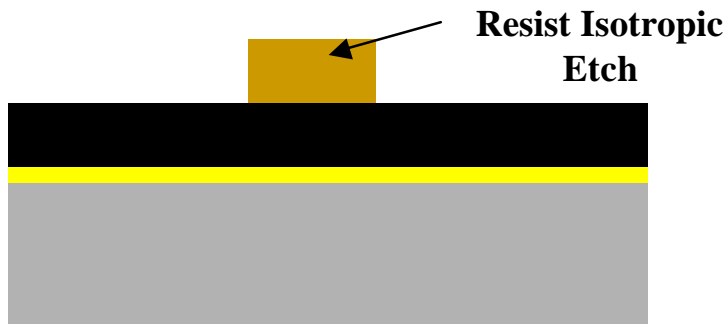
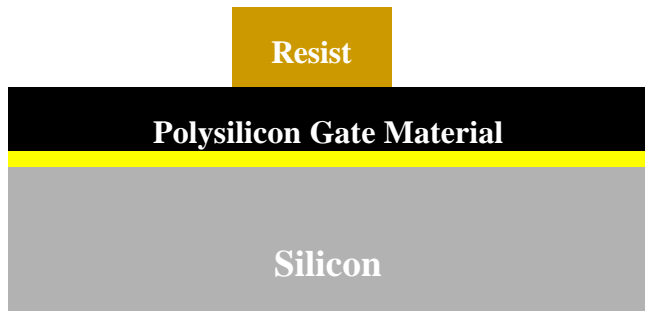
Impact of Proposed New Physical Gate Length

<i>Year of Introduction "Technology Node"</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>	<i>Driver</i>
<i>Was: MPU Gate Length (nm)</i>	<i>140</i>	<i>120</i>	<i>100</i>	<i>85</i>	<i>80</i>	<i>70</i>	<i>65</i>	<i>M Gate</i>
<i>Is: MPU/ASIC Gate Length (nm)</i>	<i>140</i>	<i>120</i>	<i>100</i>	<i>90</i>	<i>80</i>	<i>70</i>	<i>65</i>	<i>MPU/ASIC</i>
<i>New: Proposed Final Physical Bottom Gate Length after Etch (nm)</i>	<i>120</i>	<i>100</i>	<i>90</i>	<i>80</i>	<i>70</i>	<i>65</i>	<i>60</i>	<i>MPU/ASIC</i>

- New proposed reduced gate length is achieved by added etching processes
- Etch practice adds variance to the final physical gate length
- Two Etch processes have been identified
- The practices appear to be widely used
- The year 2000 updated requirements given in table 34 do not reflect the new proposed gate length



Gate Etch Proposed Process Alternatives



Year 2001 CD Etch Process Plans

- **Complete Etch Variance Analysis**
- **Generate Etch Process Requirements**
 - Resist Etch Rate Uniformity
 - Polysilicon Etch Rate Uniformity
 - Polysilicon Thickness Uniformity
- **Validate/Update post-etch physical gate length & future scaling**
- **Update Transistor Requirements**
 - Thermal/Films Requirements
 - Doping Requirements



Year 2001 ITRS MOSFET Plans

- **Develop Application Specific MOSFET Technology Requirements and Potential Solutions**
 - High Performance Logic
 - Low Operating Power Logic
 - Low Standby Power Logic
 - Embedded DRAM transfer device
- **Develop Pre-metal Dielectric Layer Technology Requirements and Potential Solutions.**
- **Collaborate with PIDS TWG to develop FEP requirements related to “beyond CMOS” devices.**
- **Develop new text for the 2001 ITRS publication.**

