International Technology Roadmap for Semiconductors

Defect Reduction

Cross-Cut Technology Working Group

Overview

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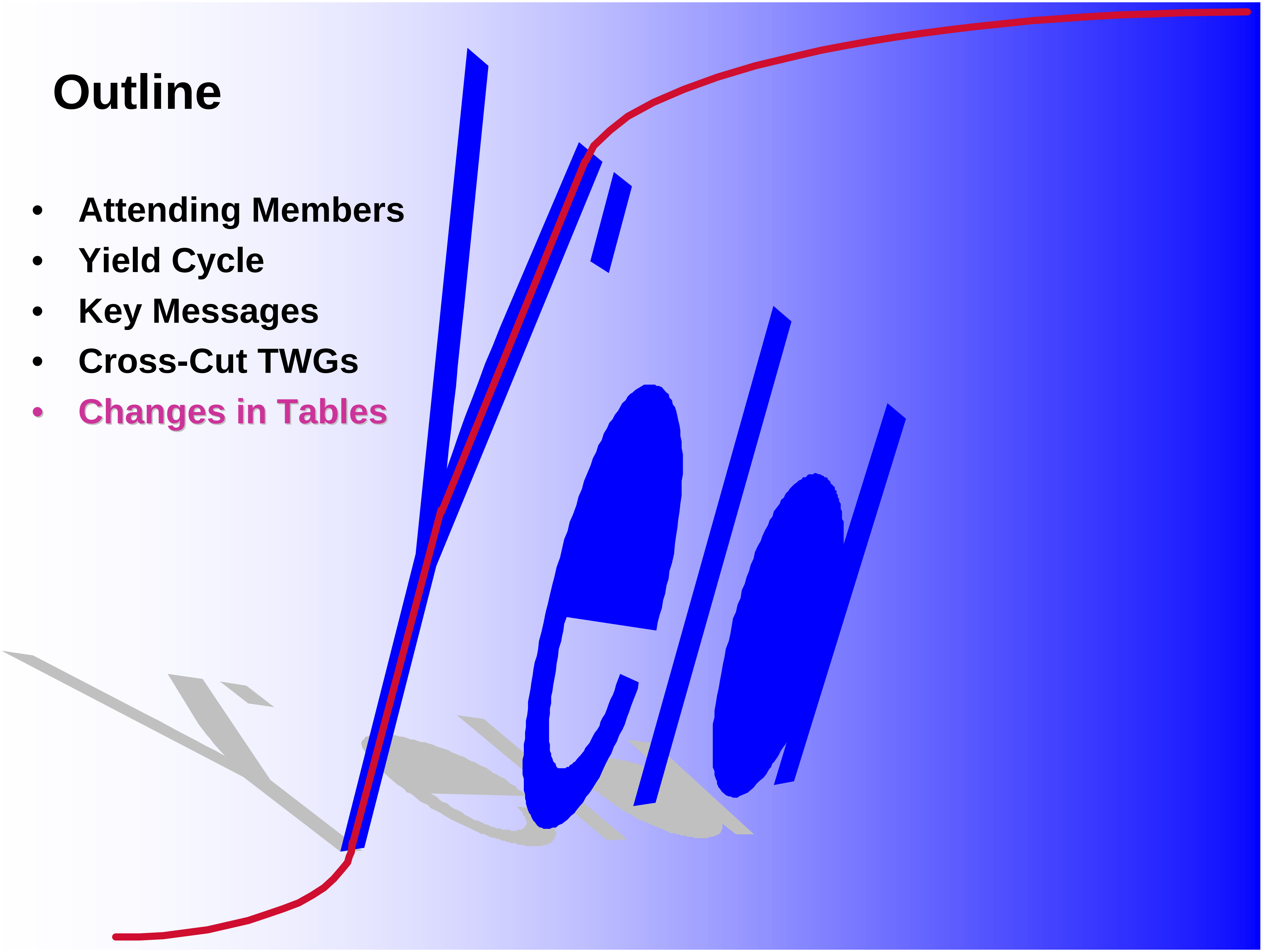
Outline

- Attending Members
- Yield Cycle
- Key Messages
- Cross-Cut TWGs
- Changes in Tables



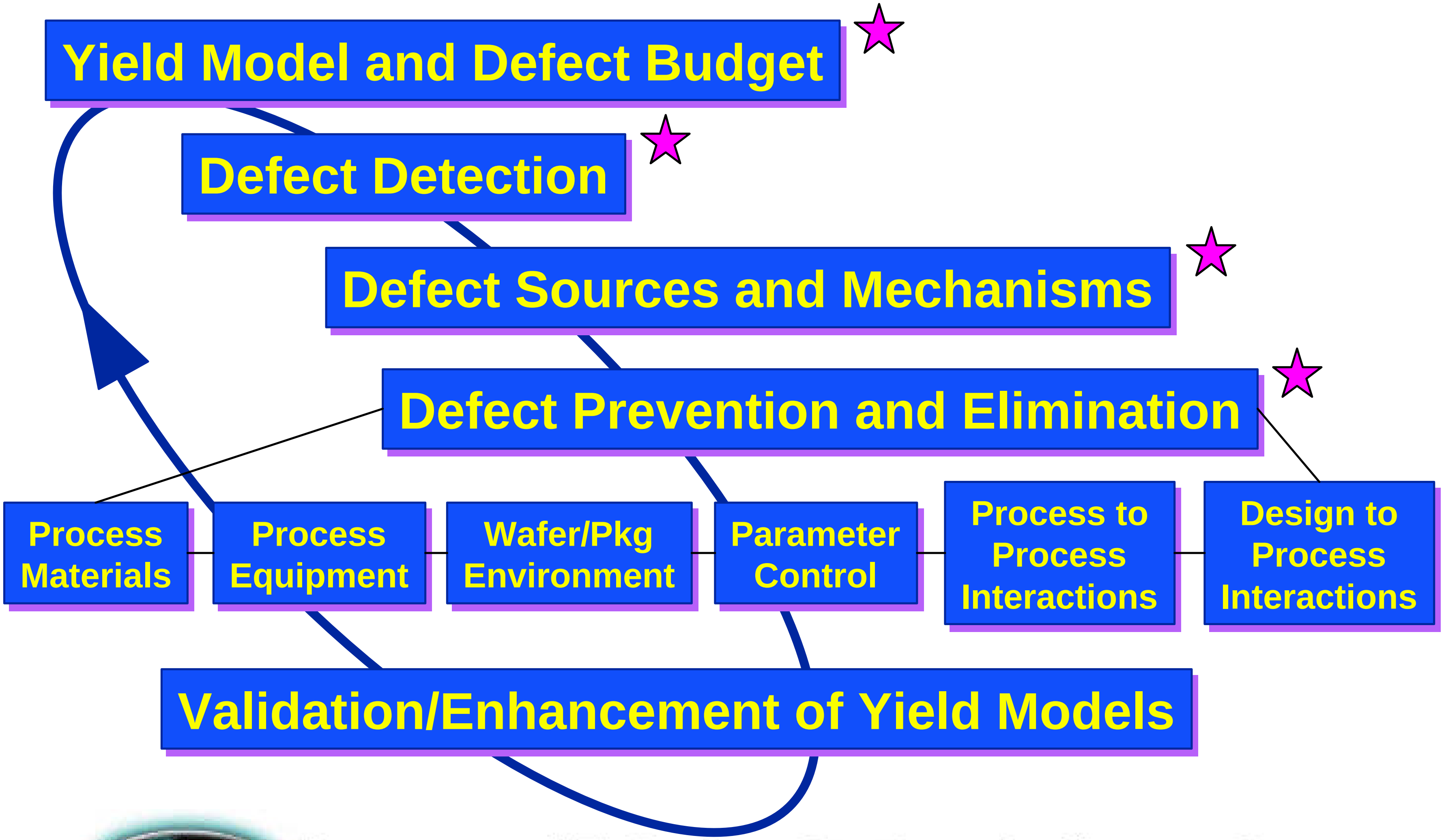
Defect Reduction TWG - ITRS
IMEC April 10-12, 2000

Attending Members

• David Jensen	Co-Chairman	AMD/US
• Milt Godwin	Co-Chairman	AMAT/US
• Chris Long		IBM/US
• Toshihiko Osada		Japan/Fujitsu
• Lothar Pfitzner		Europe/ Fraunhofer Institut
• Nagaswami Venkat		Europe/Philips

DR CCTWG Yield Learning Cycle

★ Focus Topics



Yield Model and Defect Budget ★

Defect Detection ★

Defect Sources and Mechanisms ★

Defect Prevention and Elimination ★

- Process Materials
- Process Equipment
- Wafer/Pkg Environment
- Parameter Control
- Process to Process Interactions
- Design to Process Interactions

Validation/Enhancement of Yield Models

Defect Reduction TWG - ITRS
IMEC   April 10-12, 2000

AGENDA	UPDATE
• Yield Model Re-Evaluation	2000
• SoC Yield Model-Interfaces	2001
• Mini-Line Yield Management	2001
– Yield Goals for Pilot Line	
• Edge Die	2001
– Yielding to Edge/Metrology/Yield Limiter Generated at Edge	

Defect Reduction TWG - ITRS
IMEC April 10-12, 2000

- Measuring Dishing/Warping/ Flatness 2001
- Combining Defect Reduction/ Metrology/Automatic Process Control - How to get efficiencies? 2001
- FOUP Particle Control/ Maintenance 2001
- Defectivity requirements for Novel technologies such as 3-D structures

Defect Reduction TWG - ITRS
IMEC April 10-12, 2000

- 10-15 Year Subjects
  - Making 100% Yield
  - Zero-Fault Control
  - Early Warning Defect Detection (In-situ)
  - Address inspection of vertical structures
  - Backside contamination/abrasion
  - Automatic Process Control
  - Project new defects from new materials and sub-0.1 um structures

- 10-15 Year Subjects (continued)
  - Defects/Faults on 300mm/450mm wafers – sag, warp, surface variations etc
  - Particle detection down to 25 nm
  - Removal of individual particles in local areas
  - Maximize DD structures for in-situ monitoring
  - Defect creation modeling
  - Rework strategy
  - Maximization of factory automation

Yield Model Re-Evaluation

- The units adopted by the Semi/Sematech for defect density is “Defect per meter 2” instead of “defects per cm 2”. Most people still use defects per square cm everywhere. So, while using the table, one can use the following conversion factor:
- Defects / cm^2 = 10^4 x Defects / m^2
- A questionnaire was sent to several member companies and equipment particle data was collected for various pieces of equipment. From this, the median defect density per equipment type was computed. Assuming negative binomial yield model (See page 270 and 271 of the ITRS roadmap 1999 Edition), the defect density per equipment type is extrapolated. the numbers in the table for the current technologies and future technologies could be quite aggressive and Osada-san from Fujitsu mentioned that they were nowhere near the numbers mentioned in the table in their factory. It is not clear how much of this information has been digested by the equipment vendors since this table could be used by the users in future to enforce equipment specifications.

SoC Yield Model-Interfaces

- The SoC chips are often mixed technology including combinations such as embedded DRAM, Logic, and in future MEMS etc. Philips (MOS4) has some experience on how to handle in-line inspections (example: Painter), but in future this can be complicated for defectivity inspections.

Mini-line Yield Management

- This was a topic from Osada-san of Fujitsu. In pilot line mode, the volume of lot starts is relatively low. Fujitsu is struggling with how to model yield on such low volume wafer starts. The typical number they mentioned was 2000 wafers (10 products per month). There were no recommendations or suggestions from other members, although everybody recognized that this is a tough problem.

Edge-Die Yield

- Great gain from edge-die especially for large dies and large wafer sizes.
- Edge exclusion is mapped by Factory Integration, currently 3mm.
- On a die size of approx. 5 mm X 5 mm, approximately 15% of the die lie on the edge of the 200 mm wafer.
- Yield limitation is greater in edge area than center due to mismatch of overlaying processes. This area is larger than the edge exclusion area.
- The problems at the edge are:
  - Thin film deposition non-uniformities
  - Absence of Metrology tool availability to verify layer thickness and defects
  - Litho Edge Bead Removal issues
  - Process Integration issues
- A roadmap on this topic is necessary.

FOUP Particle Control and maintenance (Y2001)

- This is a topic that was brought up by Lothar Pfitzner (Europe-Fraunhofer Institut), regarding FOUP particle control/outgassing/maintenance:

  - FOUP outgassing spec
  - FOUP particle spec
  - Clean room particle spec for FOUP
  - How to clean FOUP
  - Cleaning frequency of FOUP

- FOUP specification needs to be updated beyond i300i.

Defectivity Requirements for Novel Technologies such as 3-D Structures

- In a cross TWG (novel devices), we need to address this topic next meeting.
- Need a 3-D modeling tool.

Cross-Cut TWG with Factory Integration

- Image retrieval considered a key topic because of the volume of information to be transferred. 12MB of information/lot/layer needs to be transferred.
- Factory Integration TWG will attempt to define Defect Reduction Computer System with respect to Response, Capabilities and Bandwidth.
- Factory Integration stressed the needs to reduce the NPW (non-production wafers). Need reliable in-situ particle monitors to avoid NPW. But, in-situ technology has to make more progress.
- All member companies agreed that correlation to wafer level particle is difficult.
- Other topic was Cost vs benefit to expand defect reduction capabilities to include cross-correlation of data between different sources.

Cross-Cut TWG with FEP

- Starting Material and Surface preparation to be discussed by FEP.

Table 76: MPU Yield Model and Defect Budget

Year of Introduction *"Technology Node"* **(WAS)**	*1999* *140nm*	*2000*	*2001* *100nm*	*2002*	*2003*	*2004* *70nm*	*2005*	*2008* *(50nm*)*	*2011* *(35nm*)*	*2014* *(25nm*)*
Year of Introduction *"Technology Node"* **(IS)**	*1999* *180nm*	*2000*	*2001* *130nm*	*2002*	*2003*	*2004*	*2005* *100nm*	*2008* *70nm*	*2011* *50nm*	*2014* *35nm*
MPU										
MPU / ASIC 1/2 Pitch *(A)* **(WAS)**	230	210	180	160	145	130	115	81	58	41
MPU / ASIC 1/2 Pitch *(A)* **(IS)**	230	210	180	160	145	130	115	80	55	40
Critical Defect Size **(WAS)**	115	105	90	80	73	65	58	41	29	21
Critical Defect Size **(IS)**	115	105	90	80	73	65	58	40	28	20
Chip Size *(B)* **(WAS)**	170	170	170	191	214	224	235	269	308	354
Chip Size *(B)* **(IS)**	170	178	186	195	204	214	223	256	294	337
Overall Electrical D0 (faults/m^2) at critical defect size or greater *(C)* **(WAS)**	1742	1742	1742	1550	1384	1322	1260	1101	961	836
Overall Electrical D0 (faults/m^2) at critical defect size or greater *(C)* **(IS)**	1742	1664	1592	1519	1452	1384	1328	1157	1007	879
Random D0 *(faults/m^2)*(D)* **(WAS)**	1117	1117	1117	994	887	848	808	706	616	536
Random D0 * (faults/m^2) *(D)* **(IS)**	1117	1067	1021	974	931	887	851	742	646	563
# Mask Levels *(E)*	23	23	23	24	24	24	25	27	28	29
Random Faults/Mask **(WAS)**	49	49	49	41	37	35	32	26	22	18
Random Faults/Mask **(IS)**	49	46	44	41	39	37	34	27	23	19

Table 76: MPU Yield Model and Defect Budget

MPU Random Process Induced Defect (PID) Budget (defects/m2) for Generic Tool Type										
scaled to 75nm critical defect size or greater *(F)* (WAS)										
CMP Clean	293	244	179	121	89	68	49	20	8	4
CMP Insulator	421	351	258	174	128	98	70	28	12	5
CMP Metal	307	256	188	127	93	71	51	20	9	4
Coat/Develop/Bake	118	99	72	49	36	27	20	8	3	1
CVD Insulator	542	452	332	224	164	126	90	36	16	7
CVD Oxide Mask	503	419	308	208	152	117	84	34	15	6
Dielectric Track	157	131	96	65	48	37	26	11	5	2
Furnace CVD	561	468	344	232	170	130	93	37	16	7
Furnace Fast Ramp	196	164	120	81	59	46	33	13	6	2
Furnace Oxide/Anneal	269	224	165	111	81	62	45	18	8	3
Implant High Current	462	385	283	191	140	107	77	31	13	6
Implant Low/Med Current	403	336	247	166	122	94	67	27	12	5
Inspect PLY	165	138	101	68	50	38	28	11	5	2
Inspect Visual	187	156	115	77	57	43	31	12	5	2
Litho Cell	183	152	112	75	55	42	30	12	5	2
Litho Stepper	87	73	53	36	26	20	15	6	3	1
Measure CD	181	151	111	75	55	42	30	12	5	2
Measure Film	202	168	124	83	61	47	34	13	6	2
Measure Overlay	165	138	101	68	50	38	28	11	5	2
Metal CVD	263	219	161	109	80	61	44	18	8	3
Metal Electroplate	157	131	96	65	48	37	26	11	5	2
Metal Etch	611	509	374	252	185	142	102	41	18	7
Metal PVD	392	326	240	162	118	91	65	26	11	5
Plasma Etch	576	481	353	238	174	134	96	38	17	7
Plasma Strip	401	334	245	165	121	93	67	27	12	5
RTP CVD	171	143	105	71	52	40	28	11	5	2
RTP Oxide/Anneal	118	99	72	49	36	27	20	8	3	1
Test	64	54	39	27	19	15	11	4	2	1
Vapor Phase Clean	428	357	262	177	130	100	71	29	12	5
Wafer Handling	25	21	15	10	8	6	4	2	1	0.3
Wet Bench	446	371	273	184	135	104	74	30	13	5

Table 76: MPU Yield Model and Defect Budget

MPU Random Process Induced Defect (PID) Budget (defects/m2) for Generic Tool Type scaled to 75nm critical defect size or greater *(F)* (IS)										
CMP Clean	320	255	179	130	102	78	56	22	9	4
CMP Insulator	461	367	258	186	146	112	81	32	13	6
CMP Metal	335	267	188	136	106	82	59	23	9	4
Coat/Develop/Bake	129	103	72	52	41	31	23	9	4	2
CVD Insulator	593	472	332	240	188	144	104	41	16	7
CVD Oxide Mask	550	438	308	222	175	134	96	38	15	7
Dielectric Track	172	137	96	70	55	42	30	12	5	2
Furnace CVD	614	489	344	248	195	149	108	42	17	7
Furnace Fast Ramp	215	171	120	87	68	52	38	15	6	3
Furnace Oxide/Anneal	294	234	165	119	93	71	52	20	8	4
Implant High Current	505	402	283	204	160	123	89	35	14	6
Implant Low/Med Current	441	351	247	178	140	107	77	30	12	5
Inspect PLY	181	144	101	73	57	44	32	12	5	2
Inspect Visual	205	163	115	83	65	50	36	14	6	2
Litho Cell	200	159	112	81	63	49	35	14	5	2
Litho Stepper	95	76	53	39	30	23	17	7	3	1
Measure CD	199	158	111	80	63	48	35	14	5	2
Measure Film	221	176	124	89	70	54	39	15	6	3
Measure Overlay	181	144	101	73	57	44	32	12	5	2
Metal CVD	288	229	161	116	91	70	50	20	8	3
Metal Electroplate	172	137	96	70	55	42	30	12	5	2
Metal Etch	668	532	374	270	212	163	117	46	18	8
Metal PVD	428	341	240	173	136	104	75	29	12	5
Plasma Etch	631	502	353	255	200	153	111	43	17	8
Plasma Strip	438	349	245	177	139	107	77	30	12	5
RTP CVD	187	149	105	76	59	46	33	13	5	2
RTP Oxide/Anneal	129	103	72	52	41	31	23	9	4	2
Test	70	56	39	28	22	17	12	5	2	1
Vapor Phase Clean	469	373	262	189	149	114	82	32	13	6
Wafer Handling	28	22	15	11	9	7	5	2	1	0.3
Wet Bench	487	388	273	197	155	119	85	33	13	6

Table 77: DRAM Yield Model and Defect Budget

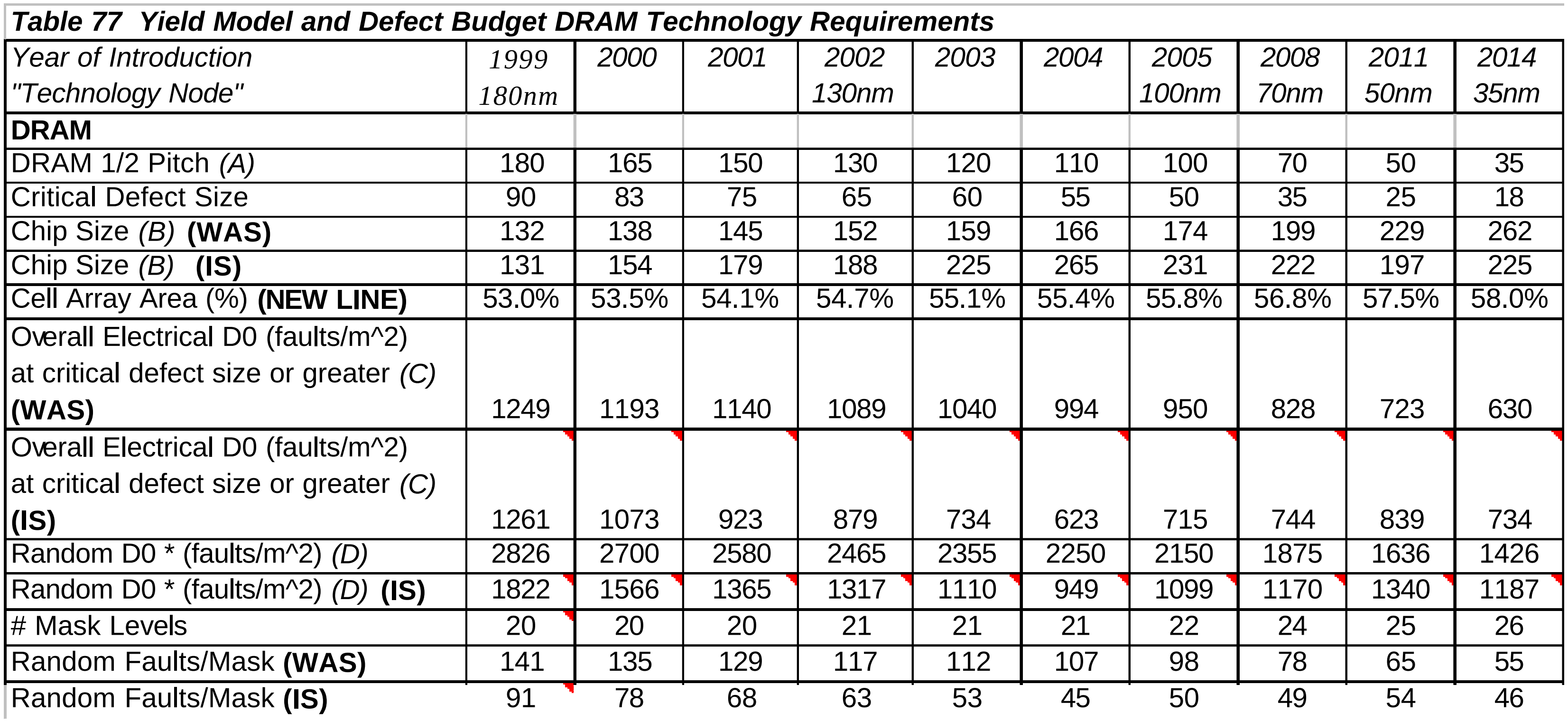


Table 77 Yield Model and Defect Budget DRAM Technology Requirements

Year of Introduction *"Technology Node"*	*1999* *180nm*	*2000*	*2001*	*2002* *130nm*	*2003*	*2004*	*2005* *100nm*	*2008* *70nm*	*2011* *50nm*	*2014* *35nm*
DRAM										
DRAM 1/2 Pitch *(A)*	180	165	150	130	120	110	100	70	50	35
Critical Defect Size	90	83	75	65	60	55	50	35	25	18
Chip Size *(B)* **(WAS)**	132	138	145	152	159	166	174	199	229	262
Chip Size *(B)* **(IS)**	131	154	179	188	225	265	231	222	197	225
Cell Array Area (%) **(NEW LINE)**	53.0%	53.5%	54.1%	54.7%	55.1%	55.4%	55.8%	56.8%	57.5%	58.0%
Overall Electrical D0 (faults/m^2) at critical defect size or greater *(C)* **(WAS)**	1249	1193	1140	1089	1040	994	950	828	723	630
Overall Electrical D0 (faults/m^2) at critical defect size or greater *(C)* **(IS)**	1261	1073	923	879	734	623	715	744	839	734
Random D0 * (faults/m^2) *(D)*	2826	2700	2580	2465	2355	2250	2150	1875	1636	1426
Random D0 * (faults/m^2) *(D)* **(IS)**	1822	1566	1365	1317	1110	949	1099	1170	1340	1187
# Mask Levels	20	20	20	21	21	21	22	24	25	26
Random Faults/Mask **(WAS)**	141	135	129	117	112	107	98	78	65	55
Random Faults/Mask **(IS)**	91	78	68	63	53	45	50	49	54	46

Table 77: DRAM Yield Model and Defect Budget

DRAM Random Process Induced Defect (PID) Budget (defects/m2) for Generic Tool Type										
scaled to 75nm critical defect size or greater *(E)* (WAS)										
CMP Clean	758	608	480	328	267	215	162	65	27	11
CMP Insulator	1090	875	691	472	385	309	233	93	39	16
CMP Metal	793	637	503	344	280	225	169	68	28	12
Coat/Develop/Bake	306	246	194	133	108	87	65	26	11	4
CVD Insulator	1402	1126	889	608	495	397	299	120	50	21
CVD Oxide Mask	1301	1045	825	564	459	369	278	111	46	19
Dielectric Track	407	327	258	176	144	115	87	35	15	6
Furnace CVD	1453	1166	921	629	512	411	310	124	52	21
Furnace Fast Ramp	508	408	322	220	179	144	108	43	18	7
Furnace Oxide/Anneal	695	558	441	301	245	197	148	59	25	10
Implant High Current	1194	959	757	517	421	338	255	102	43	18
Implant Low/Med Current	1043	837	661	452	368	295	223	89	37	15
Inspect PLY	428	343	271	185	151	121	91	37	15	6
Inspect Visual	484	389	307	210	171	137	103	41	17	7
Litho Cell	472	379	299	205	167	134	101	40	17	7
Litho Stepper	226	181	143	98	80	64	48	19	8	3
Measure CD	469	377	298	203	166	133	100	40	17	7
Measure Film	523	420	331	227	184	148	112	45	19	8
Measure Overlay	428	343	271	185	151	121	91	37	15	6
Metal CVD	680	546	431	295	240	193	145	58	24	10
Metal Electroplate	407	327	258	176	144	115	87	35	15	6
Metal Etch	1581	1269	1002	685	558	448	337	135	56	23
Metal PVD	1013	813	642	439	357	287	216	86	36	15
Plasma Etch	1491	1197	945	646	526	422	318	127	53	22
Plasma Strip	1037	832	657	449	366	294	221	88	37	15
RTP CVD	443	355	281	192	156	125	94	38	16	6
RTP Oxide/Anneal	306	246	194	133	108	87	65	26	11	4
Test	166	134	105	72	59	47	36	14	6	2
Vapor Phase Clean	1108	890	703	480	391	314	237	95	40	16
Wafer Handling	65	52	41	28	23	19	14	6	2	1.0
Wet Bench	1153	925	731	499	407	326	246	98	41	17

Table 77: DRAM Yield Model and Defect Budget

DRAM Random Process Induced Defect (PID) Budget (defects/m2) for Generic Tool Type scaled to 75nm critical defect size or greater *(E)* (IS)										
CMP Clean	518	374	270	186	134	96	88	42	24	10
CMP Insulator	746	539	388	268	192	138	126	60	34	14
CMP Metal	542	392	282	195	140	101	92	44	25	10
Coat/Develop/Bake	209	151	109	75	54	39	35	17	9	4
CVD Insulator	959	693	499	344	247	178	162	78	44	18
CVD Oxide Mask	890	643	463	320	230	165	151	72	40	17
Dielectric Track	278	201	145	100	72	52	47	23	13	5
Furnace CVD	993	718	517	357	256	184	168	80	45	19
Furnace Fast Ramp	347	251	181	125	90	64	59	28	16	7
Furnace Oxide/Anneal	475	343	247	171	123	88	80	38	22	9
Implant High Current	817	590	425	293	211	151	138	66	37	15
Implant Low/Med Current	713	515	371	256	184	132	121	58	32	14
Inspect PLY	293	211	152	105	75	54	49	24	13	6
Inspect Visual	331	239	172	119	85	61	56	27	15	6
Litho Cell	323	233	168	116	83	60	55	26	15	6
Litho Stepper	154	112	80	55	40	29	26	12	7	3
Measure CD	321	232	167	115	83	59	54	26	15	6
Measure Film	358	258	186	128	92	66	61	29	16	7
Measure Overlay	293	211	152	105	75	54	49	24	13	6
Metal CVD	465	336	242	167	120	86	79	38	21	9
Metal Electroplate	278	201	145	100	72	52	47	23	13	5
Metal Etch	1081	781	562	388	279	200	183	87	49	20
Metal PVD	693	501	361	249	179	128	117	56	31	13
Plasma Etch	1020	737	531	366	263	189	173	83	46	19
Plasma Strip	709	512	369	255	183	131	120	57	32	13
RTP CVD	303	219	158	109	78	56	51	24	14	6
RTP Oxide/Anneal	209	151	109	75	54	39	35	17	9	4
Test	114	82	59	41	29	21	19	9	5	2
Vapor Phase Clean	758	547	394	272	195	140	128	61	34	14
Wafer Handling	45	32	23	16	12	8	8	4	2	0.8
Wet Bench	788	570	410	283	203	146	133	64	36	15

(A): As defined in the ORTC Table 1a.

(B): As defined in the ORTC Table 2a.

(C): As defined in the ORTC Table 5a.

(D): Based on assumption of 89.5% Random Defect Limited Yield (RDLY) and peripheral area = (1 - Cell Array Area) times overall chip size.

(E): Random PID Budget Numbers are based on 1999 SEMATECH 150nm RDLY Model Validation Project

Table 78: Technology Requirements for Defect Detection

YEAR TECHNOLOGY NODE	1999[1] 180 nm	2000[1]	2001[1]	2002 130 nm	2003	2004	2005 100 nm	DRIVER
*Patterned Wafer Inspection, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) *[A, B]*								
Process R&D at 300 (cm²/hour) (Was)	54	49	44	39	36	33	30	0.3×DR
Process R&D at 300 (cm²/hour) (Is)	108	98	88	39	36	33	30	0.3×DR
Yield ramp at 3,000 (cm²/hour) (Was)	72	65	59	52	48	44	40	0.4×DR
Yield ramp at 3,000 (cm²/hour) (Is)	144	131	117	52	48	44	40	0.4×DR
Volume production at 10,000 (cm²/hour) (Was)	90	81	73	65	60	55	50	0.5×DR
Volume production at 10,000 (cm²/hour) (Is)	180	160	150	65	60	55	50	0.5×DR
High Aspect Ratio Feature Inspection: Defects other than Residue, Equivalent Sensitivity in PSL Diameter(nm) at 90% Capture Rate. [C]								
All stages of manufacturing (Was)	54	49	44	39	36	33	30	0.3×DR
All stages of manufacturing (Is)	150	136	122	39	36	33	30	0.3×DR
Unpatterned, PSL Spheres at 90% Capture, Equivalent Sensitivity (nm) [D, E]*								
Metal film(Was)	69	63	57	51	47	43	39	0.3×M
Metal film (Is)	138	114	93	51	47	43	39	
Nonmetal films (Was)	54	49	44	39	36	33	30	0.3×DR
Nonmetal films (Is)	108	98	88	39	36	33	30	0.3×DR
Bare Silicon (Was)	54	49	44	39	36	33	30	0.3×DR
Bare Silicon (Is)	108	98	88	39	36	33	30	0.3×DR
Wafer backside	180	163	150	130	120	110	100	DR
Defect Review								
Resolution (nm) [F]	9	9	8	7	7	6	5	0.05×DR
Coordinate accuracy (µm) at above resolution	3	3	2	2	2	1	1	*
Automatic Defect Classification on a Defect Review Platform [G, H]								
Redetection: minimum defect size (nm)	72	65	59	52	48	44	40	0.4×DR
Number of defect types (Was)	5	5	5	10	10	10	15	**
Number of defect types (Is)	3	3	5	10	10	10	15	**
Speed (seconds/defect)	10	10	7	5	5	5	5	
Speed—w/elemental (seconds/defect)	25	25	20	15	15	13	10	

Table 79a: Defect Sources and Mechanisms

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
DRAM ½ PITCH (nm)	180			130			100
MPU GATE LENGTH (nm)	140		100			70	
WAFER SIZE (mm)	300	300	300	300	300	300	300
Sourcing Complexity [A], [F]							
Logic transistor density/mm^2 (1E4)	**7.0**	**9.9**	**14.0**	**17.6**	**22.2**	**30.0**	**40.6**
Number of processing steps	**380**	—	—	**430**	—	—	**480**
Defect sourcing complexity factor (1E6) [B] (Was)	**27**	– –	– –	**76**	– –	– –	**195**
Defect sourcing complexity factor (1E6) [B](Is)	**27**	—	—	**76**	—	—	**195**
Defect sourcing complexity trend [C] (Was)	**1**	—	—	**3**	—	—	**7**
Defect sourcing complexity trend [C] (Is)	***1***	—	—	**3**	—	—	**7**
Data Analysis for Rapid Sourcing							
Defect data volume (#data items/wafer) (1E12) [D] (Was)	**1.9**	—	—	**5.4**	—	—	**14**
Defect data volume (#data items/wafer) (1E12) [D] (Is)	**1.9**	—	—	**5.4**	—	—	**14**
Defect data volume (DV) trend [E] (Was)	**1**	—	—	**3**	—	—	**7**
Defect data volume (DV) trend [E] (Is)	**1**	—	—	**3**	—	—	**7**
Time required to recognize trends (Was)	**Days**	—	—	**Days**	—	—	**Hours**
Time required to recognize trends (Is)	**Days**	—	—	**Days**	—	—	**Hours**
Information sources for automatic data analysis (Was)	**Spatial**	—	—	**Spatial and time**	—	—	**Merge**
Information sources for automatic data analysis (Is)	**Spatial**	—	—	**Spatial and time**	—	—	**Merge**
Transport Modeling							
Gas transport mechanism (Was)	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**
Gas transport mechanism (Is)	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**	**Transitional**
Deposition mechanism (Was)	**Assumed**	**Assumed**	**Assumed**	**Sticking coefficient**	**Sticking coefficient**	**Sticking coefficient**	**Sticking coefficient**
Deposition mechanism (Is)	**Assumed**	**Assumed**	**Assumed**	**Sticking coefficient**	**Sticking coefficient**	**Sticking coefficient**	**Sticking coefficient**
Time to solve for analysis (Was)	**Hours**	**Hours**	**Hours**	**Minutes**	**Minutes**	**Minutes**	**Minutes**
Time to solve for analysis (Is)	**Hours**	**Hours**	**Hours**	**Minutes**	**Minutes**	**Minutes**	**Minutes**

Reference Slides

Technology Requirements:

Yield Model and Defect Budget

- Defect budget requirements for the 1999 180nm technology node use results of a 1999 study of current process-induced defects (PID) at SEMATECH Member Companies.
- Based on the negative binomial yield model
  - Future technology node requirements extrapolated from median PID value for typical tool in each process module by considering increase in area, increase in complexity, and shrinking feature size.

$$PID_n = PID_{n-1} * \frac{F_n}{F_{n-1}\left(\frac{S_{n-1}}{S_n}\right)}$$

PID Extrapolation Equation

Where:
PID = Process Induced Defects (/m^2)
***n* = Technology Node of Interest**
F = Faults per Mask
S = Minimum Defect Size (nm)

Technology Requirements:

Yield Model and Defect Budget

- Previous iterations of the NTRS have assumed that Systematic Limited Yield (Y_S) was 100%.
  - Based on inputs from the chip die size table, microprocessor systematic limited yield (Y_S) is defined to be 80% at the yield ramp phase.
  - Using this and the defined chip area, the microprocessor random fault density (D_0) is calculated.
  - Given the number of mask layers allows for the calculation of allowed random faults per microprocessor mask level.

$$Ysort = Ys * Yr = Ys * \left\{ \frac{1}{\left(1 + \frac{AD}{a}\right)^{a}} \right\}$$

Ysort = Probe Yield
Ys = Systematic Limited Yield
Yr = Random Defect Limited Yield
A = Chip Area (m^2)
D_0 = Electrical Fault Density ($/m^2$)
a **= Cluster Factor**