2000 Test Roadmap Update

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2000 TTWG Members

US Members

Name	Company
Robert Nesbitt	Schluberger

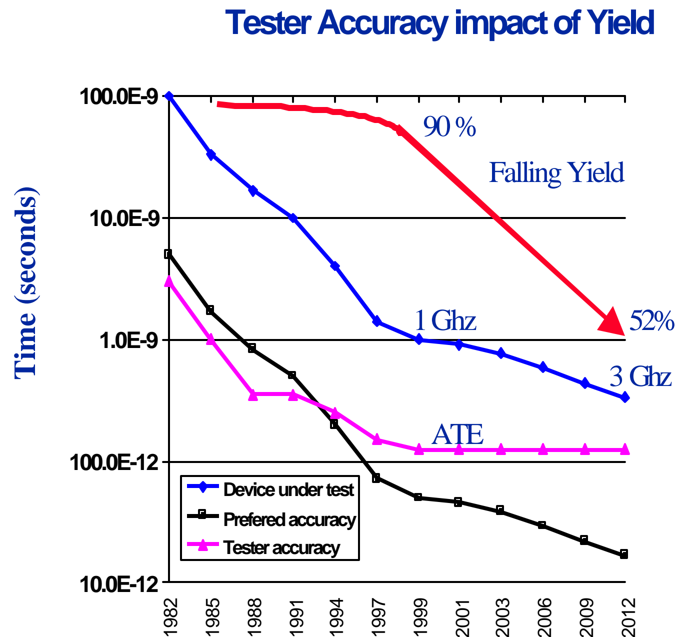
International Members

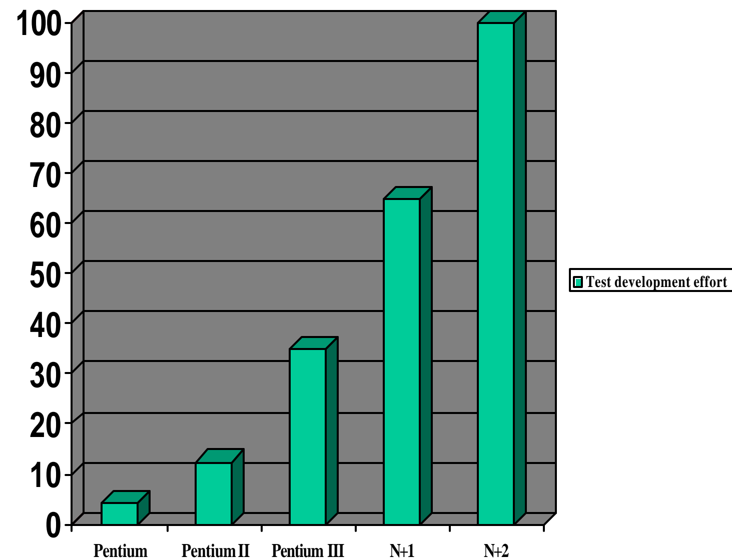
What Were the Issues with Structural Test Implementation in the Past

- Design did not own the problem and test was a relative inexpensive capital investment compared to FAB's
  - **Design's focus was on die size, performance and cost**
    - Adding DFT structures effected all the above
  - **Test did not inhabit the ability to ship parts**
    - Test Engineers could always brute force the test development
    - Interface development below 100 MHz was not an issue (loadboards, probe cards,contractors, etc)
- Test development efforts were relative small compared to design
  - **Test development staff cost was < 10 man years or < $1.5 million**
  - **Device Frequency where < 200 MHz and system accuracy were ok**

Design for Test Mandatory

- Design cannot trade off DFT verses functional test
  - Too expensive to develop functional test
  - Tester will lack the accuracy required for functional test





–Source: ITRS Design TWG

Why Structural Test Now

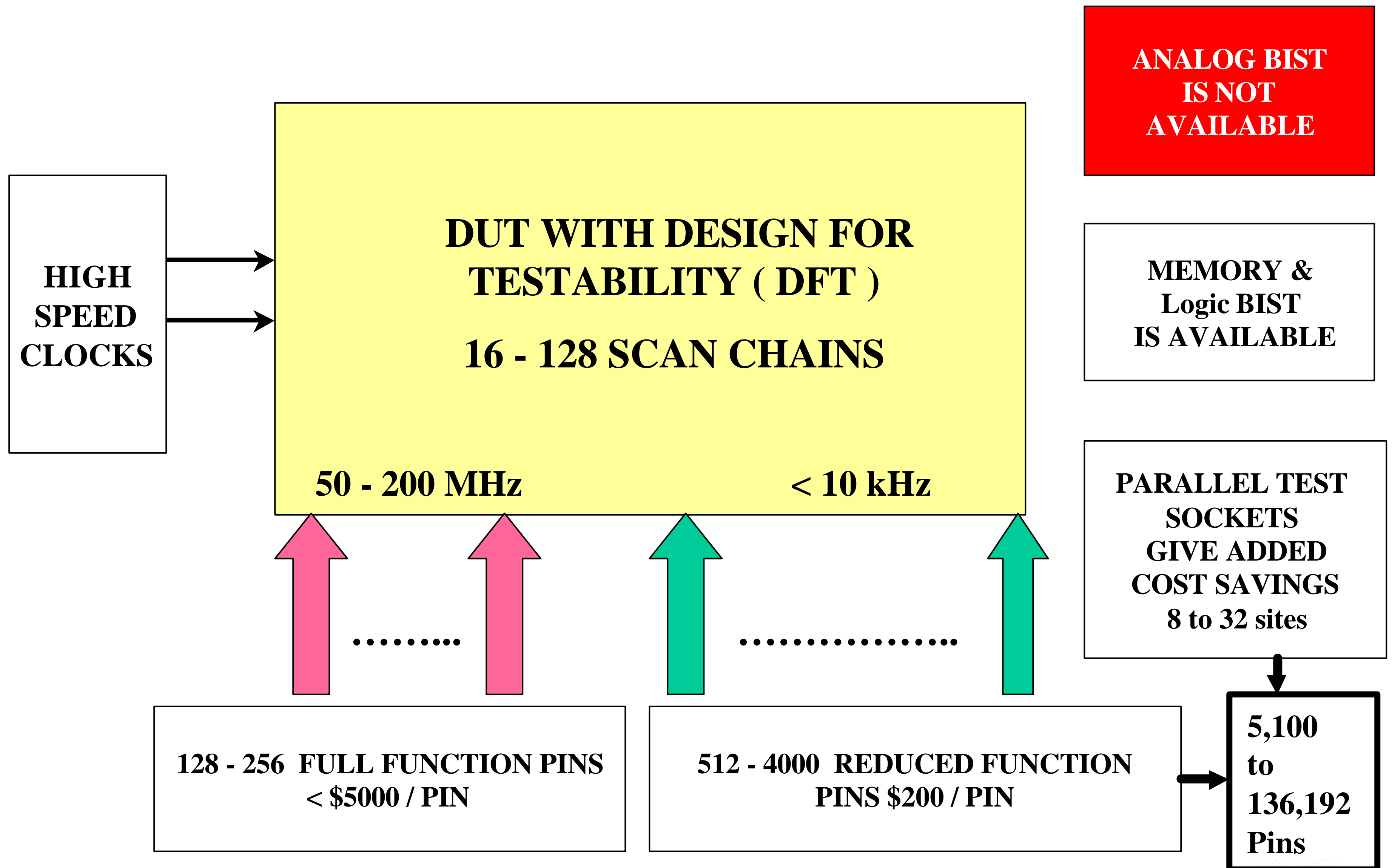
- Design now owns Test and needs to make Test a process
  - **Die size and performance effects of DFT will not be a issues by 100 nm technology node**
  - **Test will inhabit the ability to ship units**
    - >200 MHz Interface development and infrastructure not in place and no industry focus to guide its development (lack of consortium)
    - Tester accuracy will make @speed functional test impractical
    - Test development effort is now 10's of man years and >> $2 m
      - Fault coverage tools for functional test poor
      - Sematech DFT experiment using standard design tools
        - » Function test coverage 52%
        - » Stuct-@, Scan and IDDQ at 95+% fault coverage

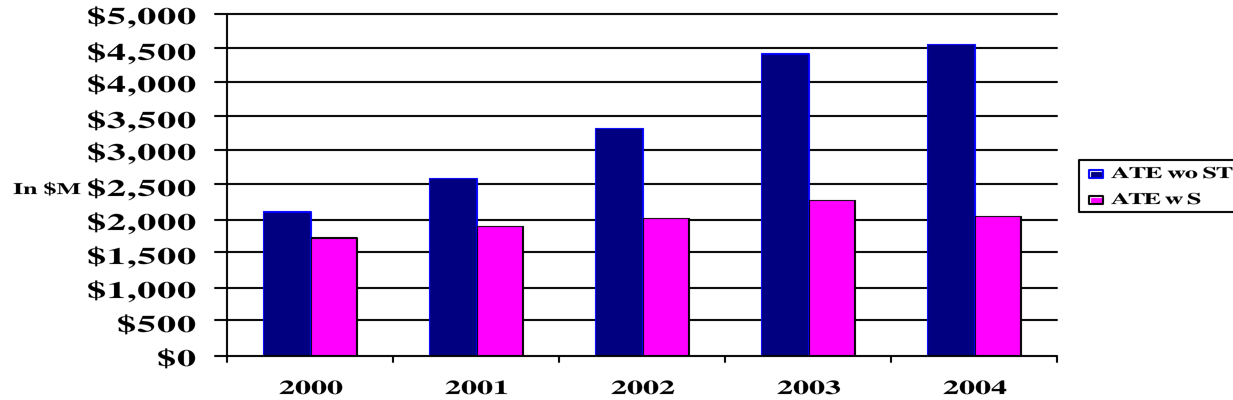
Test TWG 2000/1 Focus/Direction

- **Little Update in 2000 execpt DFT/BIST**
- **2001 Revamp Tables**
  - ✓ Yld Vs Accuracy
  - ✓ High Performance ASIC
  - ✓ High Performance Logic
  - ✓ Low End Logic
  - ✓ Mixed Signal
  - ✓ Commodity DRAM
  - ✓ Commodity Flash
  - ✓ Embedded DRAM
  - ✓ Embedded Flash
  - ✓ DFT/BIST

- ➢ DFT/BIST
- ➢ Memory
- ➢ Characterization
- ➢ Manufacturing
- ➢ SOC ?????
- ➢ Power Management

LOW COST TESTING OF DEVICES DESIGNED WITH DFT




Total Stuructural Test Impact Analysis
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$4,500
$4,000
$3,500
$3,000
In $M $2,500
$2,000
$1,500
$1,000
$500
$0
2000
2001
2002
2003
2004
ATE wo ST
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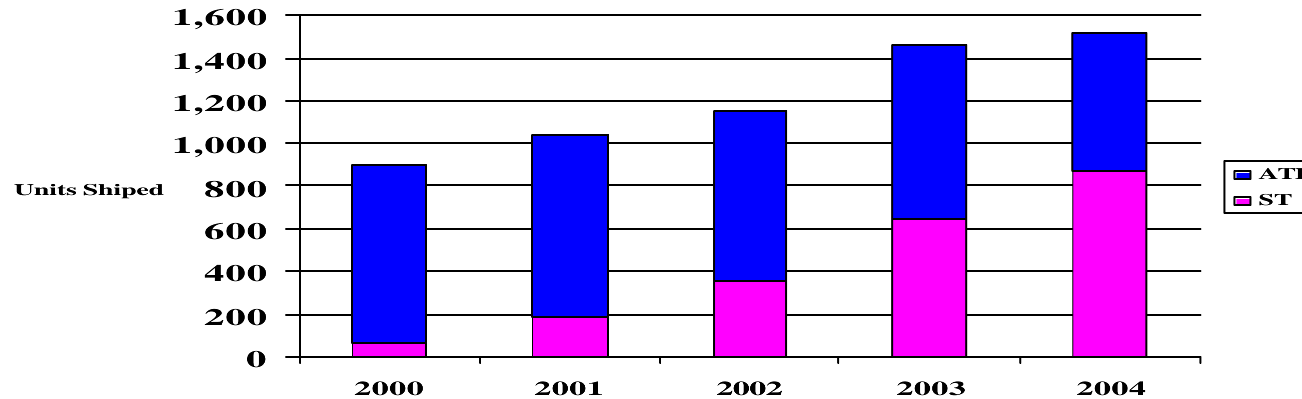
Total ST Shipment Analysis
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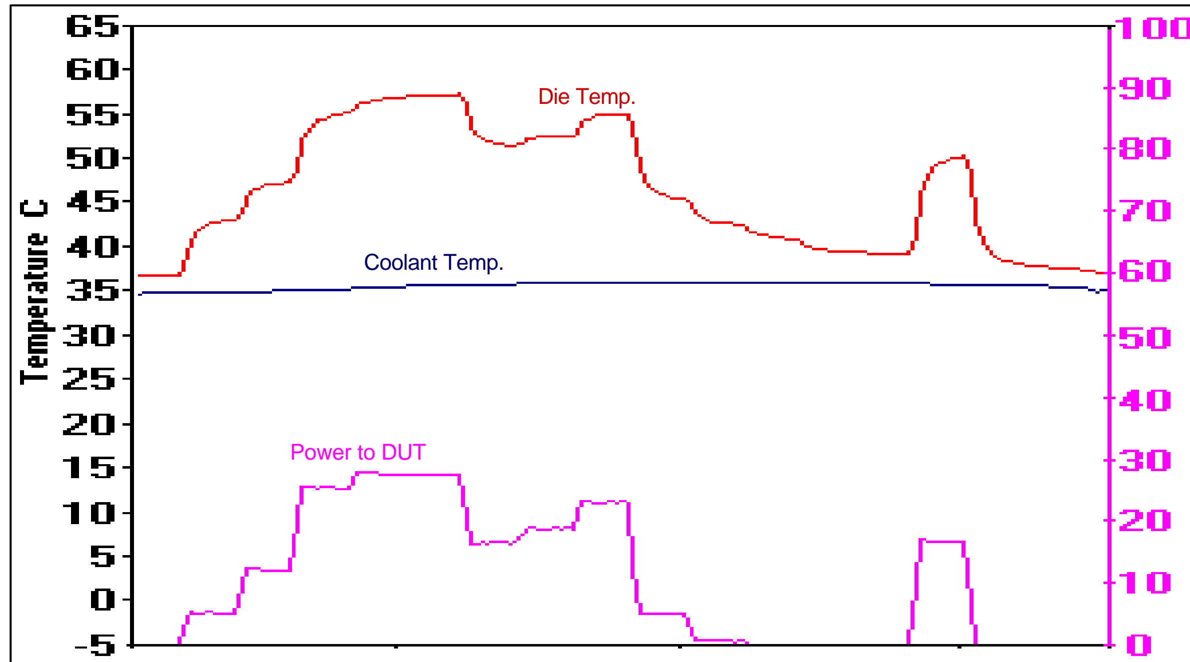
1,400
1,200
1,000
Units Shiped
800
600
400
200
0
2000
2001
2002
2003
2004
ATE
ST

Power/Thermal Management Test Issue



Passive Temperature control

Die temperature deviation: 20°C

Test Cross TWG Issues for Assembly & Packaging, and SOC

- Types of pin interfaces on SOC packages
  - Standard types or will novel interfaces be added (i.e. phone jack, Network Jack etc)
- AC ground return for signals what is the design rule
  - Needs to be 1to1 for greater than 100 MHz
  - Is this a design rule check for design??
- What are the thermal design rules for packages Vs Tj.
  - Device are spec'ed with case temperature but high power mpu's can have up to a 20 O^C change in Tj during test operation.
  - Do we need dynamic thermal control??

Test Cross TWG Issues for Design

- What new type of buss structures are coming ?
  - As transistor counts continue to increase will pin count be reduced because cache requirement for performance will be on chip ?
- How do we make “TEST” a process with all required design rules and interfaces
  - Limited pin count with fixed resources
  - Where in the design process do the test modules need to be inserted ?
  - What EDA systems does Test need to interface or develop API’s for?
  - Will BIST replace scan or will it be some mixed application or do we grow scan memory and scan chains to reduce test time?
- Thermal management will be a problem with testing high powered devices. Holding case temperature constant will allow large swings in Tj
  - Will structural test will require more power than normal device operation?