

ITRS 2000 Update

ORTC Table Node/Chip Size Update Proposals

4/10/2000 - UPDATE 4/19/00, Rev b*

Alan Allan / Intel Corporation

* Update to ICE "Off-the-Shelf" actual cell area analysis

Agenda

- Roadmap Goal Review
- Node/Chip Size Study Group
- Some Key Proposals
 - Scaling Goals
 - DRAM Chip Sizes
 - MPU Chip Sizes
- Summary/Plans

THE 1999 INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS) GOALS:

- Present an **industry-wide consensus** on the “best current estimate” of our future research and development needs out to a 15-year horizon.
- Provide a **guide** to the efforts of research organizations/sponsors (industry, government, and universities.)

...Based on **premise** of continuing the four-decade-long trends of an industry that has distinguished itself by:

- rapid pace of improvement in its **products**
- exponential improvement of manufacturing capability and productivity to reduce the minimum **feature sizes** and **cost/function** used to fabricate integrated circuits.

THE 1999 INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS) Table A:

Improvement Trends for ICs Enabled by **Feature Scaling**

| <u>TREND</u> | <u>EXAMPLE</u> |
|-------------------|--|
| Functionality | nonvolatile memory, smart power |
| Integration Level | components/chip—Moore's Law * |
| Compactness | components/cm ² |
| Speed | microprocessor clock MHz |
| Power | laptop or cell phone battery life |
| Cost | cost-per-function—historically decreasing at >25% / year |

* “the number of components per chip doubles every 18-24 months”

Feature Scaling Enabled by:

- significant R&D investments
- industry-wide learning
- changed industry perception of collaboration
 - “the competitive/pre-competitive boundary.”
 - many R&D partnerships, consortia, and other cooperative ventures.

Node/Chip Size Study Group

- Participants
 - Co-Chairs: John Canning/Litho TWG ; Alan Allan/ORTC
 - Participants: Bob Doering/IRC; Walt Class/FEP; David Jensen/DR; Chi-Shih Chang/A&P; Peter Zeitzoff/PIDS; et al, including Design, FI, IC, Int'l Sematech
- Goal: Evaluate 1999 ITRS ORTC Technology Node and Chip Size trends (including Functions per chip) for update proposals
- Process:
 - Regular teleconferences
 - Gather Data
 - Survey Litho and other TWG members for input
 - Evaluate and develop initial recommendations
- Outcomes:
 - DRAM “Off-the-Shelf” Product Analysis Data (ICE), DRAM Scenarios (Jensen), MPU Data(Chang),
 - Litho TWG Technology Node Trends Recommendation
 - Study Group DRAM Trend Evaluation
 - Study Group MPU Trend Recommendation

ORTC Technology Nodes

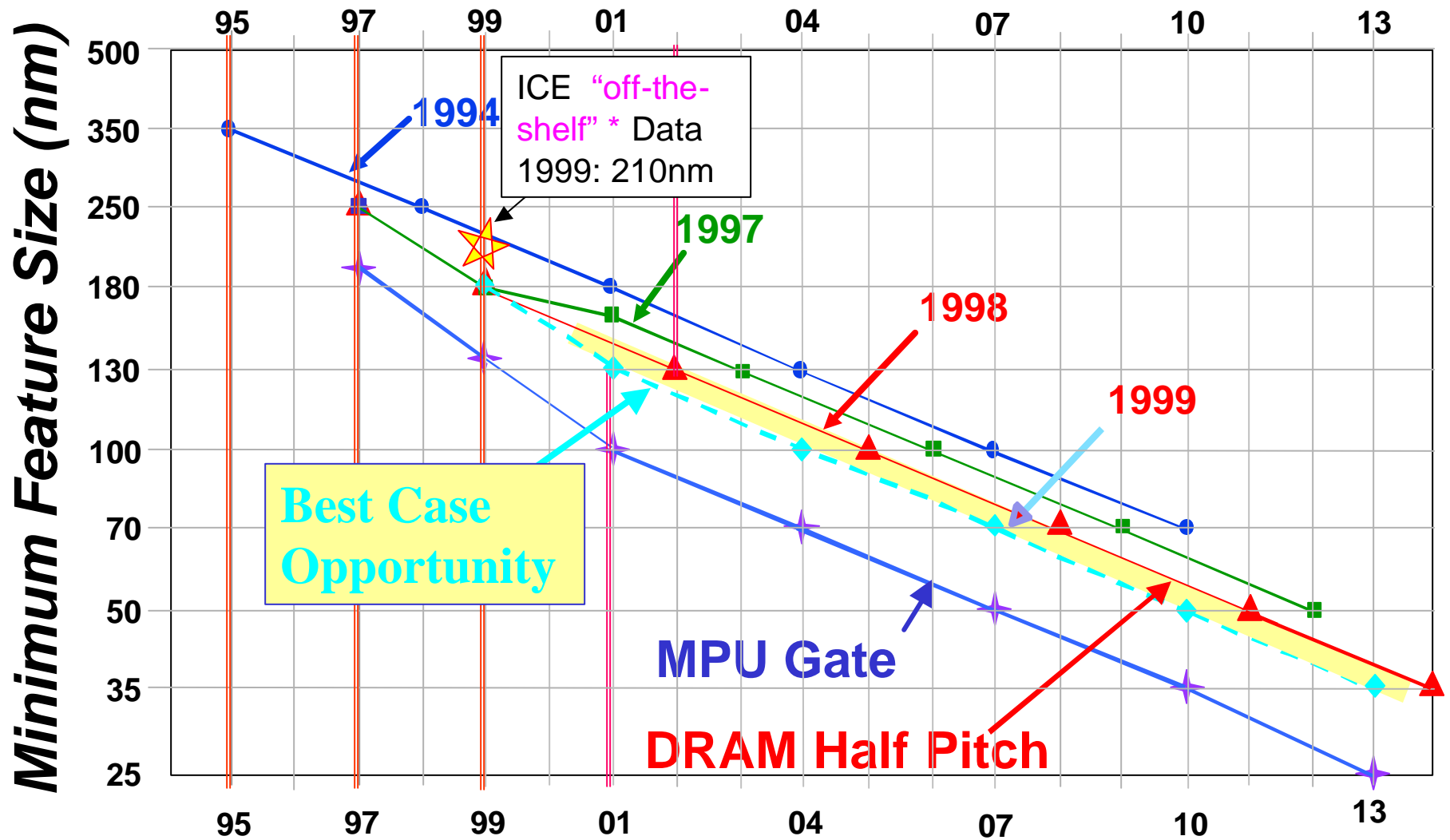
Table 1a Product Generations and Chip Size Model-Near Term Years

| YEAR | 1999 | 2000 | 2001 | 2002 | 2003 | 2004 | 2005 |
|------------------------------|---------------|-------------|-------------|---------------|-------------|-------------|---------------|
| TECHNOLOGY NODE | 180 nm | | | 130 nm | | | 100 nm |
| DRAM ½ Pitch (nm) | 180 | 165 | 150 | 130 | 120 | 110 | 100 |
| MPU Gate Length (nm) | 140 | 120 | 100 | 85-90 | 80 | 70 | 65 |
| MPU/ASIC ½ Pitch (nm) | 230 | 210 | 180 | 160 | 145 | 130 | 115 |
| ASIC Gate Length (nm) | 180 | 165 | 150 | 130 | 120 | 110 | 100 |

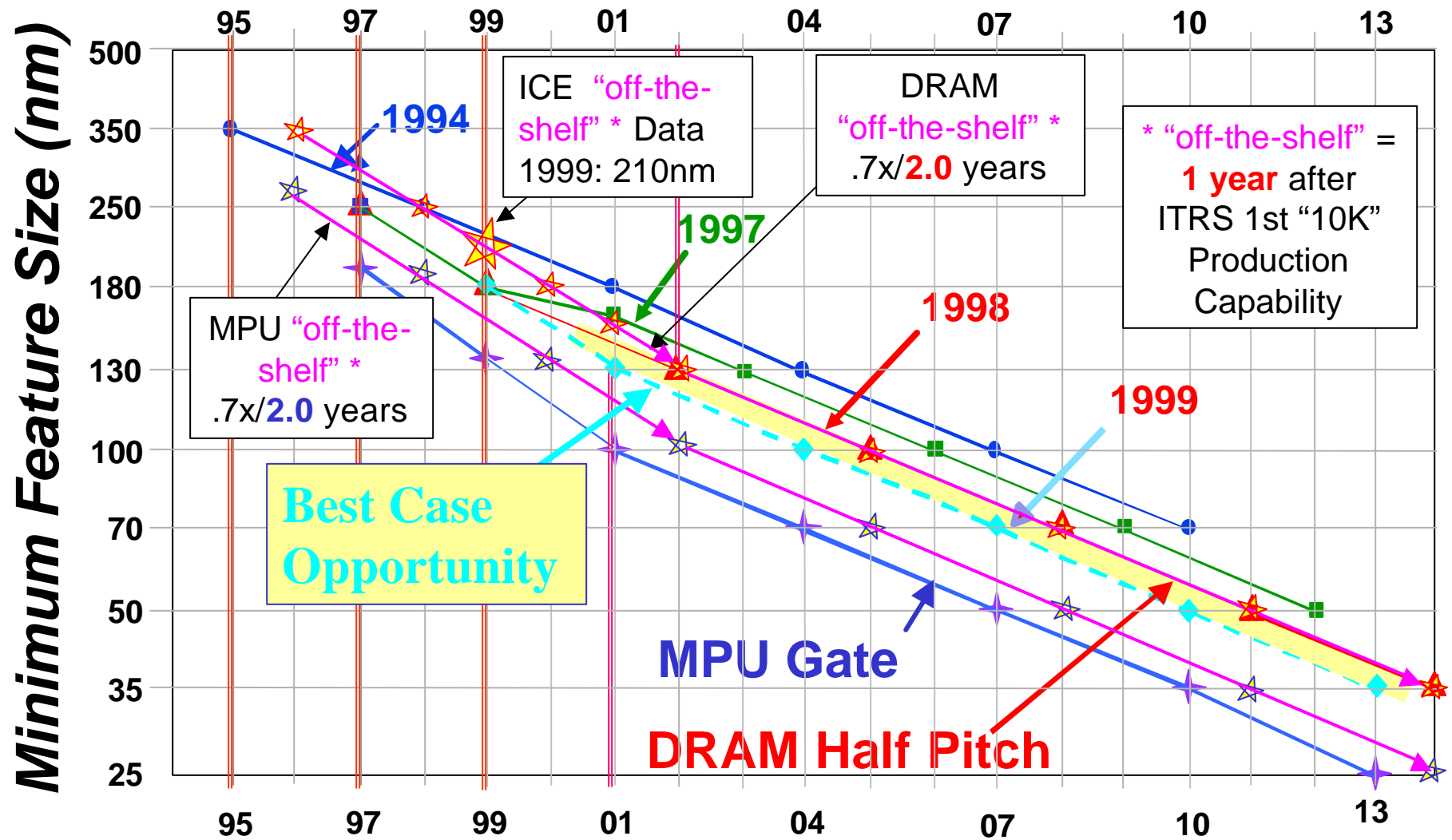
Table 1b Product Generations and Chip Size Model-Long Term Years

| YEAR | 2008 | 2011 | 2014 |
|------------------------------|--------------|---------------|--------------|
| | 70 nm | 150 nm | 35 nm |
| DRAM ½ Pitch (nm) | 70 | 50 | 35 |
| MPU Gate Length (nm) | 45 | 30-32 | 20-22 |
| MPU/ASIC ½ Pitch (nm) | 80 | 55 | 40 |
| ASIC Gate Length (nm) | 70 | 50 | 35 |

ITRS Roadmap Acceleration Continues



ITRS Roadmap Acceleration Continues (including “off-the-shelf” * Product Availability)



ICE Qtrly “Off-the Shelf” Technology “Snapshot” Data Analysis, 4/03/00:

ITRS versus ICE Anaysis Summary:

1999 256M @ Production:

| <u>Trend Target Parameter</u> | <u>ITRS Target</u> | <u>ICE Actual</u> | <u>Corrected</u> <u>ICE Actual</u> |
|--------------------------------------|--------------------|-------------------|---------------------------------------|
| DRAM Half-pitch (nm) (= f) | 180 | 210 | |
| Chip Size (mm ²) | 132 | 161 | |
| Cell Array (% of Total Area) | 53% | 82% | Cell-only 62% |
| Cell Size (micron ²) | 0.26 | 0.48 | Cell-only 0.37 |
| Cell Area Factor (x f ²) | 8x | 11x | Cell-only 8.39x |

1999 128M @ Ramp:

| <u>Trend Target Parameter</u> | <u>ITRS Target</u> | <u>ICE Actual</u> | |
|--------------------------------------|--------------------|-------------------|------------------------|
| DRAM Half-pitch (nm) (= f) | 180 | 210 | |
| Chip Size (mm ²) | 74 | 69 | |
| Cell Array (% of Total Area) | 48% | 83% | Cell-only 62% |
| Cell Size (micron ²) | 0.26 | 0.43 | Cell-only 0.32 |
| Cell Area Factor (x f ²) | 8x | 9.7x | Cell-only 7.26x |

- Latest Actual DRAM product design rules are higher (+17%) => Area should be +36%

- But Actual Chip sizes are ok (within 10-20%)

- Only because **array is greater than 60% of die (increase of 18%-29%)**

- enables the cell area factor to **meet or exceed the target 8x** range

- even though the cell size is **larger** than the target **(by 23%-42%)**

DRAM Chip Size Proposal

- Unchanged at present time (2x bits/chip every 2 years, and 1.2x chip size increase/4years), but....
 - ICE data indicates 200nm/2000, **60%** Array, **7-8x** cell factor
 - Must deal with present 1999 ITRS unrealistic cell area factors (starts yellow 8x Factor in 1999, red= 6.0x by 2003 @ 70% Array@ Intro)
 - Could **use 60% Array Area @ Production for “red” relief**
 - Also, 3 other scenarios evaluated (Jensen excel model):
 - a. Bits/chip fixed at 2x/2yrs, but chip size rate variable
 - b. Bits/chip variable, but chip size rate fixed at 1.2x/4yrs
 - c. Bits/chip fixed at 2x/3yrs, but chip size rate variable
 - Notable results
 - No Red at 1.75x/2yrs bits/chip, 1.2x/4yrs chip size rate
 - **4.0x Factor moved to 2010 by using 1.9x bits/chip, 1.2x/4yrs chip size**
 - 2x/3yrs bits/chip and 1.2x/4yrs to get white (10x) by 2006
 - Need input from DRAM Manufacturers

DRAM Cell Factor - Jensen Model Scenario Chart

| | 1999 | 2000 | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
|--|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| DRAM Technology Node (nm) | 180 | | | 130 | | | 100 | | | 70 | | | 50 | | | 35 | | | 25 | | | 18 |
| MPU Technology Node (nm) | 140 | | 100 | | | 70 | | | 50 | | | 35 | | | 25 | | | 18 | | | 12 | |
| Critical Dimensions (nm) | | | | | | | | | | | | | | | | | | | | | | |
| DRAM 1/2 Pitch | 180 | | | 130 | | | 100 | | | 70 | | | 50 | | | 35 | | | 25 | | | 18 |
| DRAM 1/2 Pitch (modeled) | 180 | 165 | 150 | 130 | 120 | 110 | 100 | 89 | 79 | 71 | 63 | 56 | 50 | 45 | 40 | 35 | 31 | 28 | 25 | 22 | 20 | 18 |
| Logic 1/2 Pitch | 230 | 210 | 180 | 160 | 145 | 130 | 115 | 102 | 91 | 81 | 72 | 65 | 58 | 51 | 46 | 41 | 36 | 32 | 29 | 26 | 23 | 20 |
| Logic Isolated Line | 141 | 119 | 100 | 89 | 79 | 71 | 63 | 56 | 50 | 44 | 40 | 35 | 31 | 28 | 25 | 22 | 20 | 18 | 16 | 14 | 12 | 11 |
| Cell Area Factor (70% Core at Eng Sample) | | | | | | | | | | | | | | | | | | | | | | |
| a) Bit Intro 2x2yr - Die Size 1.2x4yr | 8.0 | 7.1 | 6.3 | 6.3 | 5.4 | 4.8 | 4.3 | 4.0 | 3.7 | 3.5 | 3.2 | 3.0 | 2.8 | 2.6 | 2.4 | 2.3 | 2.1 | 2.0 | 1.9 | 1.7 | 1.6 | 1.5 |
| Bit Intro 2x2yr - Die Size 1.3x4yr | 8.0 | 7.2 | 6.6 | 6.6 | 5.9 | 5.3 | 4.8 | 4.6 | 4.4 | 4.2 | 4.0 | 3.8 | 3.6 | 3.4 | 3.2 | 3.1 | 2.9 | 2.8 | 2.7 | 2.5 | 2.4 | 2.3 |
| Bit Intro 2x2yr - Die Size 1.4x4yr | 8.0 | 7.4 | 6.9 | 7.0 | 6.3 | 5.8 | 5.4 | 5.2 | 5.1 | 4.9 | 4.8 | 4.6 | 4.5 | 4.3 | 4.2 | 4.1 | 3.9 | 3.8 | 3.7 | 3.6 | 3.5 | 3.4 |
| Bit Intro 2x2yr - Die Size 1.5x4yr | 8.0 | 7.5 | 7.1 | 7.4 | 6.8 | 6.3 | 6.0 | 5.9 | 5.8 | 5.7 | 5.7 | 5.6 | 5.5 | 5.4 | 5.3 | 5.3 | 5.2 | 5.1 | 5.1 | 5.0 | 4.9 | 4.8 |
| b) Bit Intro 2x2yr - Die Size 1.2x4yr | 8.0 | 7.1 | 6.3 | 6.3 | 5.4 | 4.8 | 4.3 | 4.0 | 3.7 | 3.5 | 3.2 | 3.0 | 2.8 | 2.6 | 2.4 | 2.3 | 2.1 | 2.0 | 1.9 | 1.7 | 1.6 | 1.5 |
| Bit Intro 1.9x2yr - Die Size 1.2x4yr | 8.0 | 7.3 | 6.7 | 6.8 | 6.0 | 5.4 | 5.0 | 4.8 | 4.6 | 4.4 | 4.2 | 4.0 | 3.8 | 3.7 | 3.5 | 3.4 | 3.2 | 3.1 | 2.9 | 2.8 | 2.7 | 2.6 |
| Bit Intro 1.8x2yr - Die Size 1.2x4yr | 8.0 | 7.5 | 7.1 | 7.3 | 6.7 | 6.2 | 5.9 | 5.8 | 5.7 | 5.6 | 5.5 | 5.4 | 5.3 | 5.2 | 5.1 | 5.0 | 4.9 | 4.9 | 4.8 | 4.7 | 4.6 | 4.5 |
| Bit Intro 1.78x2yr - Die Size 1.2x4yr | 8.0 | 7.5 | 7.1 | 7.4 | 6.9 | 6.4 | 6.1 | 6.0 | 5.9 | 5.9 | 5.8 | 5.7 | 5.7 | 5.6 | 5.5 | 5.5 | 5.4 | 5.3 | 5.3 | 5.2 | 5.2 | 5.1 |
| Bit Intro 1.76x2yr - Die Size 1.2x4yr | 8.0 | 7.6 | 7.2 | 7.6 | 7.0 | 6.6 | 6.3 | 6.2 | 6.2 | 6.2 | 6.1 | 6.1 | 6.1 | 6.0 | 6.0 | 6.0 | 5.9 | 5.9 | 5.8 | 5.8 | 5.8 | 5.7 |
| Bit Intro 1.75x2yr - Die Size 1.2x4yr | 8.0 | 7.6 | 7.3 | 7.6 | 7.1 | 6.7 | 6.4 | 6.4 | 6.4 | 6.3 | 6.3 | 6.3 | 6.3 | 6.3 | 6.2 | 6.2 | 6.2 | 6.2 | 6.2 | 6.1 | 6.1 | 6.1 |
| Bit Intro 1.7x2yr - Die Size 1.2x4yr | 8.0 | 7.7 | 7.5 | 8.0 | 7.5 | 7.2 | 7.0 | 7.1 | 7.1 | 7.2 | 7.3 | 7.4 | 7.5 | 7.6 | 7.6 | 7.7 | 7.8 | 7.9 | 8.0 | 8.1 | 8.2 | 8.3 |
| c) Bit Intro 2x3yr - Die Size 1.1x4yr | 8.0 | 7.8 | 7.7 | 8.3 | 7.9 | 7.6 | 7.5 | 7.7 | 7.9 | 8.1 | 8.3 | 8.5 | 8.7 | 8.9 | 9.1 | 9.3 | 9.5 | 9.8 | 10.0 | 10.3 | 10.5 | 10.8 |
| Bit Intro 2x3yr - Die Size 1.2x4yr | 8.0 | 8.0 | 8.0 | 8.8 | 8.6 | 8.5 | 8.6 | 9.0 | 9.4 | 9.8 | 10.3 | 10.8 | 11.3 | 11.8 | 12.3 | 12.9 | 13.5 | 14.1 | 14.8 | 15.5 | 16.2 | 17.0 |
| Bit Intro 2x3yr - Die Size 1.3x4yr | 8.0 | 8.1 | 8.3 | 9.4 | 9.3 | 9.4 | 9.7 | 10.3 | 11.0 | 11.8 | 12.6 | 13.4 | 14.3 | 15.3 | 16.3 | 17.4 | 18.6 | 19.9 | 21.2 | 22.7 | 24.2 | 25.8 |

MPU Chip Sizes

- No High-Performance MPU Product at 2Mbyte L2 Cache on chip, only one (HP) at 1Mbyte (Chang Data)
 - Recommend starting Die Size Model at 1997 Cost Performance Core + 1Mbyte = $170\text{mm}^2 + 140\text{mm}^2 = 310\text{mm}^2$
 - Maintain the target growth rate maximum of 1.2x/4yrs - same as DRAM
 - Max cache limited to max available Litho field, like ASIC
- Recommend starting all chip size 1.2x/4yrs growth rates start from 1999 (versus flat until 2001) if 130nm node is not pulled in 1 year
- MPU should not drive Litho Field size

Needed IRC/ITWG Approval:

- Node Trend
 - Pull-in DRAM Half-Pitch to 130nm/2001, then 3-year (results in 100nm/2004, 70nm/2007, 50nm/2010, 35nm/2013, 25nm/2016)?
 - Keep DRAM Half-Pitch per 1999 ITRS?
 - Keep MPU Gate-length per 1999 ITRS in either case above?
- DRAM Chip Size Trend
 - Keep 2x Bits per Chip Market Need/"Moore's Law" Target?
 - Use **60%** Array, **8x** Factor @Ramp starting 1999
- MPU Chip Size Trend
 - Keep 2x Transistors per Chip Market Need/"Moore's Law" Target?
 - Start HP MPU at 1Mbyte 310mm²/1999, flat to 2001, then 1.2x/4years?
 - All other trend targets per 1999 ITRS

Plans:

- Finalize Technology Node, Chip Size, and Functional Density Model Consensus with ITWGs and IRC in Brussels - 4/11
- Capture any known ITWG Line Item Updates in Brussels - 4/11
- Revise Technology Node, Chip Size, and Functional Density Models and update ORTC Tables - April
- Forward Updated Rev 1 ORTC Tables to TWGs for 2Q00 Update work, including any known Brussels ITWG revisions - April
- Poll ITWG Chairs and Integrate any 2Q00 ITWG Line Item changes into Rev 2 ORTC Tables - June
- Review Rev 2 ORTC Table WAS/IS at July IRC/ITWG Workshop - July
- Revise Line Items as required and Publish - September

Appendix

ICE Qtrly “Off-the Shelf” Technology “Snapshot” Data Analysis, 4/03/00:

Company A:

128Mb SDRAM, date code 0002.

Die size (edge of scribe lane) 8.4 x 8.2 mm. [68.88 mm²]

Metal 1 1/2 pitch (these are the bit lines) 0.21 micron [= "feature" = f => f² = 0.0441 u²].

Array [incl. Periph. ckts] = 83% of die [57.17mm²/2²⁷ bits = ave cell area = 0.4259 u² = 9.66 f²].

[ICE UPDATE 4/19: Actual cell area = 0.32 u², => 7.26 f², => 62.4% (cell-only) array %]

Company B:

128Mb SDRAM, date code 9942.

Die size (edge of scribe lane) 5.6 x 18.6 mm [104.16 mm²]

Bit line 1/2 pitch (POLYCIDIC, NOT METAL1 !) 0.24 micron [= "feature" = f => f² = 0.0576 u²]

Array [incl. Periph. ckts] = 84% of die [87.49mm²/2²⁷ bits = ave cell area = 0.6519 u² = 11.32 f²].

[ICE UPDATE 4/19: Actual cell area = 0.50 u², => 8.68 f², => 64.4% (cell-only) array %]

Company C:

256 Mb SDRAM, date code 9940.

Die size (edge of scribe lane) 8.75 x 18.4 mm [161.00 mm²]

Metal 1 1/2 pitch (NOT BIT LINE) 0.88 micron, Bit line 1/2 pitch (polycide)

0.21 micron [= "feature" = f => f² = 0.0441].

Array [incl. Periph. ckts] = 82% of die [132.02mm²/2²⁸ bits = ave cell area = .4918 u² = 11.15 f²].

[ICE UPDATE 4/19: Actual cell area = 0.37 u², => 8.39 f², => 61.7% (cell-only) array %]

Source: ICE Corp., Scottsdale, AZ, Tel. 480 515-9780, Fax 480 515-9781; Analysis [] per Alan Allan/Intel, ITRS ORTC Support Team