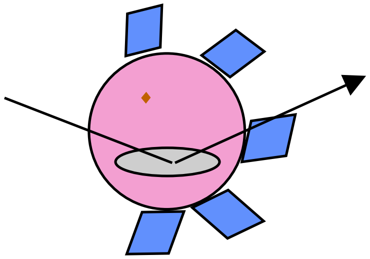
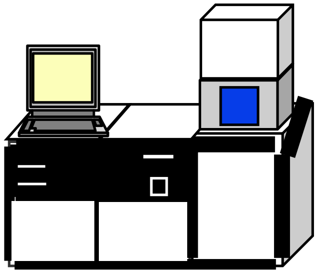
IN-SITU



IN-LINE



OFF-LINE / AT-LINE

2000 Metrology Roadmap

Europe	**Alec Reader (Philips)** **Wilfried Vandervorst (IMEC)**
Japan	**Fumio Mizuno (Hitachi)**
Taiwan	**Henry Ma (EPISIL)** **George Yen (ProMOS)**
US	**Bob Scace (NIST)** **Alain Diebold (SEMATECH)**

Metrology Update Items

- Depth of Focus Metric - Litho CD Measurements
- Address Overlay Box-in-Box Target Issues for Phase Shift and Optical Proximity Correction Masks
- New Devices change metrology
- Add trench sidewall slope and depth (3D) measurement metric (STI, capacitor, trench gate for power device, SOI)
- Adding New Integrated Metrology Requirements for particle detection, end point, and wafer surface temperature
- Improved Pattern Recognition Needed

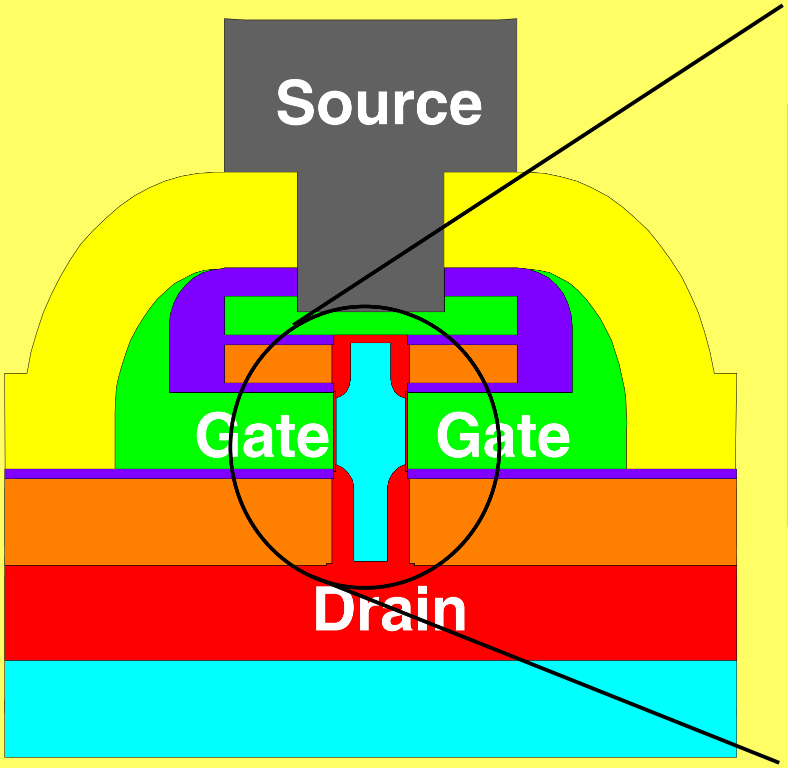
Metrology Update Items

- Add dopant Conc. Gradient specification to Spatial Resolution Metric for 2D Dopant Profiling
- Add to CMP flatness measurement discussion
- Integrated Metrology changes 4Q99: rewrite section
  Include Factory Integration Issues Discussion
- Enhance Materials Characterization Potential Solutions
  - potential solutions for small volume analysis
  - thin film characterization
  - potential solution for 1 nm stress analysis (no known solutions)
- Footnote explaining near term red
- Is reference materials section sufficiently clear about needs for CD reference materials

SEM Depth of Focus Issue

DoF needs to be a Tool Specification Listed in Roadmap

Lithography Metrology



Vertical Transistor

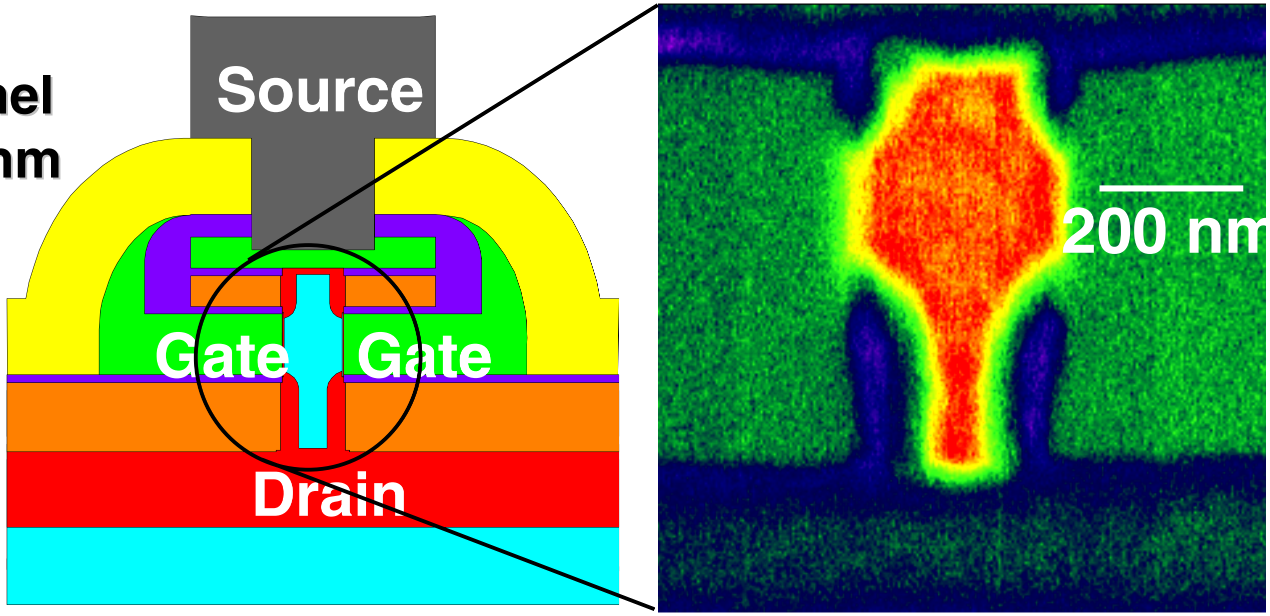
CD is a Film Thickness

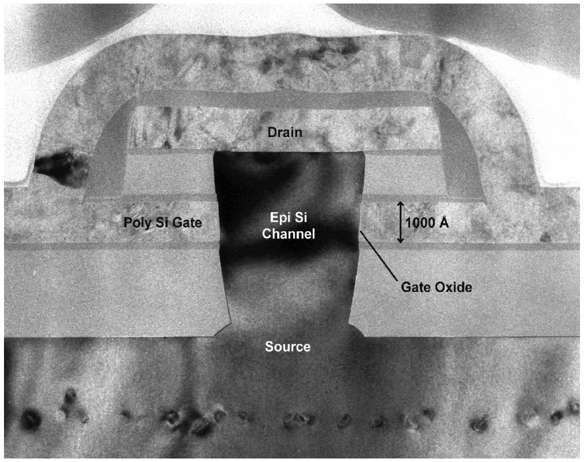
Courtesy
Rafi Kleiman
Lucent

Transistor and Capacitor Metrology

New Transistor Designs vs Metrology

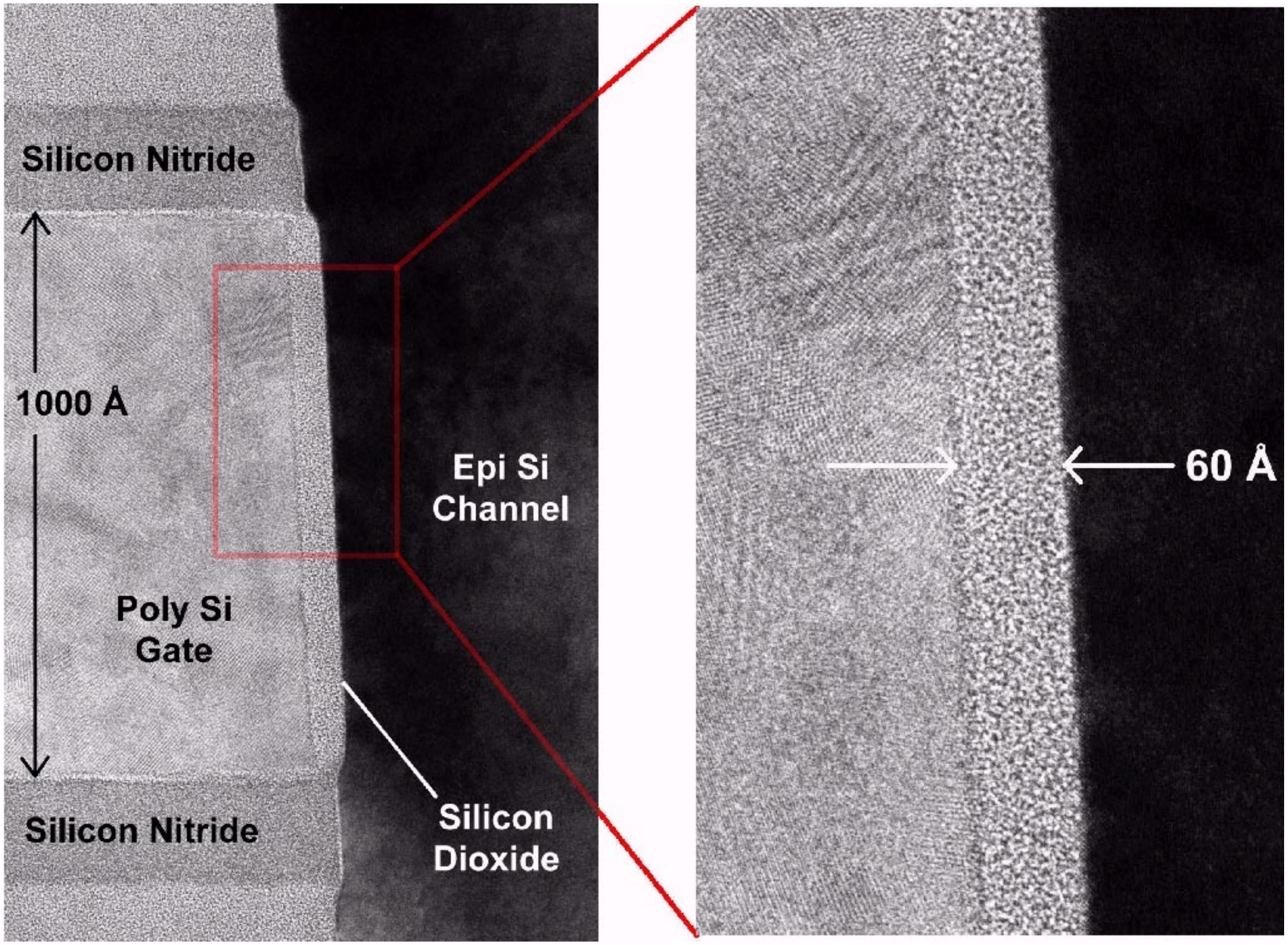
- **Vertical, dual channel Transistor sub 100nm**
- **CD done by film thickness**
- **Doping in LDD by diffusion**
- **Thanks to Rafi Kleiman (Lucent) SCM data is his**





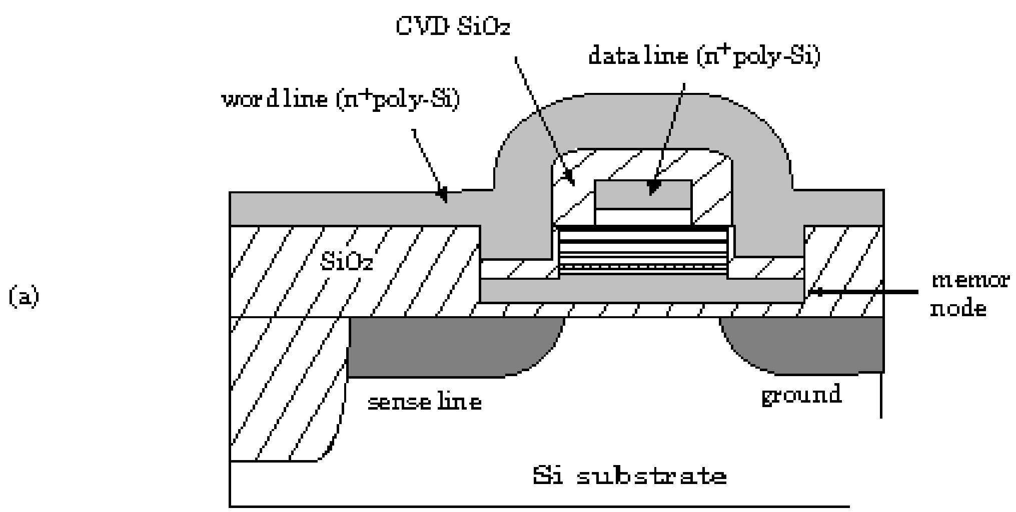
Transistor and Capacitor Metrology

Vertical Transistor : Gate Dielectric is vertical



Transistor and Capacitor Metrology

New Memory Transistor Designs vs Metrology



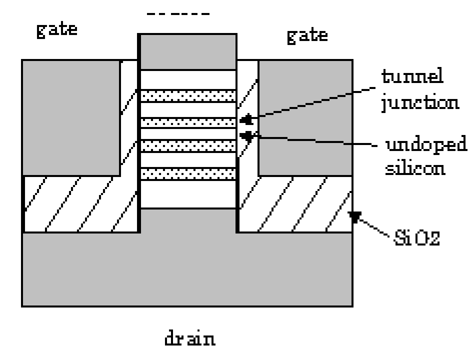


Fig. 4 Cross sectional view of vertical PLED transistor.

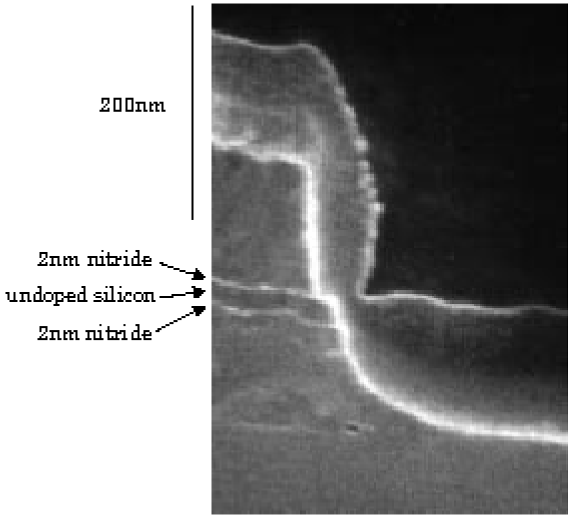


Fig. 5 SEM image of vertical PLED transistor before the formation of the gate electrode.

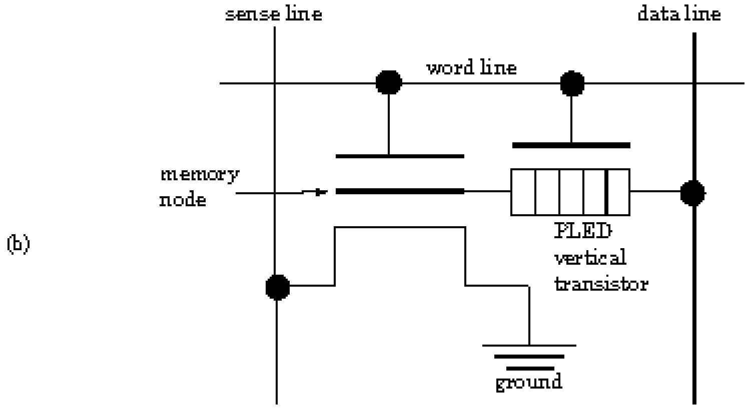


Fig. 8 (a) cross sectional view and (b) equivalent circuit diagram of PLED RAM cell

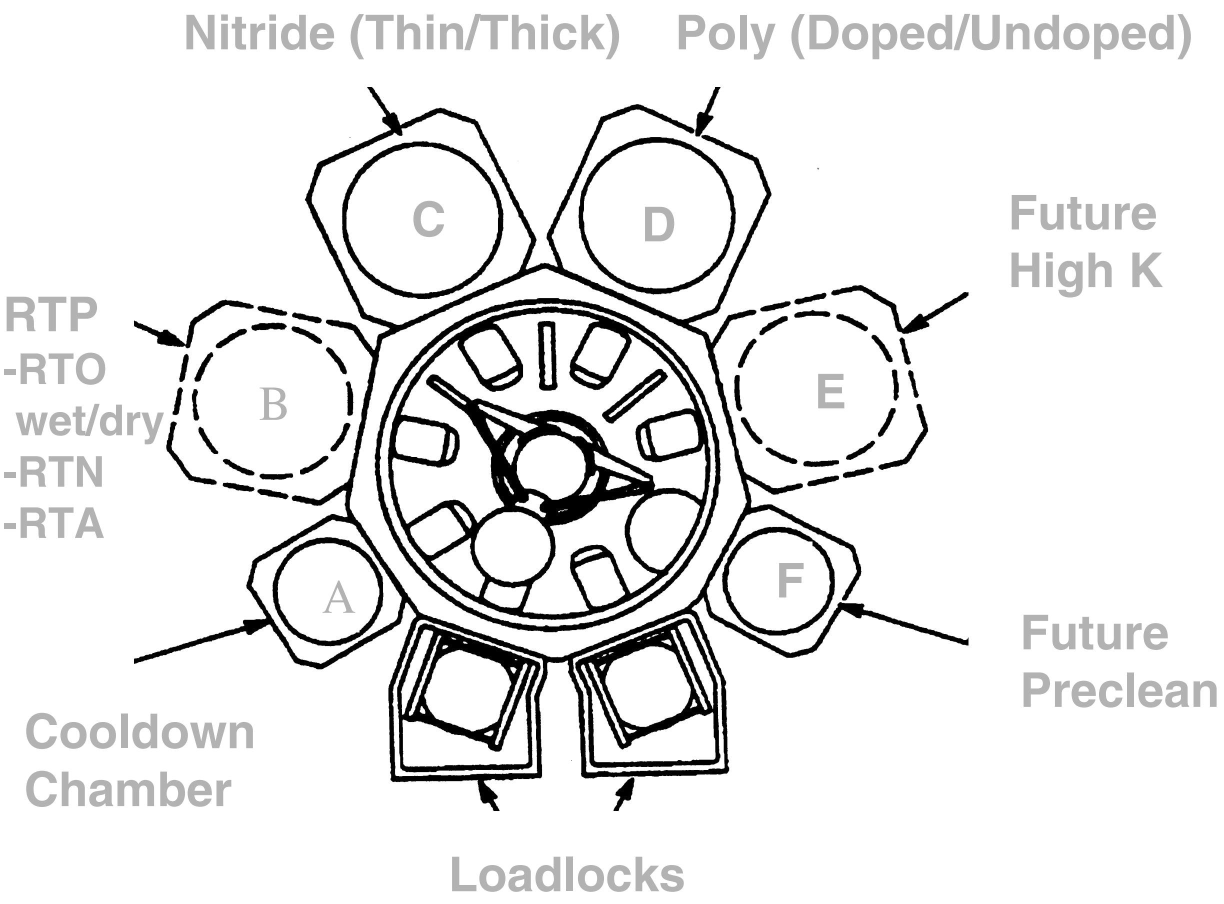
Memory only - PLED Planar Localized Electron Devices
- Nakazato, IEDM 7.7.1, 1997

Front End Process Metrology

Integrated Metrology Trend

Clustered gate dielectric & electrode

e.g., Metal Gate forces in-situ metrology for dielectric



In-situ /on-line Particle Detection for Pure Water and Liquid Chemicals

First Year of Shipment Technology Node	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Critical particle size (nm)	90	65	45	35	25	17
Particle detection limit (nm)	90	65	45	35	25	17

In-situ Film Thickness Measurement for Stacked Metal Layers (CMP End Point Monitor)

First Year of Shipment Technology Node	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
Metal layer Materials	Cubarrier metal film	Cu barrier metal film	Cu barrier metal film	single Cu	single Cu	single Cu
Thickness (nm)	350	274	225	176	137	109
Thickness control (nm, 3)	35	27	23	18	14	11
Measurement precision of film thickness (nm, 3σ, P/T=0.1)	3.5	2.7	2.3	1.8	1.4	1.1
Response time for film thickness measurement 1) (s)	0.035	0.027	0.023	0.018	0.014	0.011
Linewidth of measured metal wire (nm) [2]	180	130	100	70	50	35

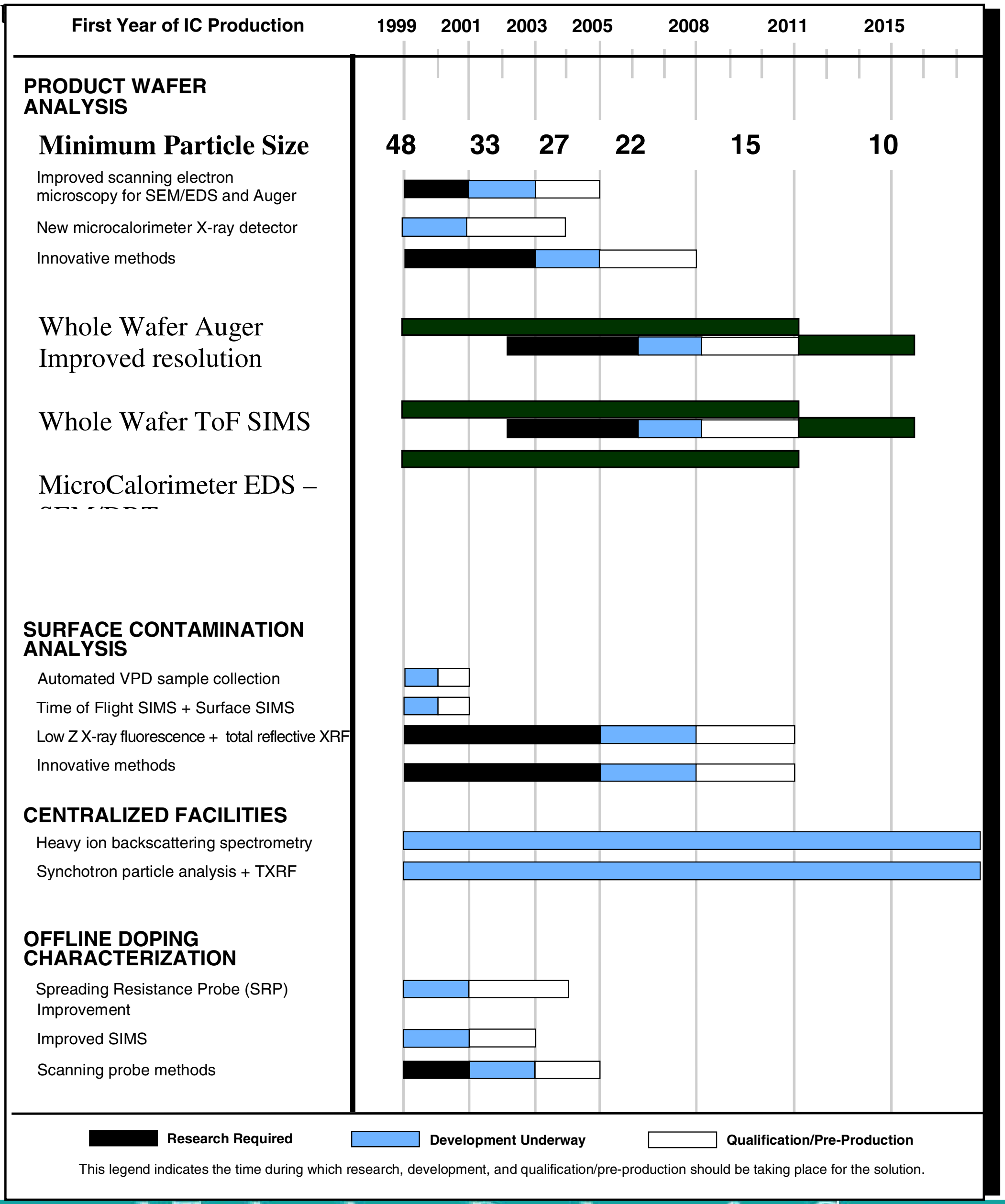
1) The response time requirements have been determined to be 1/10 of each process time required at a Cu CMP speed of 10 nm/s.

2) Film thickness measurements on metal wires are ideal, but if it is impossible the use of measurement patterns would be possible as the second choice. The measurement patterns should be located in the scribe area and have the minimum size of 60 m60 m.

In-situ Wafer Surface Temperature Measurement for RTP and Plasma Process

First Year of Shipment Technology Node	1999 180 nm	2002 130 nm	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
RTP for carrier activation						
Process temperature (°C)	600-1100	600-1000	600-1000	600-900	600-900	600-900
Temperature control (°C, 3σ)	1	1	1	1	1	1
Ramp speed of process temperature (°C /s)	150	200	250	>350	>350	>500
Measurement precision of wafer surface temperature (°C, 3σ)	0.3	0.3	0.3	0.3	0.3	0.3
Spatial resolution for temperature measurement (mm)	1	1	1	1	1	1
Time resolution for temperature measurement (ms) [1]	0.67	0.5	0.4	<0.29	<0.29	<0.2
Plasma process						
Process temperature (°C)	30-500	30-500	30-500	30-500	30-500	30-500
Temperature control (°C, 3σ)	5	5	5	5	5	5
Ramp speed of process temperature (°C /s)	20	20	20	20	20	20
Measurement precision of wafer surface temperature (°C, 3σ)	1.5	1.5	1.5	1.5	1.5	1.5
Spatial resolution for temperature measurement (mm)	1	1	1	1	1	1
Time resolution for temperature measurement (ms) [1]	5	5	5	5	5	5

1) The time resolution requirements have been determined to be P/T=0.1 for each ramp time (s/°C).



🟩

Green Line
means
method
can be used for
that size particle

Requests

- Continued interaction with Interconnect on CMP (Modeling and Simulation points to need for info at short and long surface wavelengths)
- Continued interaction with Litho