Interconnect Working Group

Ogawa-san, Bob Geffken, Simon Jang, Hans Barth, Calvin Hsueh, Aoki-san, Karen Maex, Gerhard Göltz, Dirk Gravesteijn, Christopher Case

IMEC, Leuven, BE

Europe, Japan, Taiwan, US

Agenda

- ITWG region intro
  - regional member update
- 2000 Update timing
- Key issues
- Cross TWG needs
- Table reviews
- First draft needs and assignments
- 2001 advance plans

Technology Requirement Issues

- Reliability requirements
- SOC global wiring pitch
- Usage of "Optional Levels"
- Planarization requirements
- Dielectric metrics including effective κ
- Is aggressive barrier thickness requirement (*i.e.* 0) needed for global wiring level - all 3 tables -
  - no, relax for upper levels

Assignment - Reliability

- Sub group needed -
  - Ogawa-san team leader
    - Tim Sullivan
    - A TI REP
    - Hinode-san (Hitachi)
    - Bob Havemann
    - PIDS representative
- Task
  - Ids Vs operating temperature - what temp to spec
  - via shape and verify the design rules used
  - AC or other operating conditions including pulse/width specs
  - show all "work" i.e. calculations
  - Add back FITS/unit length (with die area defined and line length specified) - show calculations

Assignment - Pitches

- C Case
- Task
  - For SOC adjust global pitch per Taiwan input
  - Distribute for comment to DTWGs
  - Response required by 4 June 2000

Table 48a SoC Interconnect Technology Requirements—Near Term

YEAR TECHNOLOGY NODE	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
MPU ½ pitch (nm)	**230**	**210**	**180**	**160**	**145**	**130**	**115**
Global wiring pitch 1999	**560**			**405**			**285**
Proposed global wiring pitch (nm)	**900**			**650**			**460**

Assignment - Optional Levels

- Sub group needed -
  - Hans Barth team leader
    - An IBM representative
- Task
  - Add text in appendix for MPU table - Optional Levels - use of ground planes and decoupling caps
  - Add in appendix for SOC table - Optional Levels - use of MIM caps, all passive elements

Assignment - Planarization Metric

- Sub group needed -
  - Geffken team leader
    - Gerhard Goltz - look for ST Micro internal experts
    - Calvin Hsueh - provide benchmark information
    - Aoki-san - Japan DTWG views
- Task
  - At what level are dishing and erosion necessary to specify?
  - Can dishing and erosion metrics be combined
  - Interface with Design TWG for parameter impact
  - Is there a PMD planarization issue or need?

Assignment - OK Low k?

- Sub group needed -
  - Karen Maex team leader
    - Carlye Case
    - Bob Havemann
    - Japan representative
    - Dirk Gravesteijn
- Task
  - Select option
    - Change effective k range following Taiwan proposal
    - Add adjacent requirement line which is the bulk κ value which is equal to low end of k range in the aforementioned
    - Correctly verify k needs against RC performance in ORTC table
    - Even if nodes are pulled in keep k as listed in original year of introduction
    - Add footnote stating that the low number in k range represents the very unlikely integration scheme of bulk material not requiring caps/or the use of higher k etch stops
  - Coordinate XCUT dielectric additional metrics

Potential solutions issues

- Identified Barrier Solutions error - ALD atomic layer deposition line was deleted in error
- Terminology “ECP” second and third generation ECD

Assignment - Acronymia

- C Case (with R Geffken)
- Task - write Appendix sections for
  - ECP - describe more in appendix and add footnote to the appendix in Potential Solutions
  - 2nd 3rd generation - describe more in appendix and add footnote to the appendix in Potential Solutions
  - For 2001 - need text rewrite

Overall (IRC) Issues

- Insufficient description of SOC creates problem with using SOC table to represent foundry ASICs
  - considering changing table name or adding footnote defining ASIC/SOC better

FEP Cross Cut Issues

- Need to agree on high κ between *FEP* (both DRAM capacitor and gate dielectric) and interconnect (decoupling and MIM caps). Are the two uses and processes sufficiently different to be included in both TWG potential solutions? Some additional considerations on capacitor performance (linearity, frequency behaviour)
    - Interconnect will own high κ
- Pre - Metal Dielectric
    - Need to address planarization issues associated with pre-metal dielectric
    - *FEP* will own PMD and its planarization

PIDS Cross Cut Issues

- What are issues with high k used in MIM or other interconnect capacitors
  - consider specs for PIDS Table 29
- What is *PIDS* Maximum Wire Length
  - *PIDS* will change nomenclature to Max Signal Local Wire and share with Interconnect
- Review *PIDS* wiring pitches
  - for 2000 update, correct Line 19 Table 28 to show range of pitch from DRAM local to MPU local
- First pass on interconnect needs for novel devices
  - start addressing for 2001

PIDS Cross Cut Issues

- Dielectric leakage and breakdown
  - under *PIDs* consideration
- Can *PIDS* help with Jmax reliability calculations
  - Yes - will join Sub Group on reliability

SOC Cross Cut Issues

- Further clarification of optional levels and role as bypass capacitor, ground plane and use for integrated MIM etc. elements.

Packaging Cross Cut Issues

- Underbump metallurgy for flip chip and wire bond
  - treat in both sections with emphasis on materials compatibility and Cu/low κ integration with *Interconnect* and packaging schemes in *Packaging*
    - Pete Elenius from Packaging
    - R Geffken and H Barth from *Interconnect*
- Major issues
  - list of issues for 2000
  - should receive further treatment in 2001

Design Cross Cut Issues

- Can W at contact meet all design needs for all products?
- What is the value of reducing wiring resistivity from 2.2 to 1.8 μ-Ω-cm?
  - Subgroup task beginning with telecon with *Interconnect*, *Design* and *PIDS*
- Please state requirements for dielectric leakage/length @ operating conditions
  - Capacitor requirements

Modeling Cross Cut Issues

- Design constraints due to process induced variation
- Look at temperature gradient within a level
- Still waiting for global model

Lithography Cross Cut Issues

- Does DOF place any limits at our M0 or M1 level?
  - From Litho - generally not - not necessary to include any special metrics

Random Issues

- Do we need to include final anneal potential solutions?
- Are there top passivation issues
- Control of hydrogen content in processing to avoid dielectric damage and ferroelectric degradation
- Difficult Challenges Table - long term
  - Solutions beyond copper and low κ
    - Material innovation with traditional scaling will no longer satisfy performance requirements. Accelerated design, packaging and unconventional interconnect innovation will be needed.
      - Add: Design of interconnect for novel devices.

Y2k planning

- Multi region video conference held in March 2000
- Validate small change to:
  - Difficult Challenges Table
- ITWG meeting 4 June 2000 San Francisco Airport Hyatt
- Presentation to Linda Wilson for July meeting 25 June 2000

Y2.001k planning

- *Interconnect* needs to address novel devices
- Performance impact of process induced variation
- Parametric performance models
- Can technology metrics be tied to performance limits
  - do you really need 0 barrier thickness and 0 erosion and 1.8 μ-Ω-cm bulk Cu resistivity
  - Trade-offs between low k and metal levels and design rules
- What to do with metrics (pitches for example) in years beyond which Cu/low k do not work

ITRS