

1999 Test & Equipment Roadmap

Test Working Group
Robert Nesbitt (Co-Chair)

1999 TTWG Members

US Members

Name	Company
• Mark Baber	Lucent
• Bill Ortner	Lucent
• Marc Mydill	TI
• Suresh Nadig	Compaq
• Don Weater	IBM
• Paul Roddy	Motorola
• Uli Schoettmer	HP
• Peter Maxwell	HP
• Steve Strauss	Intel
• Brad Robbins	Teradyne
• Phil Nigh	IBM
• Anne Gattiker	IBM
• Robert Nesbitt	Schlumberger
• Jody Van Horn	IBM
• Rochit Rajsuman	Advantest
• Roger Barth	Intel
• Yi Cai	Lucent

International Members

Name	Company
Peter Muhmenthaler	Infineon
Rene Seger	Philips
Kazumi Hatayama	Hitachi
Takeshi Onodera	Sony
Takashi Aikyo	Fujitsu

DIFFICULT TEST CHALLENGES THROUGH 2005

- BIST & DFT
 - Test Equipment will approach \$20 million and yield losses will become unacceptable without BIST & DFT
 - DFT required for @-speed test on low cost tester
 - EDA tools required for inserting DFT/BIST and estimating cost
- DUT to ATE Interface
 - A major road block for development of high-frequency, high pin count probe cards and sockets. Major focus needed to reduce pin inductance and cost.
 - Higher pincounts are leading to larger test heads which impact RTD, size and weight.
 - Power and thermal management problems will be big issue.
 - EDA tools needed to simulate path from device to package to ATE interface.
- Mixed-Signal instruments
 - IC Manufactures must partner with the ATE suppliers for mixed signal ATE requirements
 - Increased digital pin count with RF and lower analog noise levels is a major challenge.

DIFFICULT TEST CHALLENGES THROUGH 2005

- Failure Analysis
 - 3D CAD and FA systems for isolation of defects in further multi-level metal process
 - CAD software for fault diagnosis using new fault models to support DFT/BIST
- Test Development
 - Automatic test program generation to reduce test development time
 - Test standards, such as STIL and IEEE P1500 are needed
 - Reuse of core test for SoC to reduce test development time
 - Simulation of the ATE, interface and DUT avoid test debug on expensive testers
 - Data management needs to be integrated into the test program development

DIFFICULT CHALLENGES BEYOND 2005

- DUT to ATE interface
 - Optical probing techniques
 - Full wafer test
 - Power and Thermal management
 - Contactless probing using BIST/DFT
- SoC Test Methods
 - New DFT/BIST techniques and methods to replace current SCAN/BIST methodology
 - Deterministic self-test instead of pseudo random test patterns
 - Analog BIST
 - Logic BIST for new fault models and failure analysis
 - EDA tools for DFT considering cost/performance issues
- MEMS, Sensors and new IC technologies (SoC driven)
 - Research required
 - New fault models such as noise
 - New EDA tools for diagnosis and failure analysis especially for analog and RF devices

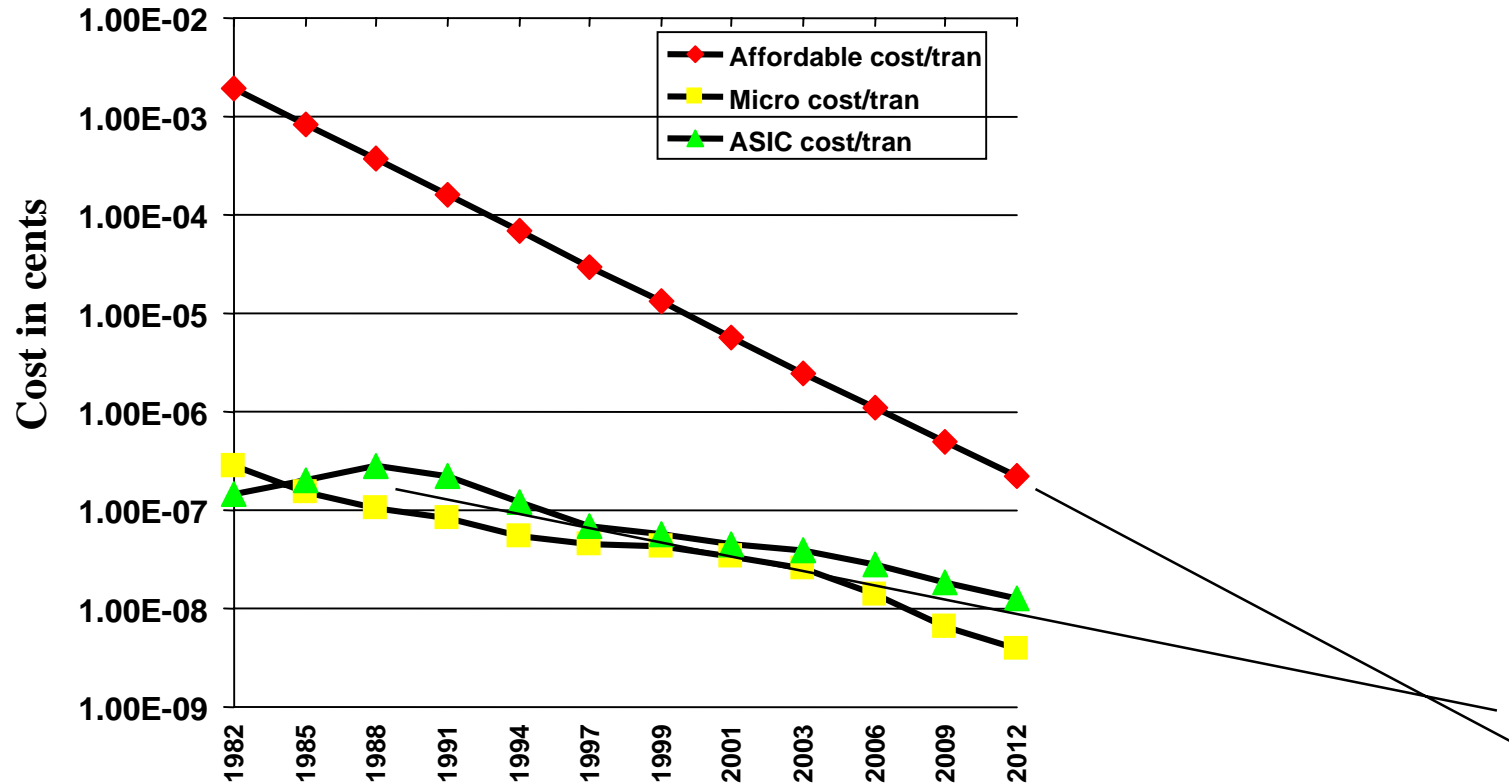
DIFFICULT CHALLENGES BEYOND 2005

- New Burn-in techniques
 - research required
 - Test during burn-in using DFT/BIST capability
- Failure Analysis
 - Real-time analysis of defects in multi-layer metal process
 - New fault models
 - New CAD tools for diagnosis and faults
 - Failure analysis for analog & RF devices

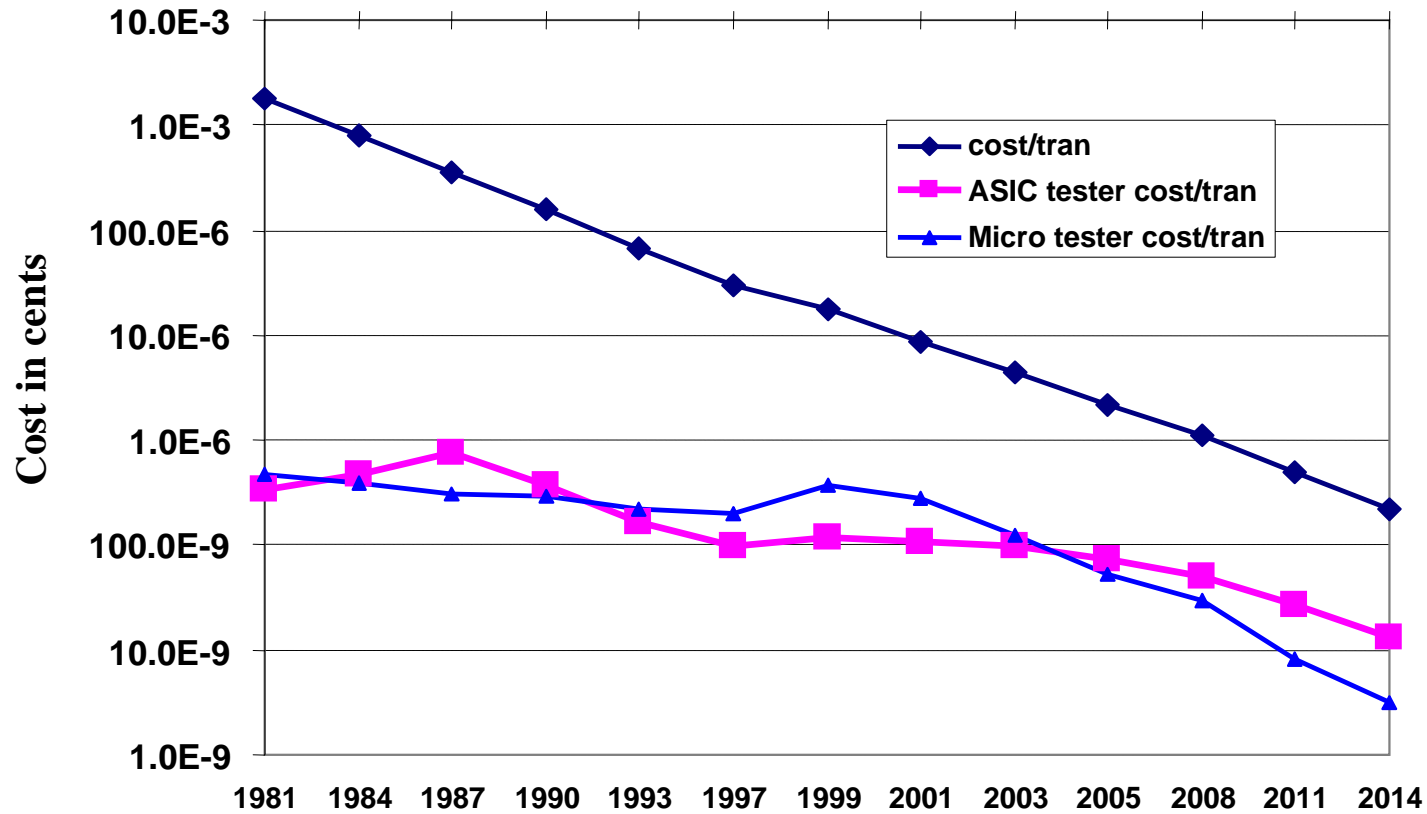
TEST TWG - GENERAL ISSUES

- **Forecasting The Demise Of @Speed Functional Testing**
 - When will DFT/BIST eliminate expensive @speed functional testing
 - The 1997 roadmap forecasted the \$20 M TEST SYSTEM

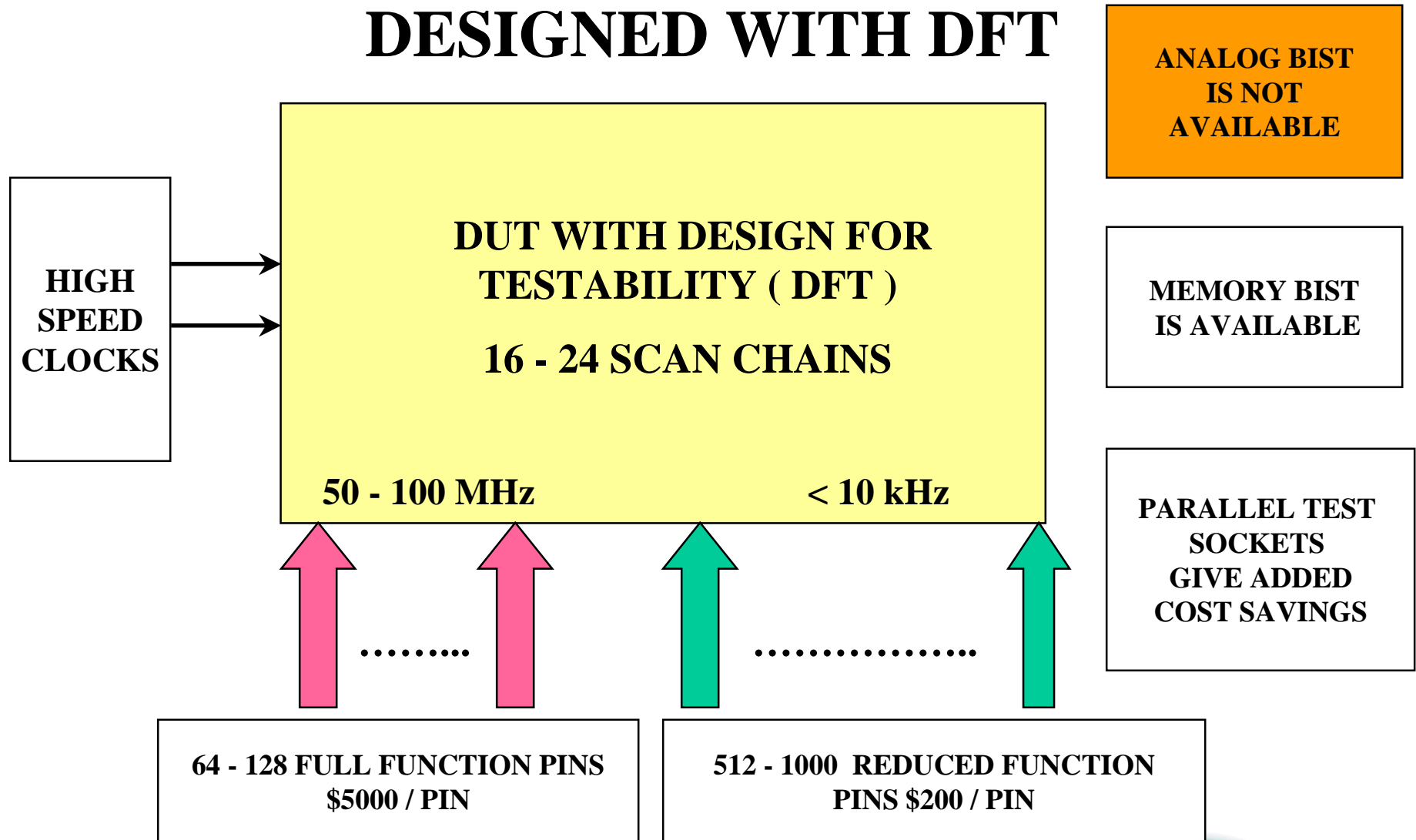
Tester Cost/Transistor/Socket 1997 NTRS



Tester Cost/Transistor/Socket 1999 ITRS

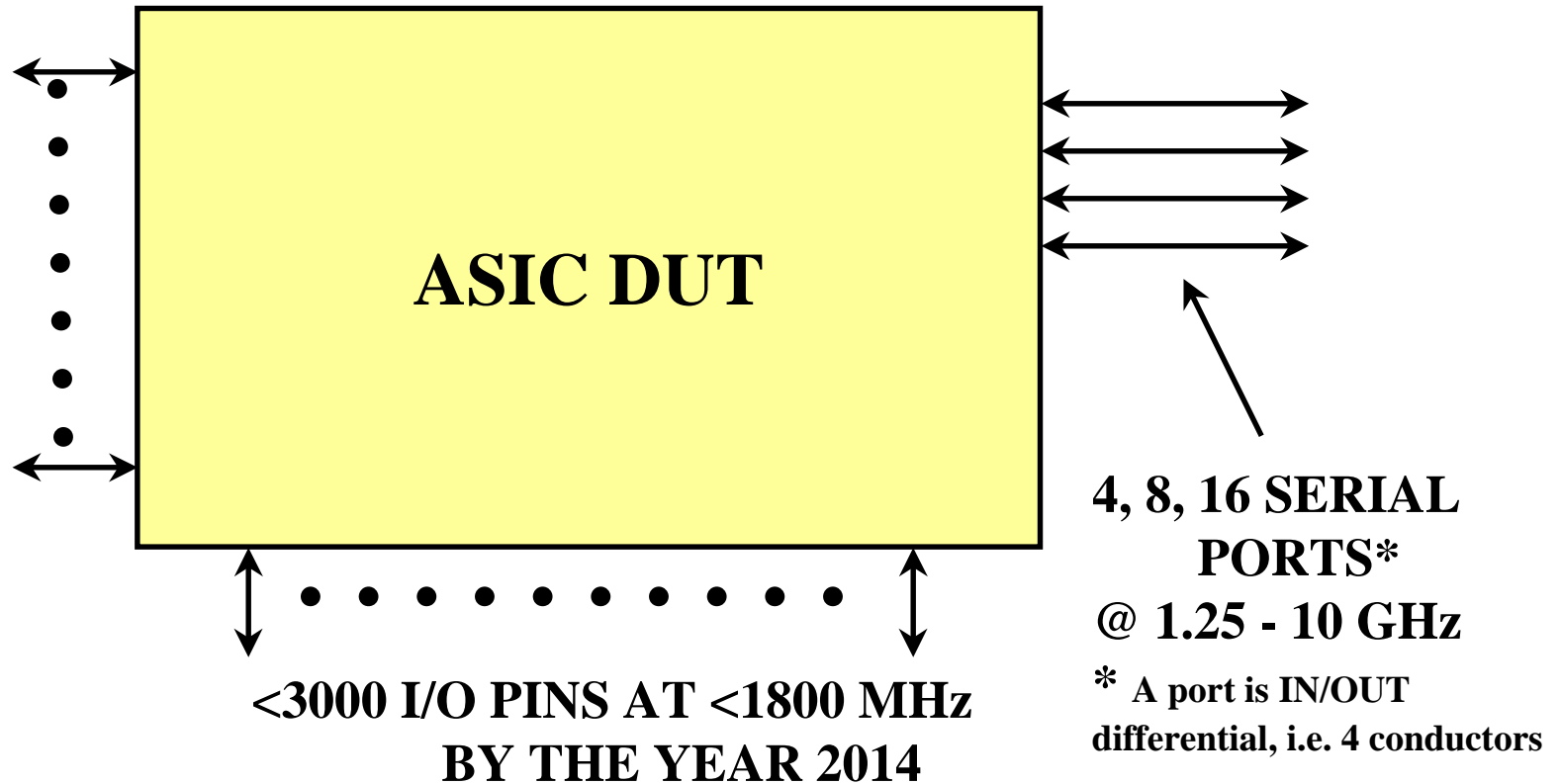


LOW COST TESTING OF DEVICES DESIGNED WITH DFT

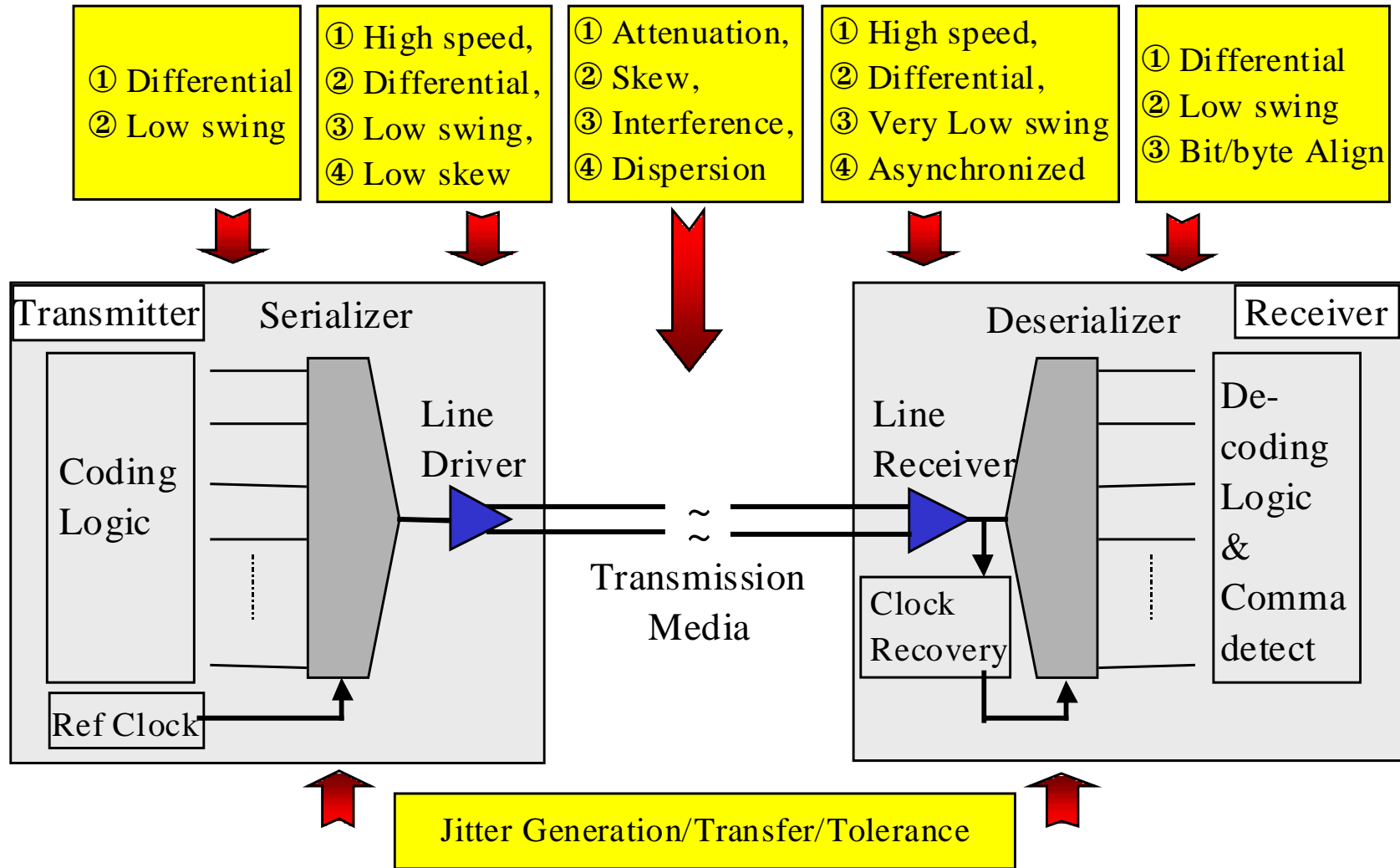


FUTURE ASIC TEST REQUIREMENTS

ATE PIN COUNT AND FREQUENCY FOR MAJORITY OF I/O PINS MAY BE LOWER THAN PREVIOUSLY PREDICTED



Challenges for Testing Serial Communication Devices

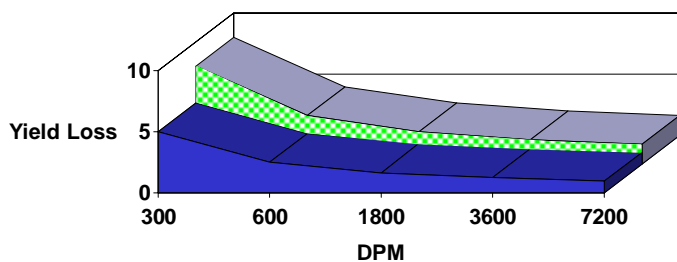
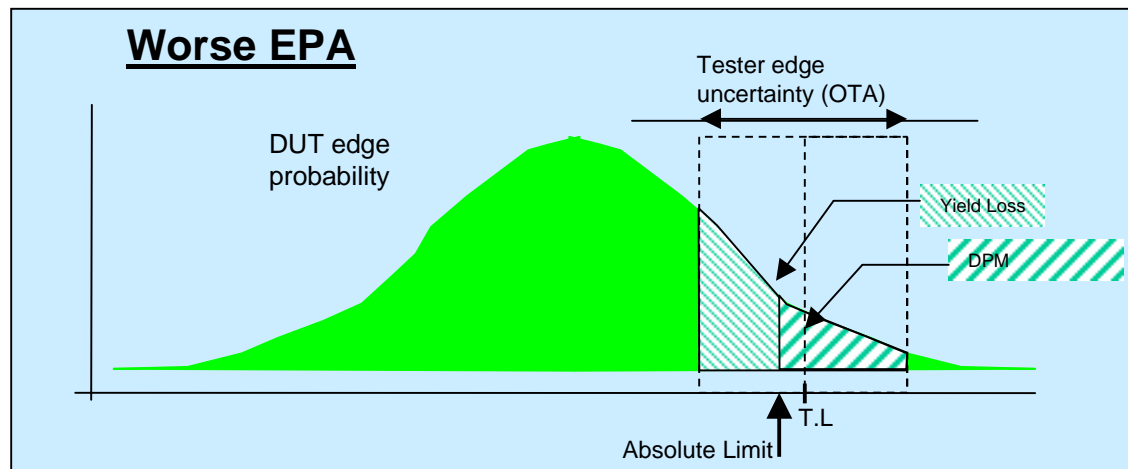
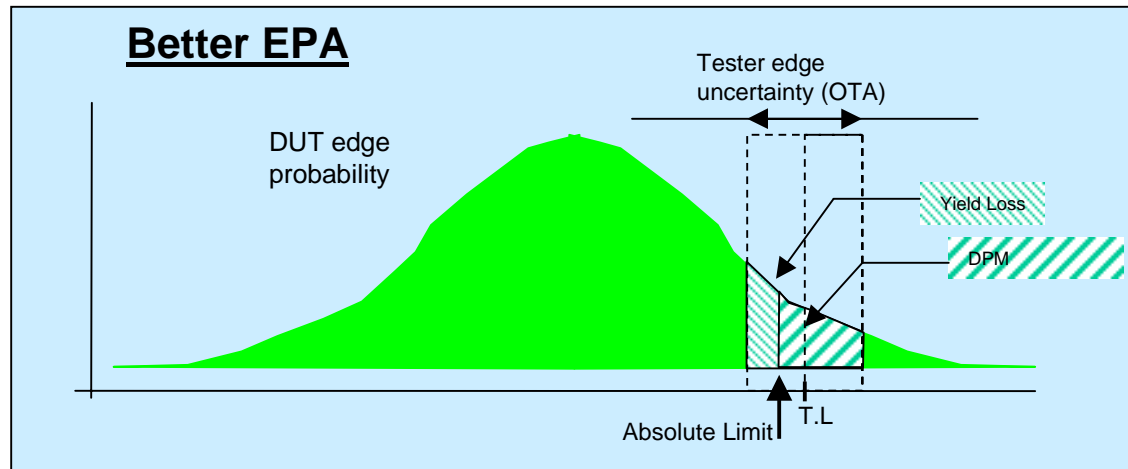


TEST TWG - GENERAL ISSUES

- **Forecasting The Demise Of @Speed Functional Testing**
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 - The 1997 roadmap forecasted the \$20 M TEST SYSTEM
- **To Avoid Falling Wafer and Package Yield due to automatic test equipment (ATE) accuracy limitations.**

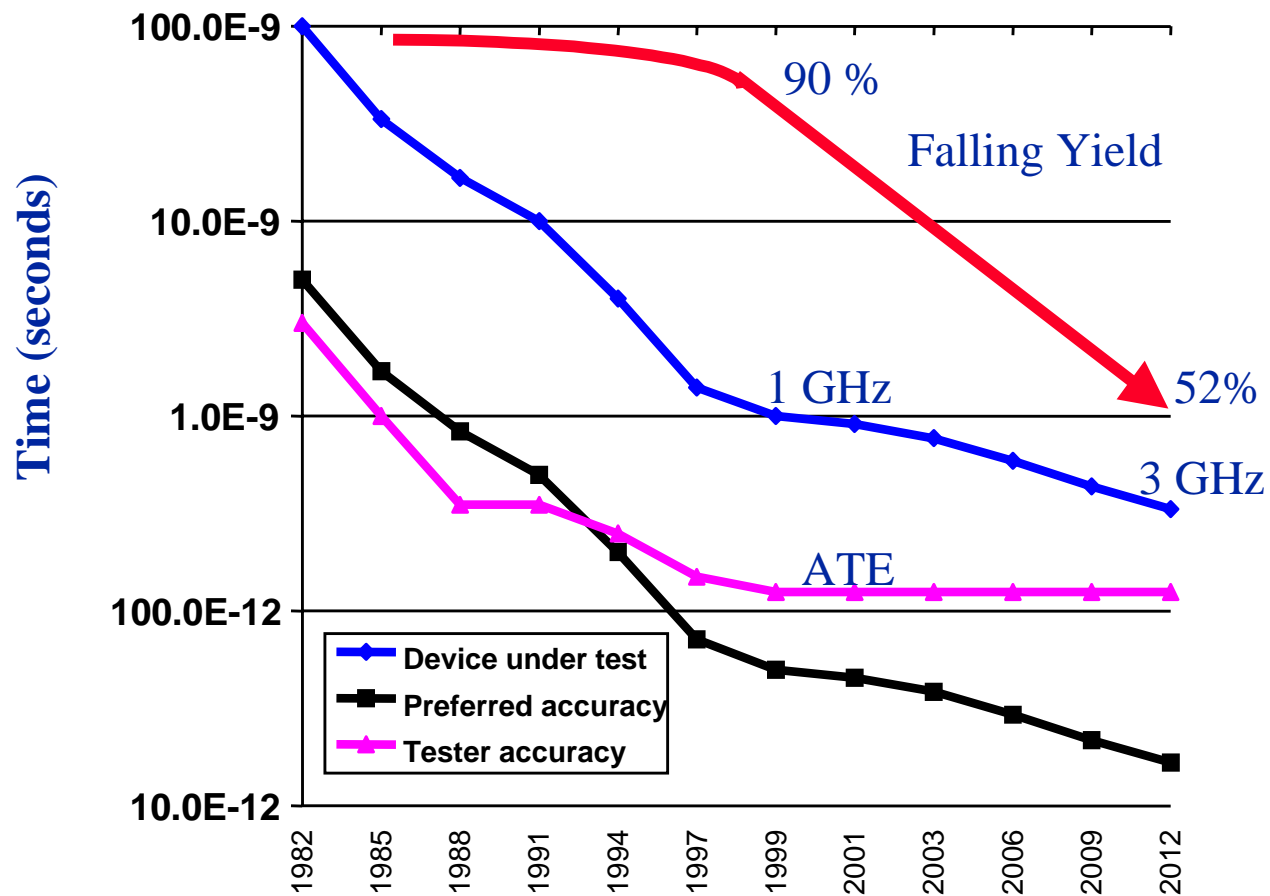
Edge Placement Accuracy (EPA) effect on Yield and Defects Per Million (DPM)

- If yield is <100%: lower tester accuracy, means wider uncertainty box => worse Yield Loss and DPM
- Loosening the test limit moves the uncertainty box to the right: higher yield but higher DPM.
- Tightening the test limit move the box to left: lower yield, but lower DPM.



■ Savings
■ Better EPA ■ Worse EPA

Tester Accuracy impact of Yield



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- **What is the Future Impact for IDDQ as a Test**

IDDQ TESTING; PROJECTED MAX. IDDQ IN HIGH-PERF. ICs

<u>Year</u>	<u>Maximum IDDQ</u>
1999	5 – 10 ma
2001	30 – 70 ma
2003	70-150 ma
2005	150 – 400 ma
2008	400 – 1,600 ma
2011	1,600 – 8,000 ma
2012	8,000 – 20,000 ma

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- **What is the Future Impact for IDDQ as a Test**
- **Power Management May Be the Biggest Single Test Challenge**

Power Management

