

PIDS TWG Report on the ITRS Roadmap Issues

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Outline

- **Difficult Challenges**
- **Memory and Logic Requirements**
- **Analog and Mixed Signal Requirements**
- **Device Reliability**
- **Potential Solutions**
- **SOC Issues**
- **Chip Size Model**
- **Summary**

Near Term Difficult Challenges:

1999 Difficult Challenges

<i>FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005</i>	<i>SUMMARY OF ISSUES</i>
Meeting device performance targets with available gate stack materials	Production worthy high-k dielectrics and compatible gate materials will not be available.
Function integration at low V_{dd}	Crosstalk, substrate noise, and device performance difficult to optimize simultaneously at high clock rates and low V_{dd} .
Managing power, ground, signal, and clock on multilevel coupled interconnect	Despite the use of low-k dielectrics, interconnect scaling is increasing coupling capacitance, crosstalk and signal integrity issues. Power, clock, and ground distribution will consume an increasing fraction of available interconnect.
Management of increasing reliability risks with the rapid introduction of new technologies.	Inadequate identification and modeling of failure modes in new materials, new operating regions (e.g. tunneling) and new SOC technologies (e.g. MEMS)
Integration of precision passive elements	Maintaining high Q, low noise, and tolerances of discrete components.

- **No gate dielectric available for 100nm node (65nm devices)**
- **Meeting device requirements at low V_{DD}**
- **Management of reliability issues with many new materials**
- **Need for precision passive elements**

Long Term Difficult Challenges:

<i>FIVE DIFFICULT CHALLENGES <100 nm / BEYOND 2005</i>	<i>SUMMARY OF ISSUES</i>
Overcoming fundamental scaling limits for current device structures	Switching drive, noise margin, material properties, and reliability will limit performance improvements from scaling
Integration choices for system on a chip	Cost effective process integration of many functions on a single chip.
Atomic level fluctuations and statistical process variations	Possible reduction of yield and performance below desired levels due to unacceptable statistical variations.
Design for manufacturability, reliability, and performance.	Inadequate smart design tools that incorporate integration challenges in process control, proximity effects, reliability, performance, etc.
Low power, low voltage, high performance, and reliable nonvolatile memory element	NVM program and erase require voltages which are incompatible with highly scaled low voltage devices

- **Scaling limits will reduce performance of devices and memory cells**
- **SOC issues will cause difficult integration problems as well as the need for smart design tools to design around process limitations**
- **Atomic level fluctuations causing unacceptable statistical variation**

Memory and Logic Requirements(1)

	<i>Year of First Product Shipment Technology Node</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>	<i>2008 70nm</i>	<i>2011 50nm</i>	<i>2014 35 nm</i>
2	MPU Gate Length (nm)	140	120	100	85	80	70	65	45	32	22
3	MPU /ASIC Half Pitch (nm)	230	210	180	160	145	130	115	80	55	40
4	ASIC Gate Length (nm)	185	165	150	130	120	110	100	70	50	35
5	Min. Logic V _{dd} (V) (desktop)	1.5-1.8	1.5-1.8	1.2-1.5	1.2-1.5	1.2-1.5	0.9-1.2	0.9-1.2	0.6-0.9	0.5-0.6	0.3-0.6
6	Tox equivalent (nm)	1.9-2.5	1.9-2.5	1.5-1.9	1.5-1.9	1.5-1.9	1.2-1.5	1.0-1.5	0.8-1.2	0.6-0.8	0.5-0.6
7	Nominal I _{on} @25°C(μA/μm)[NMOS/PMOS] High Performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	750/350	750/350	750/350
8	Max I _{off} @25°C(nA/μm) (For min. L device) High Performance	5	7	8	10	13	16	20	40	80	160
9	Percent Static Power Reduction Necessary due to Innovative Circuit/System Design	0	33	48	55	71	77	81	91	97	98
10	Nominal I _{on} @25°C(μA/μm)[NMOS/PMOS] Low Power	490/230	490/230	490/230	490/230	490/230	490/230	490/230	490/230	490/230	490/230
11	Max I _{off} @25°C (pA/μm) (For min. L device) Low Power	5	7	8	10	13	16	20	40	80	160
12	Percent Static Power Reduction Necessary due to Innovative Circuit/System Design	0	36	55	65	80	85	88	95	98	99

- Device scaling will end without new gate stack materials
- Simultaneously satisfying I_{on} and I_{off} needs will require new materials and structures

Memory and Logic Requirements (2)

	<i>Year of First Product Shipment Technology Node</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100nm</i>	<i>2008 70nm</i>	<i>2011 50nm</i>	<i>2014 35nm</i>
1	DRAM Half Pitch (nm)	180	165	150	130	120	110	100	70	50	35
21	DRAM cell size (μm^2)	0.26	0.19	0.14	0.105	0.08	0.058	0.004	0.018	0.0072	0.0030
22	DRAM Cell Dielectric Tox Equivalent (nm)	3.0	2.2	1.6	1.2	0.9	0.67	0.50	0.20	0.084	0.034
23	DRAM Retention Time (ms)	250	250	250	250	250	250	250-500	250-500	250-500	250-500
26	NOR Cell Size (mm ²)	0.34	0.29	0.24	0.17	0.15	0.13	0.1	0.05	0.025	0.012
27	+/- Vpp	8-10	8-10	8-9.5	8-9.5	8-9.5	7-9	7-9	7-8.5	6.5-8.5	6-8.5
28	Tunnel Oxide (nm)	8-10	8-10	8.5-9.5	8.5-9.5	8.5-9.5	8-9	8-9	7.5-8.5	2-8	2-7

- Requirements for DRAM cell size scaling will quickly reach the limit of the current approaches
- Drive a change in material, cell design, and memory architecture

Analog and Mixed Signal Requirements

1	Year of Introduction Technology Node	1999 180 nm	2000	2001	2002 130nm	2003	2004	2005 100nm	2008 70nm	2011 50nm	2014 35nm
2	Minimum Digital Supply Voltage (V)	1.8-1.5		1.5-1.2			1.2-0.9		0.9-0.6	0.6-0.5	0.5-0.3
3	Minimum Analog Supply Voltage (V)	3.3-2.5	2.5-1.8						1.8-1.5		1.5
4	RF Frequency (GHz)	0.9-2.5	0.9-10							0.9-100	
5	Analog Frequency (GHz)	<0.1	0.1-5							0.1-10	

- Analog and mixed signal difficulties are compounded at low voltages.
- Excessive analog power dissipation under reduced signal swing conditions must be addressed.
- Precision passive elements will be very difficult to fabricate.

Device Reliability

- **Chip reliability levels are maintained while the technology undergoes massive changes**
(Early Failures, Long Term Failures, Soft Error Rate etc.)
- **Reliability Infrastructure is not prepared for new material introductions**
- **Lead Time for new technologies is long for reliability evaluations**

Potential Solutions

Logic : High-k dielectric, Metal gate
Switched Vt, Dynamic Vt
SOI
Low-k dielectric

DRAM : High-k cell dielectric
Open Bitline, Gain cell
Multi-state logic

Storage Devices : FeRAM etc.

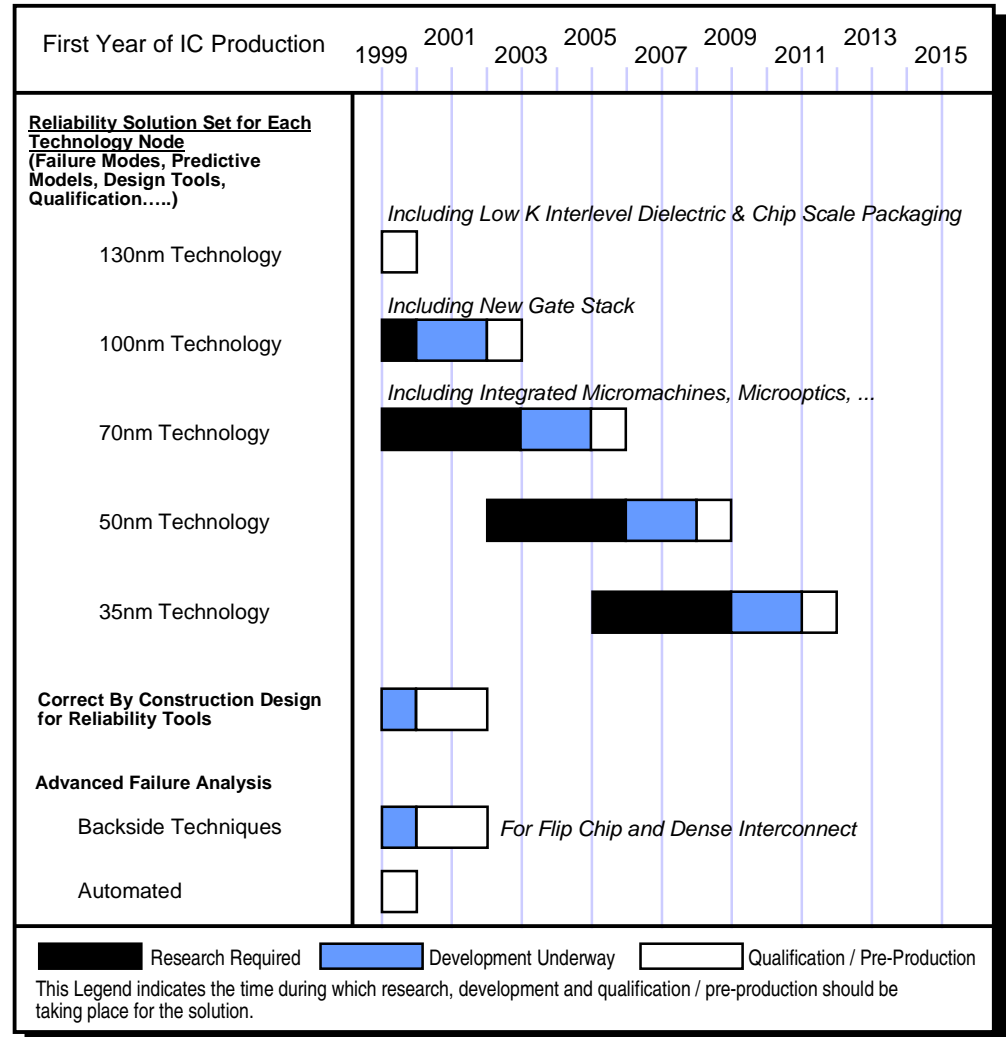
Analog & Mixed Devices : Passive elements
(Inductors, Resonators, Capacitors)
MEMS, SOI

Reliability Potential Solutions

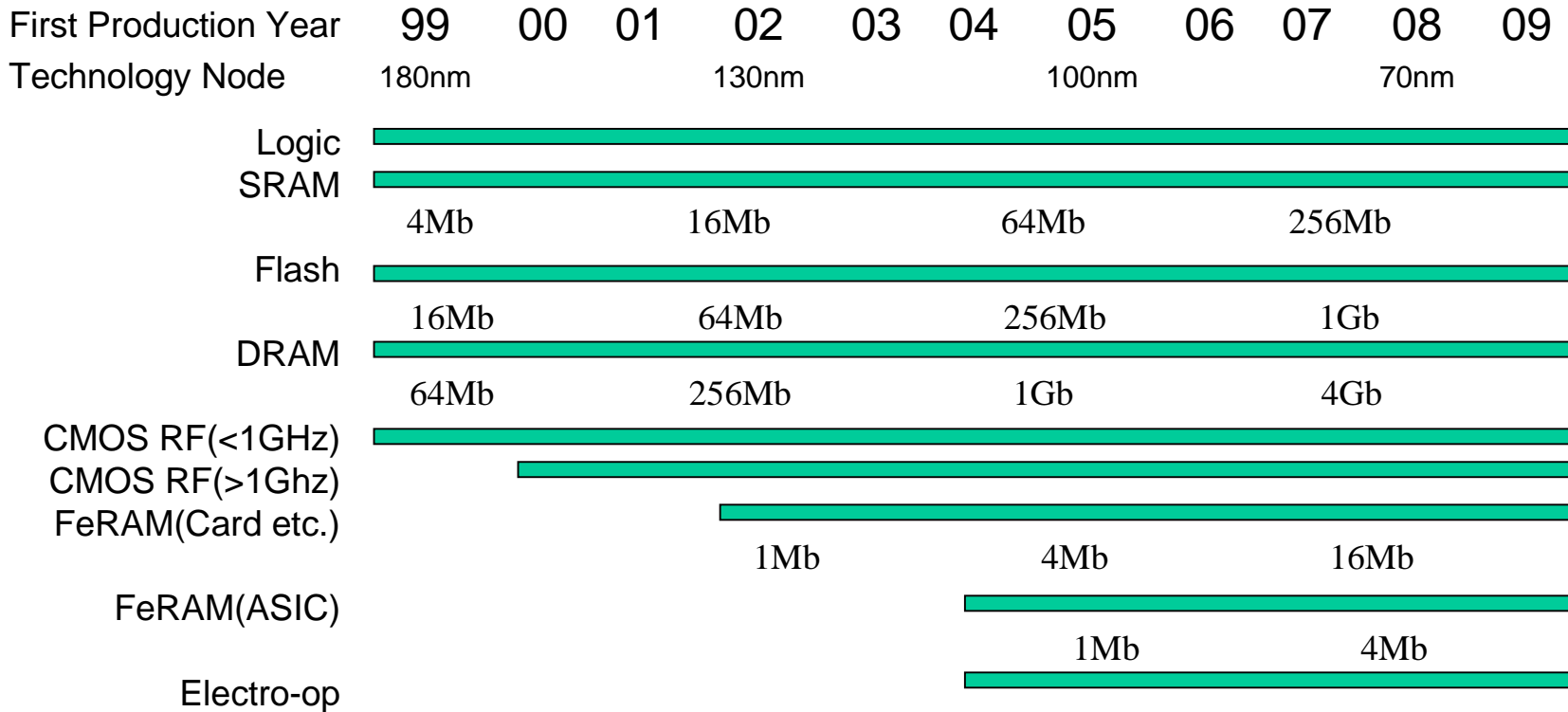
Reliability solutions need ~6 year lead

Correct by construction design for reliability tools

Advanced failure analysis



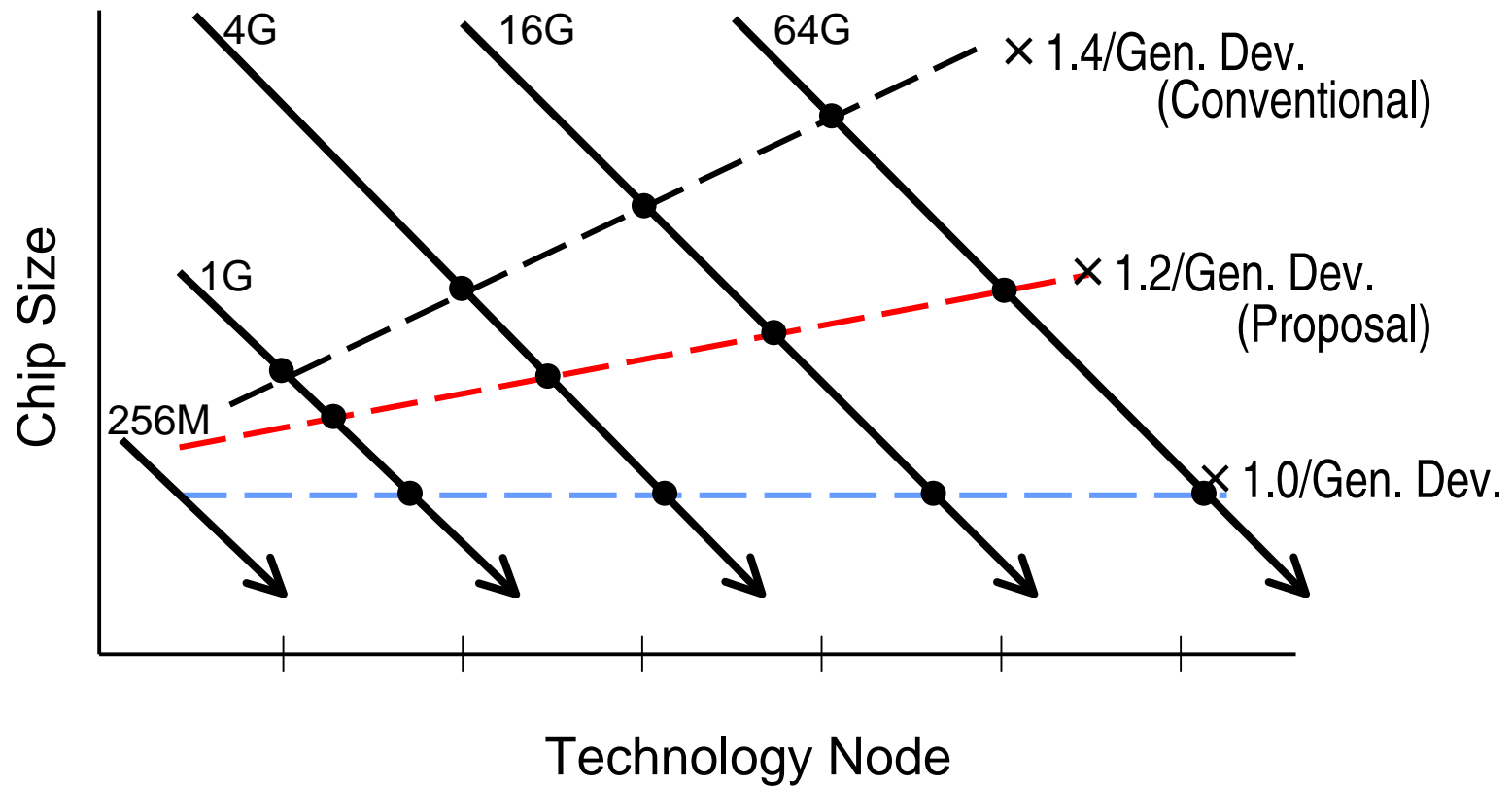
SOC Roadmap and Maximum Embedded Capacities



•SOC integration issues will put a greater demand on process innovation



DRAM Chip Size Shrink Curve



New Chip Size Model

First Production Year	99	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14
Technology Node	180			130			100			70			50			35
DRAM 1/2 Pitch(nm)	180	165	150	130	120	110	100	90	80	70	60	55	50	45	40	35
DRAM	1G		(2G)		4G		(8G)		16G		(32G)		64G		(128G)	
Introduction	400		450		480		530		580		640		700		760	
After 2 years (x 0.62mm ²)	250		270		300		330		360		400		440		470	
After 4 years (x 0.39mm ²)	160		170		190		210		230		250		270		300	
After 6 years (x 0.24mm ²)	100		105		115		130		140		150		165		180	

Summary

- **Gate stack and new material issues will limit device performance**
- **Vdd scaling is an issue for analog, RF and digital technologies**
- **New material introductions will increase reliability risks**
- **SOC integration increasing complexity of processing**

Additional materials for question & answer time

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Changes from 97 to 99

- **Accelerating scale parameters**
 - MPU gate Length, Tox(equivalent)**
 - DRAM cell size, Capacitor dielectric etc.**
- **Separating logic devices into high performance and lower power**
- **Relaxing Vdd and noise factors for analog and mixed signal devices**
- **Showing SOC that is the trend for future devices**

Chip Size Shrink Rate

•Feature size scaling : 0.7

•DRAM

cell size shrink : $(0.7)^2 \times 0.84 = 0.41/3\text{yrs.} = 0.55/2\text{yrs.}$

chip size shrink : $2 \times 0.55 = 1.1/2\text{yrs.}$

•MPU

2003~ $2.8\text{Tr}/3\text{yrs} \times (0.7)^2 \times 0.84 = 1.15/3\text{yrs.} = 1.1/2\text{yrs.}$

1999~2002 $2.0\text{Tr}/2\text{yrs} \times (0.7)^2 = 1.0/2\text{yrs.}$

(0.84 : improvement factor)

Complexity table for SOC applications

Cost of adding technology in units of mask	Logic	SRAM	Flash	DRAM	CMOS RF	FPGA	MEMS	FRAM	Chem. Sensors	Electro-Optica
Logic	0									
SRAM	1-2	0								
Flash	4	3-4	0							
DRAM	4-5	3-4	7-9	0						
CMOS RF	3-5	5-9	6-9	6-10	0					
FPGA	2	2-4	4-6	3-7	5-7	0				
MEMS	2-10	3-12	6-14	6-15	5-15	4-12	0			
FRAM	4-5	3-4	7-9	2-3	7-10	6-7	9-15	0		
Chem. Sensors	2-6	3-7	6-10	6-11	5-11	4-8	4-16	6-11	0	
Electro-Optical	5-8	6-9	9-12	9-13	8-12	7-10	7-18	9-13	7-14	0