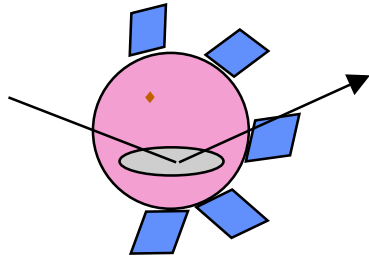
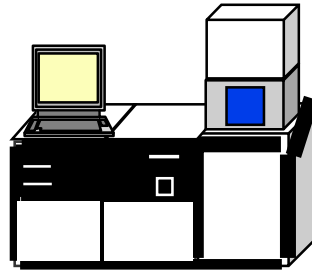


IN-SITU



IN-LINE



OFF-LINE / AT-LINE



1999 Metrology Roadmap

Europe

**Alec Reader (Philips)
Patrick Dussouillez (ST Microelectronics)**

Japan

Fumio Mizuno (Hitachi)

Taiwan

**Henry Ma (EPISIL)
George Yen (ProMOS)**

US

**Bob Scace (NIST)
Alain Diebold (SEMATECH)**

International Technology Roadmap for Semiconductors

Tokyo, Japan; November 1999



Outline

- **Changes from 1997**
- **Critical Challenges**
- **Lithography Metrology**
- **Front End Processes**
- **Interconnect Metrology**
- **Integrated Metrology**
- **Risks**



Changes from 1997 NTRS

- Mask Metrology Expanded
- New needs from 157 nm Lithography
- Sensors now a part of Integrated
Metrology

Difficult Challenges > 100 nm / Before 2005

- Metrology integration for in-situ and in-line metrology tools
- Particles, oxygen, and metallics detection at levels of interest for starting materials and reduced edge exclusion for metrology tools
- Measurement of the frequency-dependent dielectric constant of low k interconnect materials at 5x to 10x base frequency.
- Control of high-aspect ratio technologies such as Damascene challenges all metrology methods.
- Measurement of complex material stacks

Additional Difficult Challenges < 100 nm / Beyond 2005

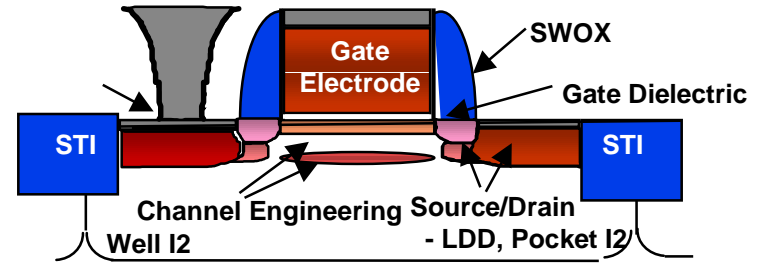
- Microscopy for critical dimension measurement, overlay, defect detection, and analysis
- Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials
- Statistical limits of sub-70 nm process control
- 3-D dopant profiling
- Production worthy, physical inline metrology for transistor processes that provides SPC required to achieve consistent electrical properties

Domestic vs International Points of View

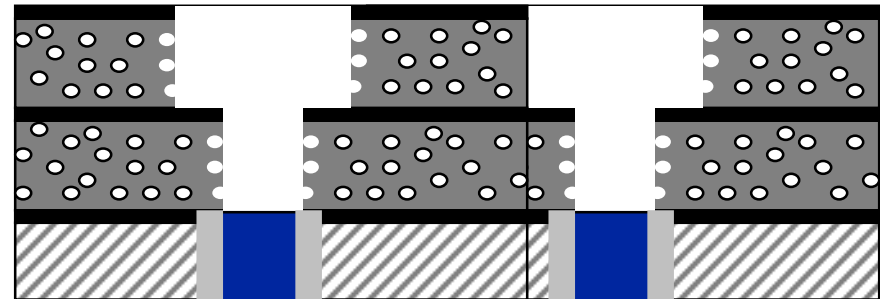
- Precision vs Accuracy
- Precision US Centric
- Accuracy and Precision Global Centric

Lithography Metrology

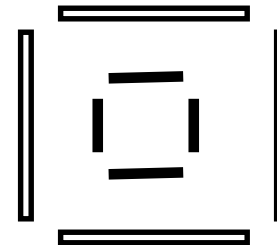
Gate Length Control



Damascene Line Width

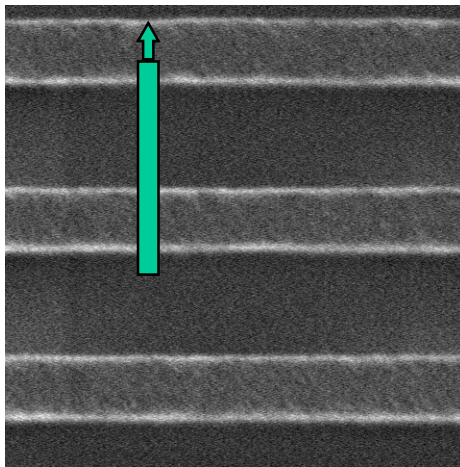


Overlay Control



Lithography Metrology

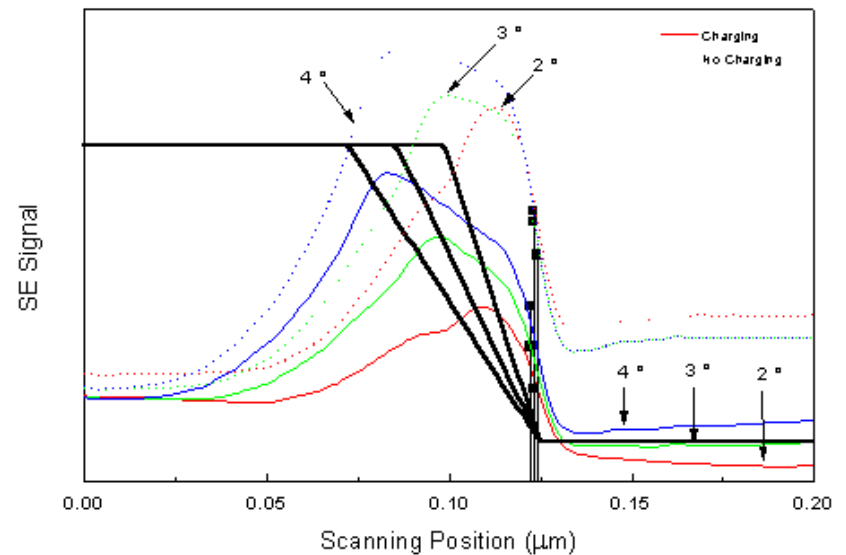
Improve CD-SEM thru 100 nm node



top down
CD-SEM

KRISS

Isolated (Sidewall Angle)



Signal → CD Value

NEED: Determine CD from Fundamental Model

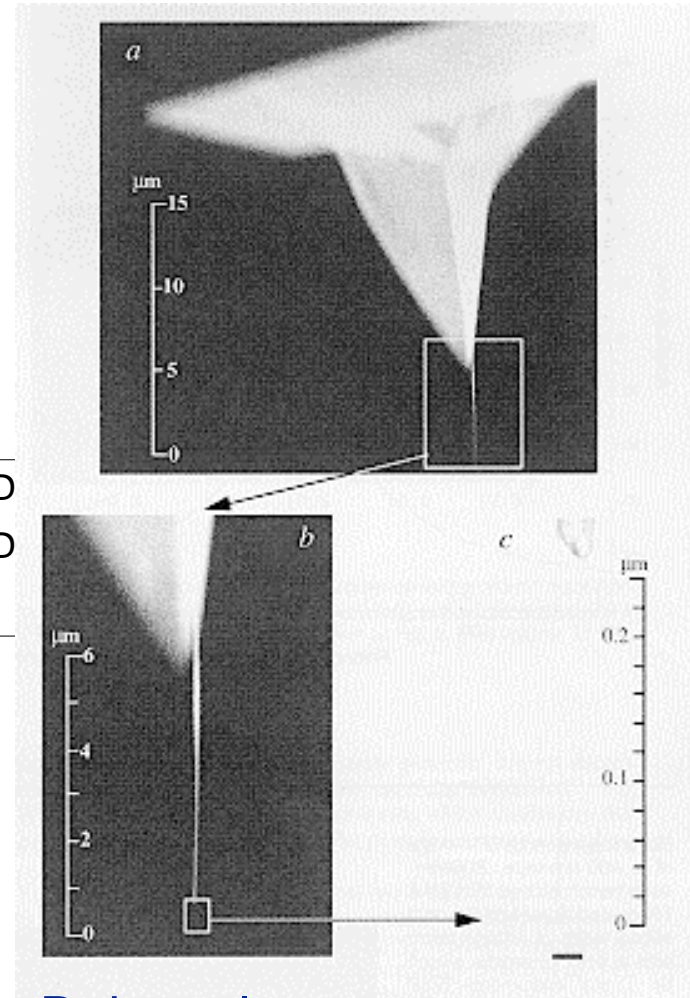
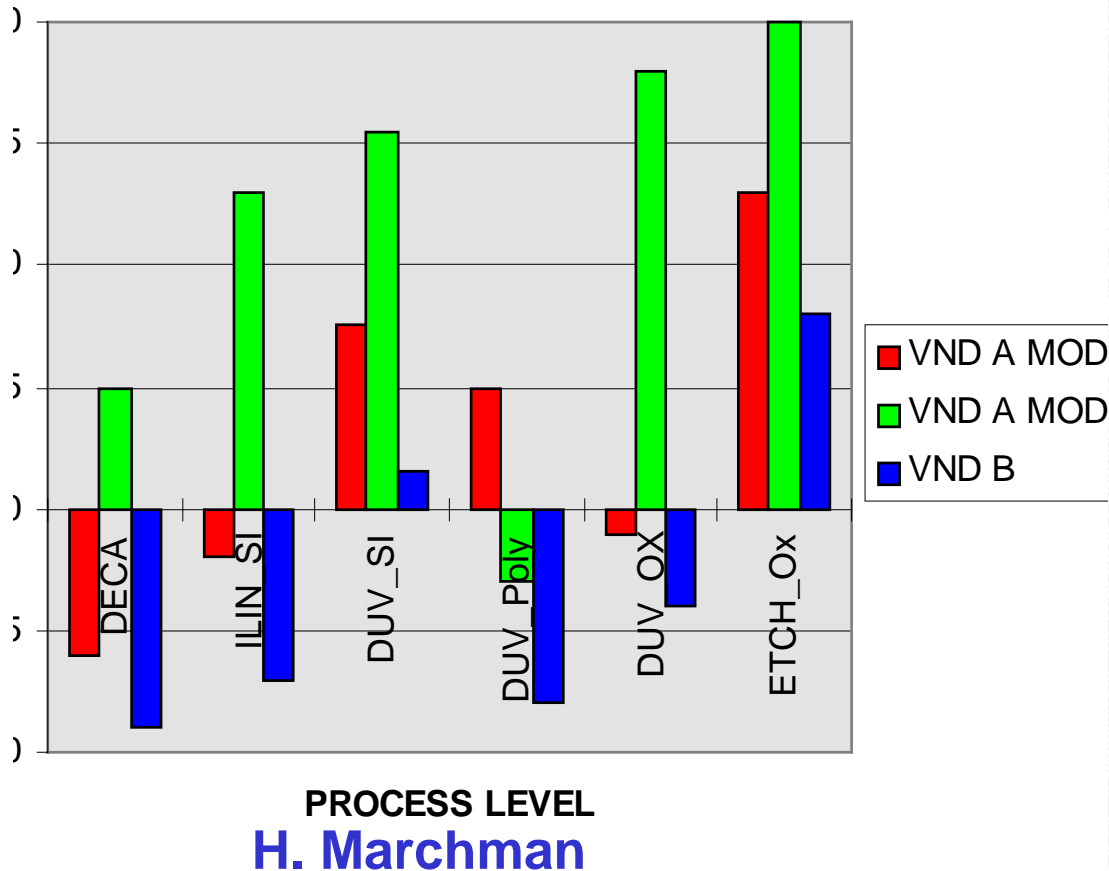
International Technology Roadmap for Semiconductors

Tokyo, Japan; November 1999



Process Level Dependence of CD SEM

Calibration requires New Probe tips for CD-AFM



Dai, et al.,
Nature **384**, 147 (1996)

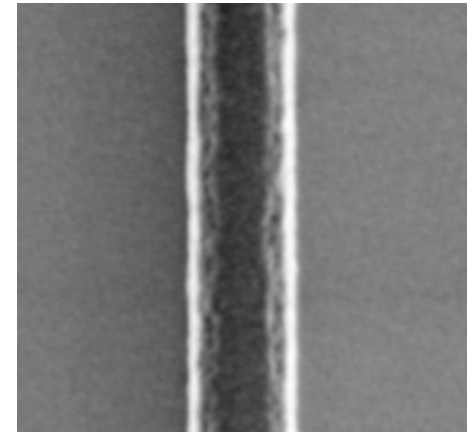
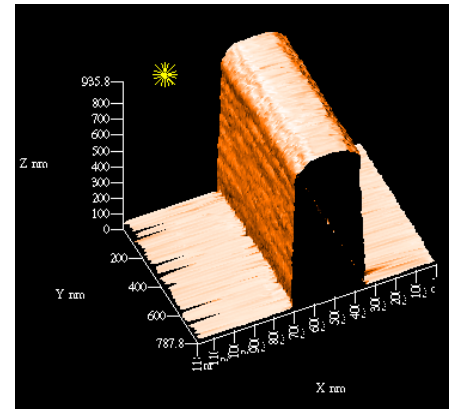
Microscopy

Issues:

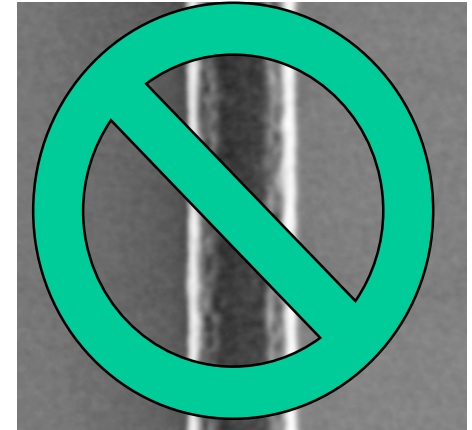
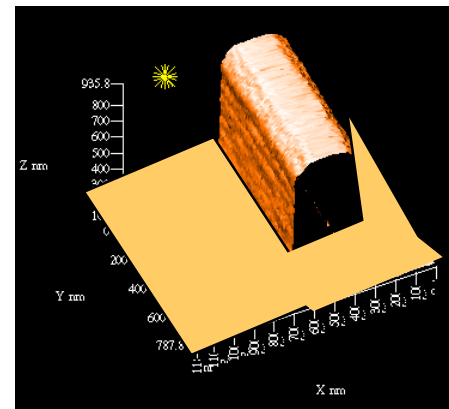
CD and Detection require new microscopy

- SEM with resolution required for sub 100 nm has **poor Depth of Focus**
- 3D Information Required
- Improved throughput required

SEM



Today : Depth of focus > 1 micron



With Future Resolution:
Depth of focus << 1 micron

International Technology Roadmap for Semiconductors

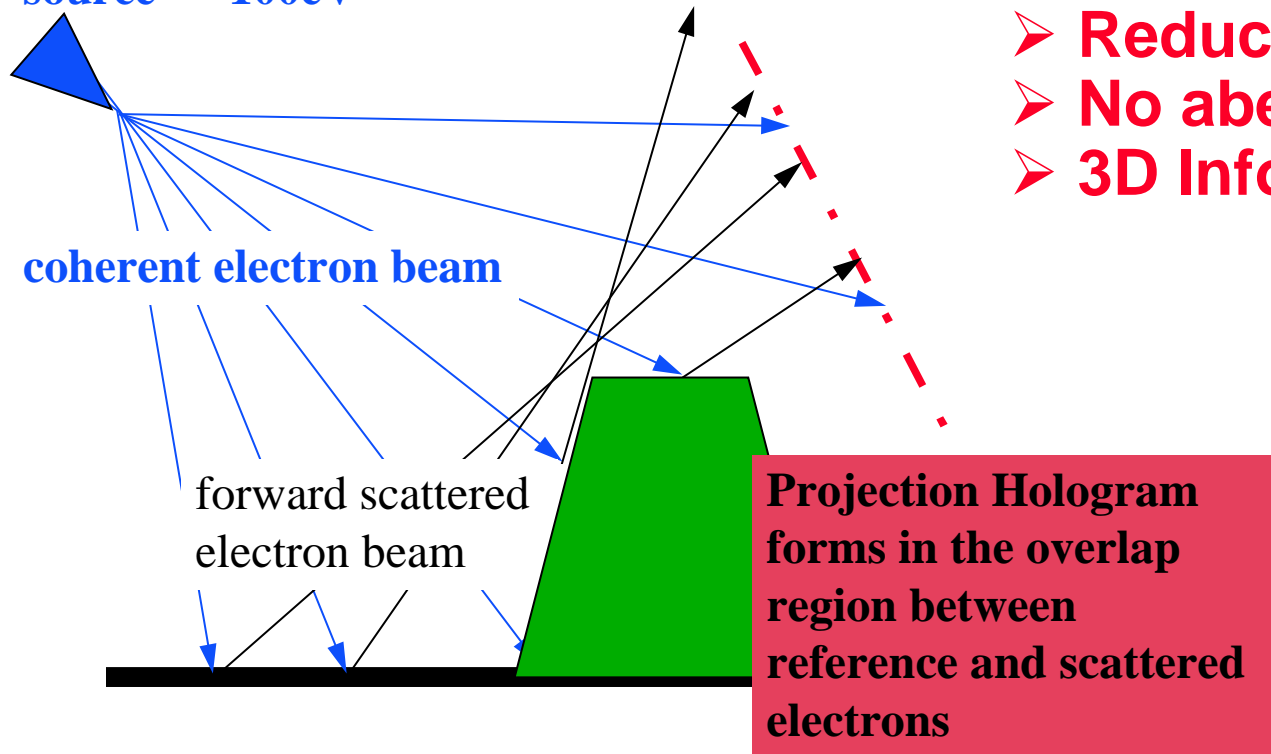
Tokyo, Japan; November 1999



Microscopy and Lithography Metrology

Long Term Research and Development

Nanotip Field Emission
source ~ 100eV



Electron Holography

- Low damage
- Reduce Charging
- No aberration/diffraction
- 3D Information

David Joy, Univ. of TN

International Technology Roadmap for Semiconductors

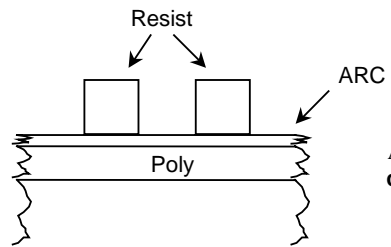
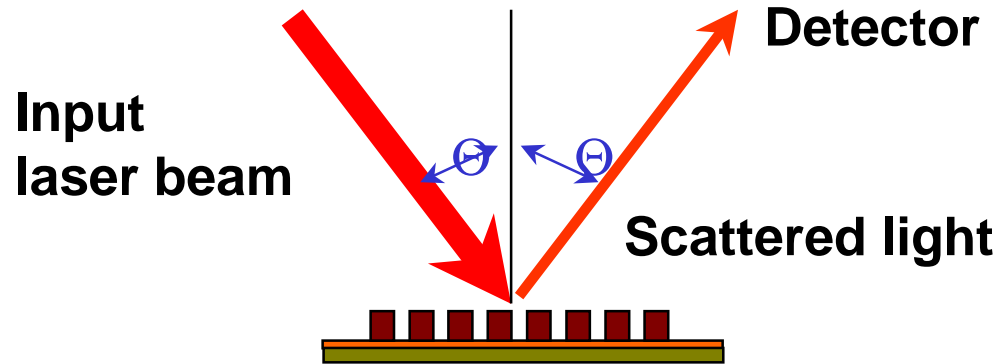
Tokyo, Japan; November 1999



CD-Scatterometry : Another Potential Solution

2- Θ scatterometer: CDS-2

- Developed as a Sensor at Sandia and UNM
- Available as an in-line system



Parameters

Variables :

- CD = $270 \pm 60\text{nm}$
- Resist thickness = $725 \pm 25\text{nm}$
- Poly thickness = $2500 \pm 350\text{nm}$
- ARC thickness = $80 \pm 10\text{nm}$
- Sidewall angle = $86 \pm 2^\circ$

Fixed :

- Pitch
- Resist, Poly and ARC optical properties

All parameter combinations

Signature Generator Software

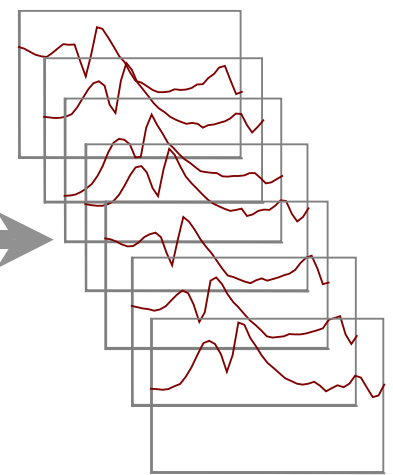
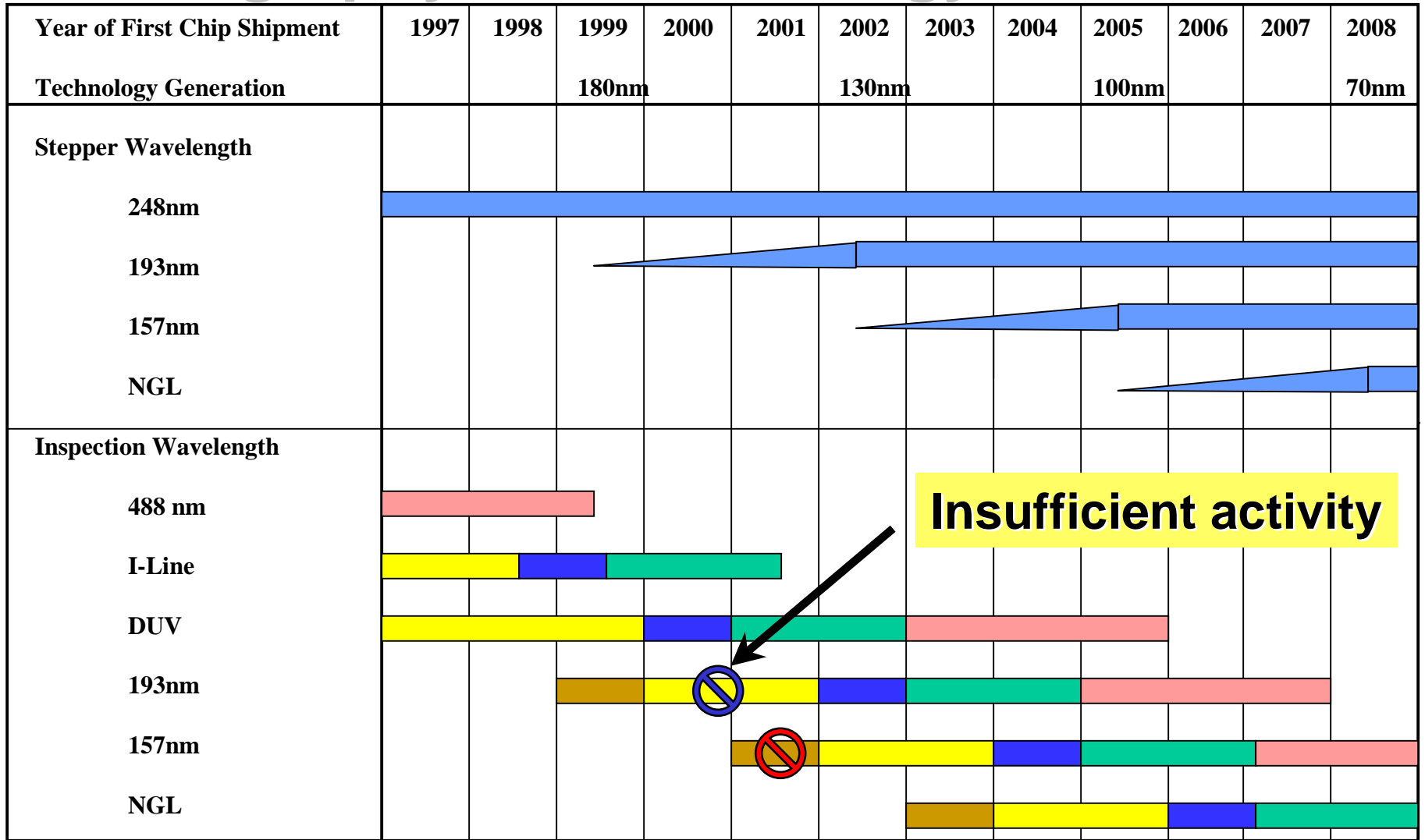


Figure courtesy
BIO-RAD



Lithography Mask Metrology



Wally Carpenter

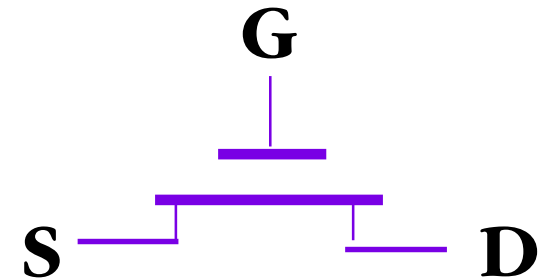
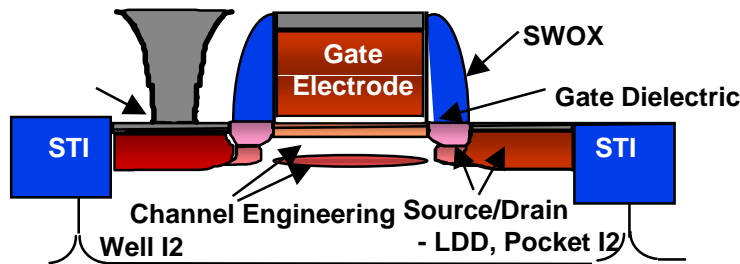
International Technology Roadmap for Semiconductors



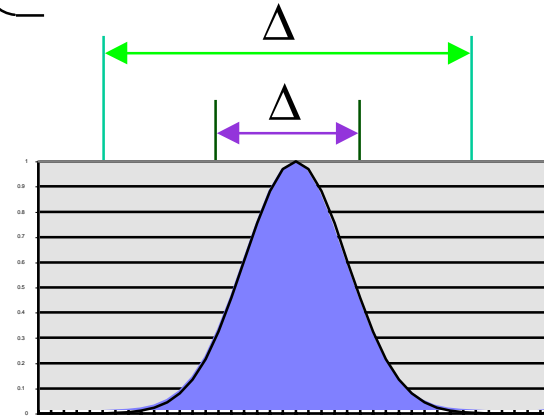
Tokyo, Japan; November 1999

Front End Processes

(Transistor & Capacitor Process) Metrology



Δt_{oxide} , ΔL_g ,
 $\Delta \text{dose/junction}$



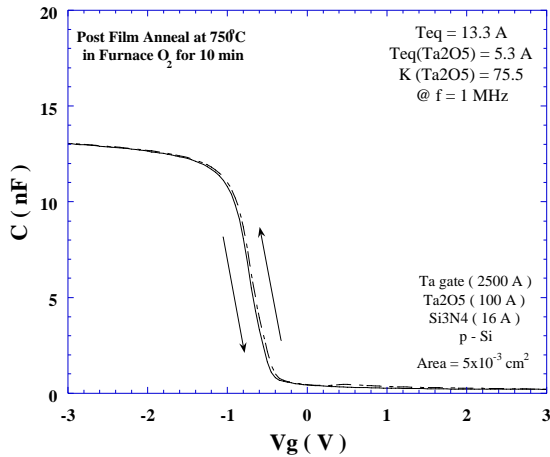
ΔL_{eff} , ΔV_t , ΔI_{off}

Electrical Measurement requires fabrication of a transistor.
Will physical metrology be able to adequately

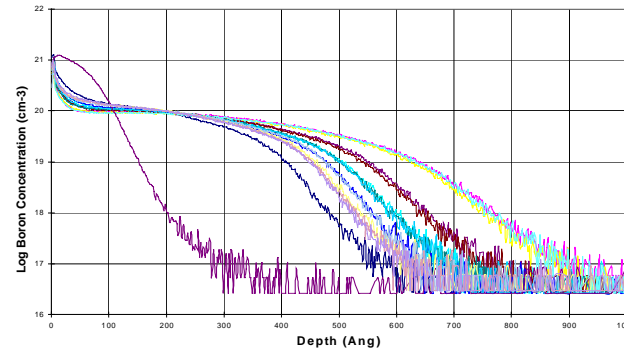
control critical processes at 100 nm and

Transistor Process Metrology Challenges

New Materials & Ultra Shallow Junctions



SIMS Profile
Boron Concentration vs Junction Depth Xj

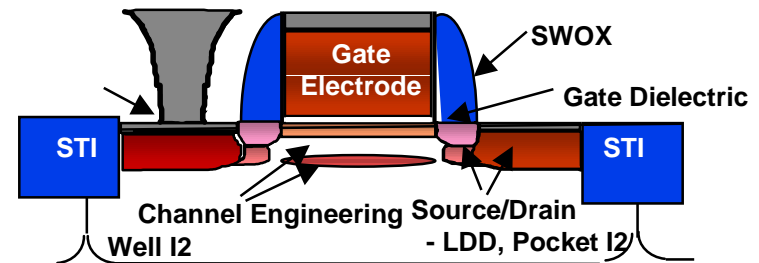


Gate metal / Ta₂O₅ / Oxynitride Dielectric

Ta₂O₅ Gate Dielectric

Oxynitride Interface

20 Å



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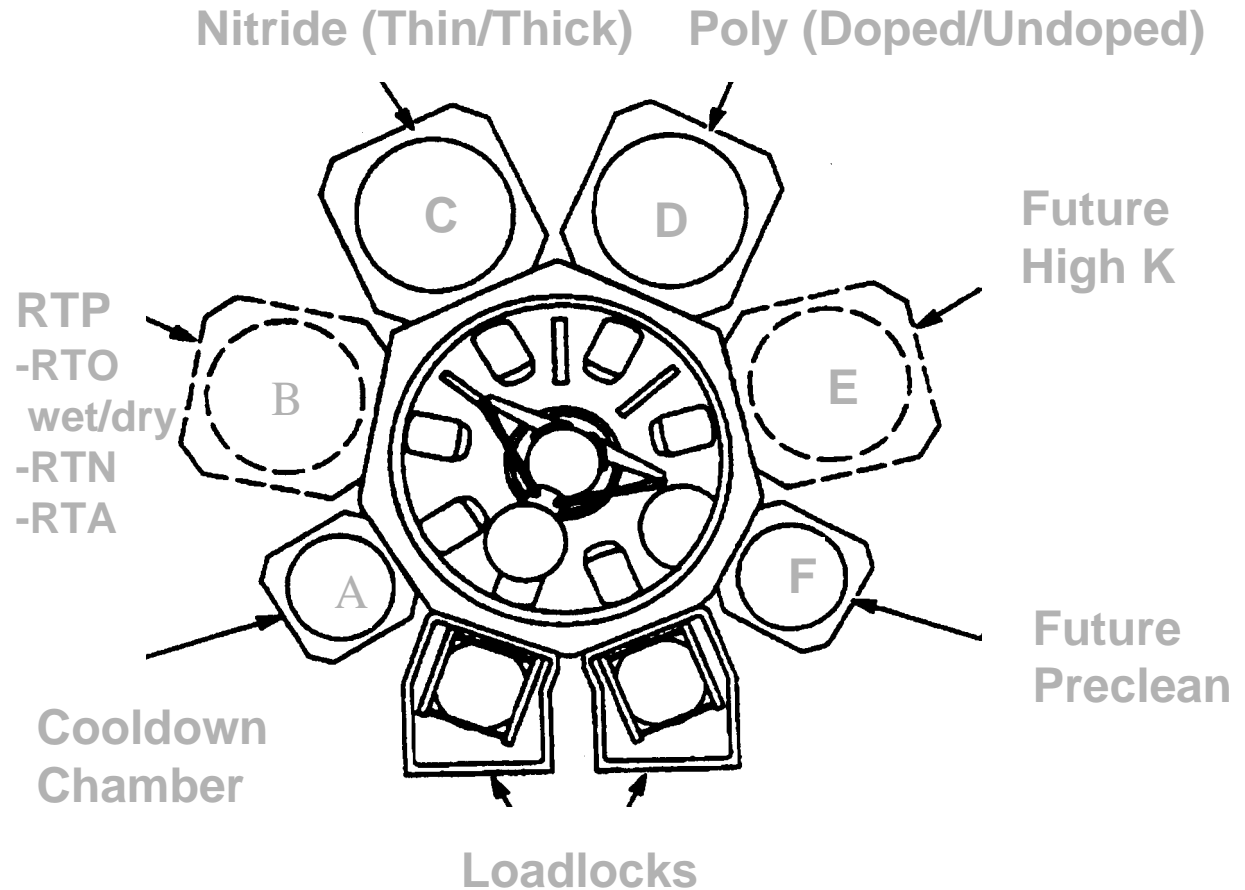


Front End Process Metrology

In-Situ Needs vs Integrated Metrology Trend

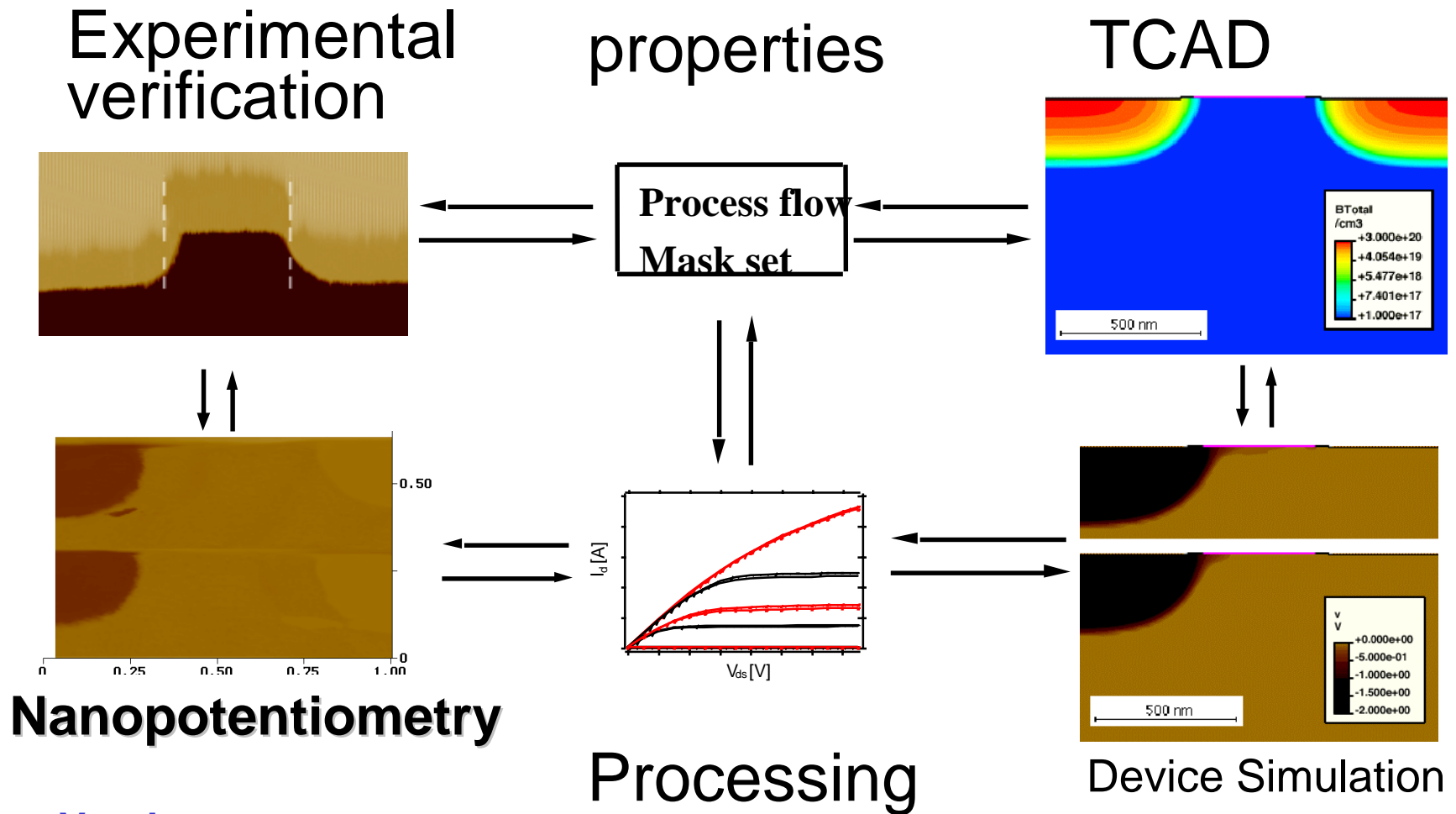
**Clustered
gate dielectric
& electrode**

**e.g., Metal
Gate forces in-
situ metrology
for dielectric**



2D Dopant Profiling

Issue : Spatial Resolution



imec - Vandervorst

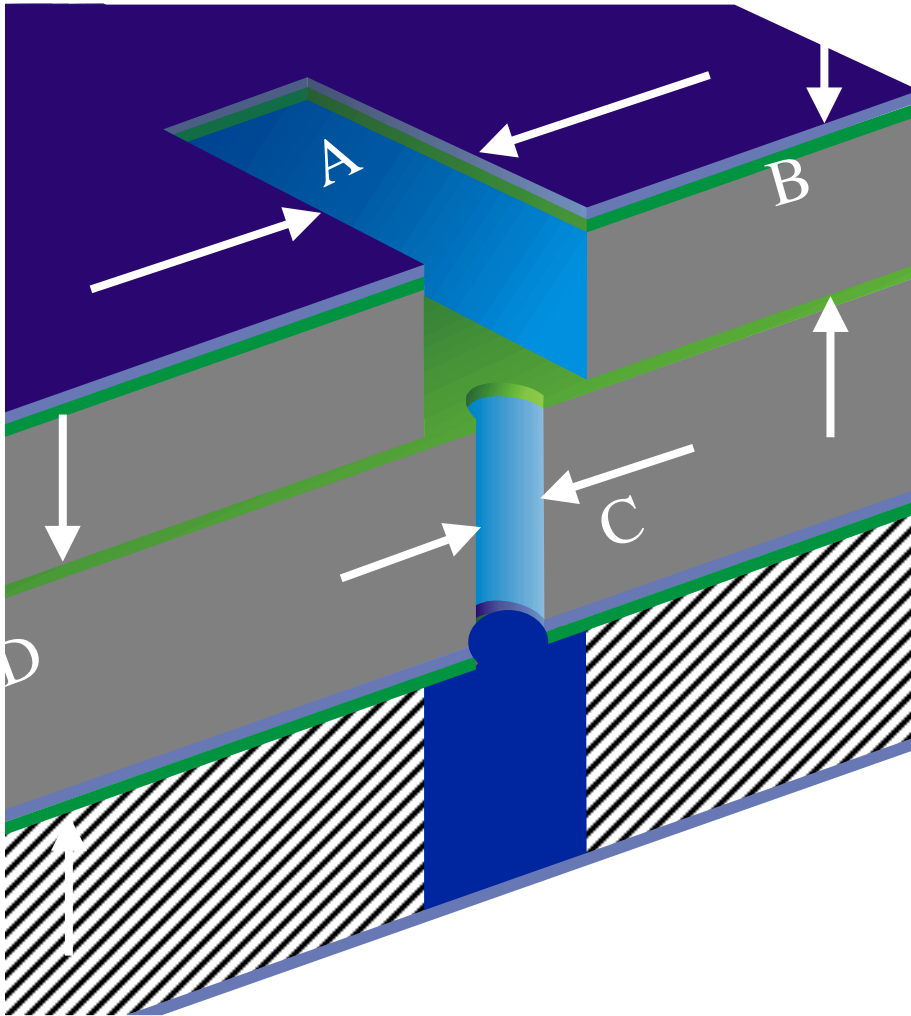
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Interconnect Metrology

New Materials and Processes



Copper/barrier Film Thickness

100 micron diameter size test areas
by acoustic

Low k Dielectrics

High frequency dielectric testing
needs development for > 40 GHz

Need optical models for porous
materials

Developing Physical Properties and
Delamination testing

SENSOR based Integrated Metrology

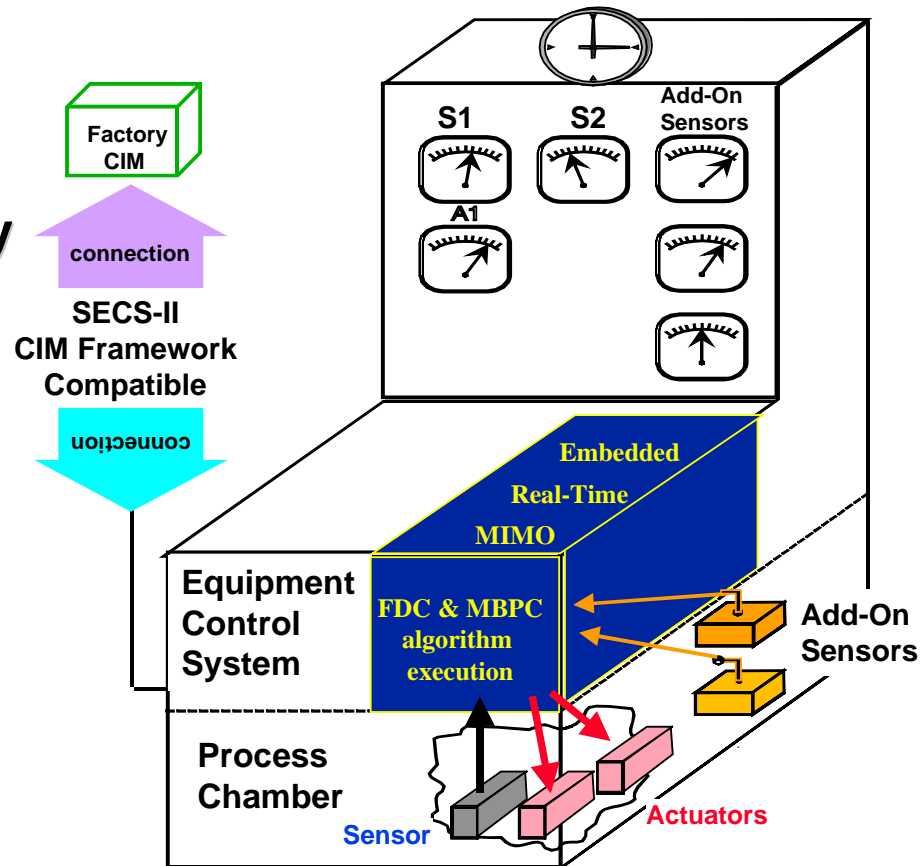
Comments on :

Advanced Process Control - Advanced Equipment Control

- **AEC/APC GOAL :**
model based predictive control
based on process and metrology
models using in-situ and in-line
measurements

➤ **Momentum ?**

➤ **Now suppliers advocate
Integrated Metrology**



RISKS

- **Many Measurements have precision requirements that will be difficult to meet. This leads to a Lack of Metrology Tools for accelerated Technology Cycle**
- **Important New Approaches need additional funding for long term R+D (ex. - Electron Holography, arrayed AFM/SEM)**
- **Business Model for Metrology does not fit Industry needs**
- **Lack of methodology for Statistically Limited Processes and appropriate metrology**
- **Shrinking scribe lines limit test areas needed for adequate measurement precision**

Background

International Technology Roadmap for Semiconductors
Tokyo, Japan; November 1999



In-line Metrology usage

400 + step Process Flow

steps

~25 Overlay

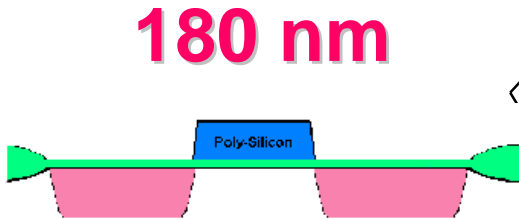
~20 CD

<20 Defect/Particle

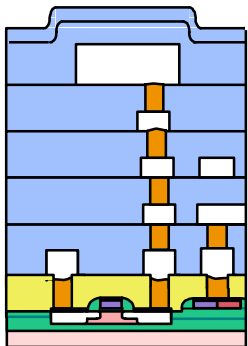
~ 6 { Poly Si Control
ILD Thickness
Contact Etch
ILD Etch Control
Metal Thickness

~ 4 Implant Dose

1 Gate Ox Thickness



6 metal levels

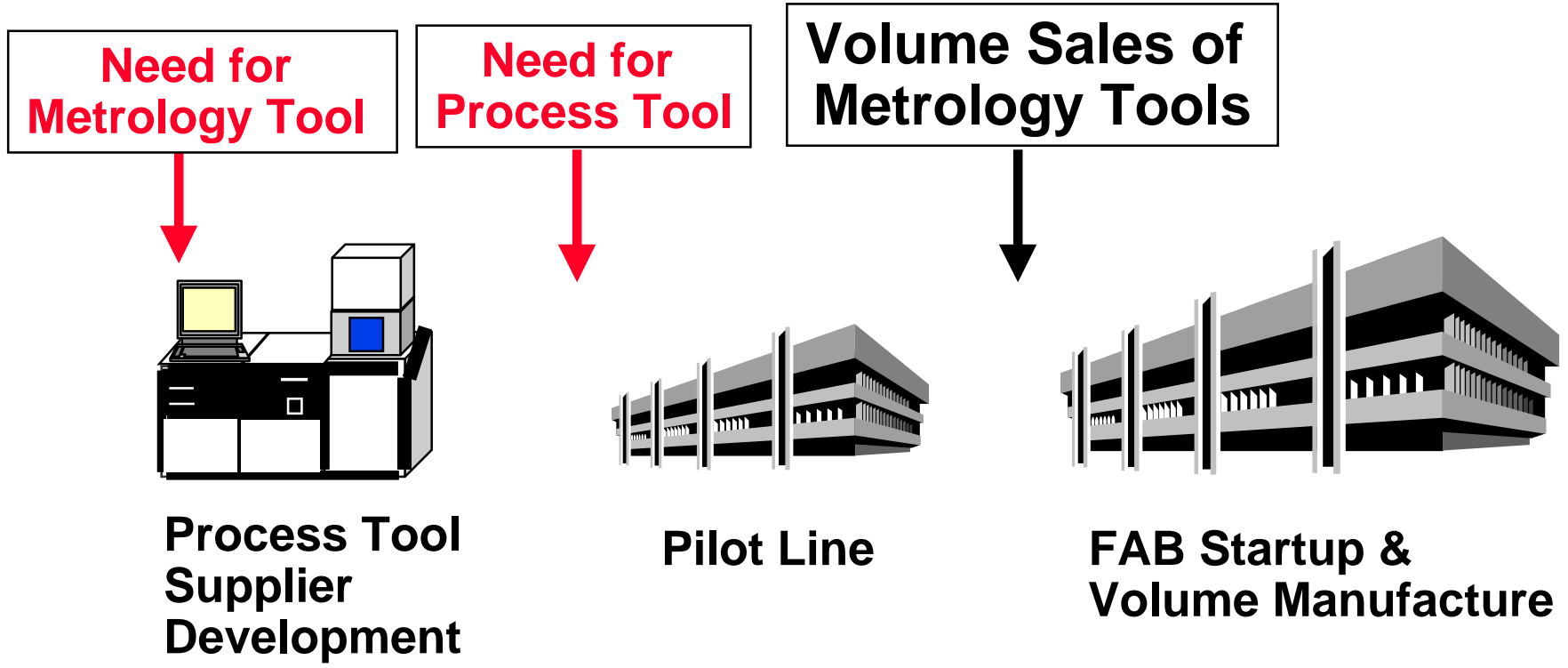


Messages from overview

- Infrastructure
- Requirements have too much RED
- Challenge Associated with Precision Requirements
- Microscopy Development
- Interfacial Measurements

Metrology Timing vs Infrastructure Capabilities

Gap in long term R&D Spending + Development Funding Model



Typical Potential Solutions Time Line for Process Tool



Too Many Metrology Technology Requirements are R

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Wafer gate CD control*	4.0	3.0	2.0
Wafer dense line CD control*	7.0	5.0	3.5
Wafer contact CD control*	8.0	5.5	4.0
Wafer CD metrology tool precision* P/T=.2 for isolated lines**	0.8	0.6	0.4
Wafer CD metrology tool precision* P/T=.2 for dense lines**	1.4	1.0	0.7
Wafer CD metrology tool precision* P/T=.2 for contacts**	1.6	1.1	0.8
Maximum CD measurement bias (%)	10	10	10
Mask CD control isolated lines*	7	5	3.3
Mask CD control dense lines*	11	8	5.6
Mask contact area control Normalized to ρ of area*	12	9	6.4
Mask CD metrology tool precision* P/T=.2 for isolated lines**	1.4	1.0	0.7
Mask CD metrology tool precision* P/T=.2 for dense lines**	2.2	1.6	1.1
Mask area metrology tool precision for contact normalized to ρ of area- ρ of target for P/T=.2	1.6	1.8	1.3
Wafer overlay control (nm)	25	20	15
Wafer overlay output metrology precision (nm, 3 sigma)* P/T=.1	2.5	2.0	1.5
Final mask image placement	15	12	9
Mask image placement metrology precision P/T=.1	1.5	1.2	0.9
Mask phase (in degrees)	1	NA	NA
Phase metrology precision P/T=.2 (in degrees)	0.2	NA	NA
Variation in attenuated mask film transmission % of deviation from nominal (%)	4	NA	NA
Transmission metrology precision % of nominal attenuated PSM transmission P/T=.2 (%)	0.8	NA	NA

* All precision values are 3 sigma in nm and include metrology tool matching.

** Measurement tool performance needs to be independent of line shape, line materials, and density of lines.

Intern Solutions Exist
Solutions



Solutions Being Pursued



No Known



Tokyo, Japan, November 1999

Examples of Precision Requirements

Year of First Product Shipment Technology Generation	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2003 100 nm	Driver
DRAM 1/2 Pitch	180	165	150	130	120	110	100	D _{1/2}
Logic Isolated Lines	140	120	100	85	80	70	65	M Gate

Microscopy and Lithography

Microscopy resolution (nm) for P/T=0.1	1.4	1.2	1.0	0.85	0.8	0.7	0.65	MPU
Wafer Gate CD Control*	13	12	10	8.5	8	7	6.3	MPU
Wafer CD Tool Precision* P/T=.2 Isolated Lines**	2.6	2.4	2.0	1.8	1.6	1.4	1.3	MPU
Mask Area Metrology Tool Precision P/T=.2	4.8	4.2	3.4	2.8	2.6	2.4	2.2	MPU

Front End Processes

Logic Dielectric Thick Precision 1 σ (nm) ^B	0.0075	0.0075	0.006	0.006	0.006	0.005	0.004	MPU Gate
2D Dopant Profile Spatial Resolution (nm)	3	3	3	2	2	2	1.5	MPU Gate

Interconnect

Barrier layer Thick (nm)	17	16	14	13	12	11	10	MPU
process range ($\pm 3\sigma$)	10%	10%	10%	10%	10%	10%	10%	
Precision 1 σ (nm)	<0.06	0.05	<0.05	0.04	0.04	<0.04	0.03	

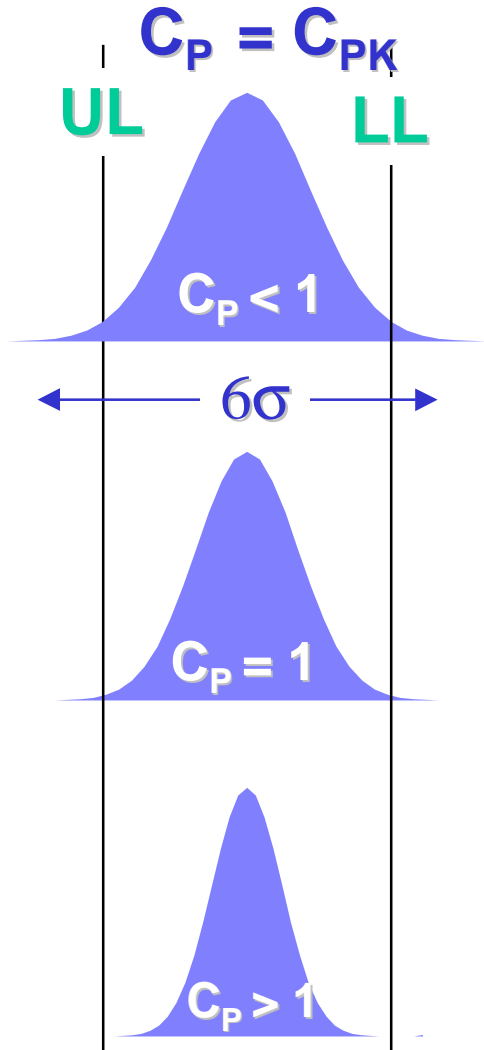
International Technology Roadmap for Semiconductors

Tokyo, Japan; November 1999



Effect of P/T on Process $C_p = (UL-LL) / 6 \sigma$

If Distribution is Centered



EFFECT OF MEASUREMENT PRECISION (P/T RATIO) ON C_p AS MEASURED

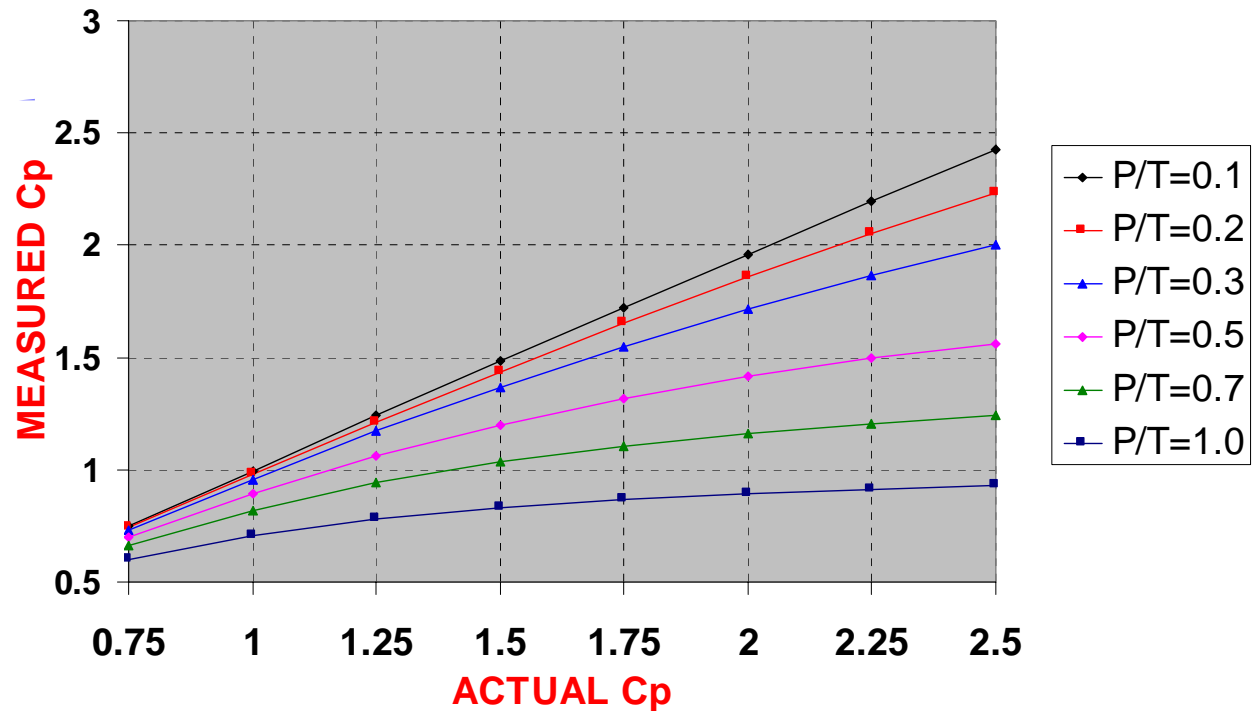


Chart from Jerry Schlesinger, TI

International Technology Roadmap for Semiconductors

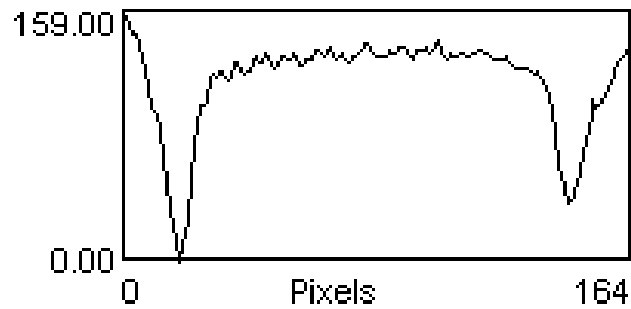
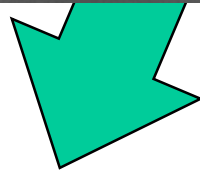
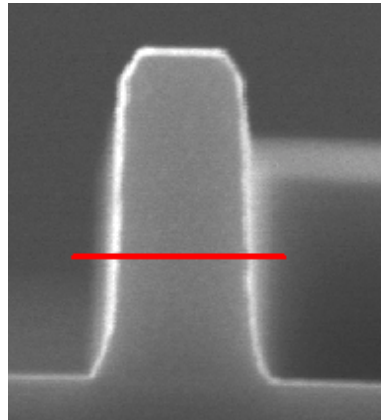


Tokyo, Japan; November 1999

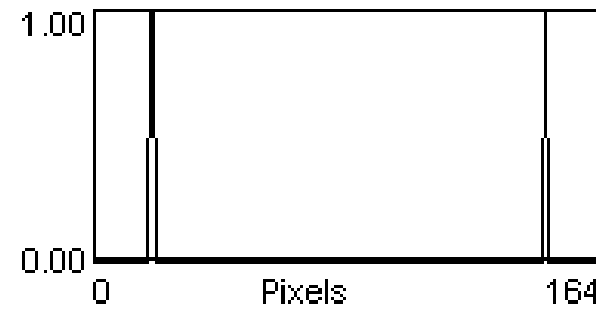
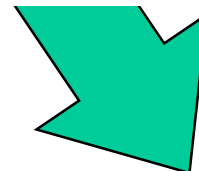
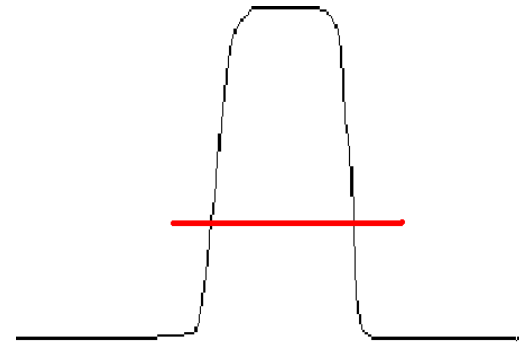
Calibration of CD-SEM

Intensity Profiles From CD-AFM / SEM

SEM



CD-AFM
Stylus
Nano
Profilometer



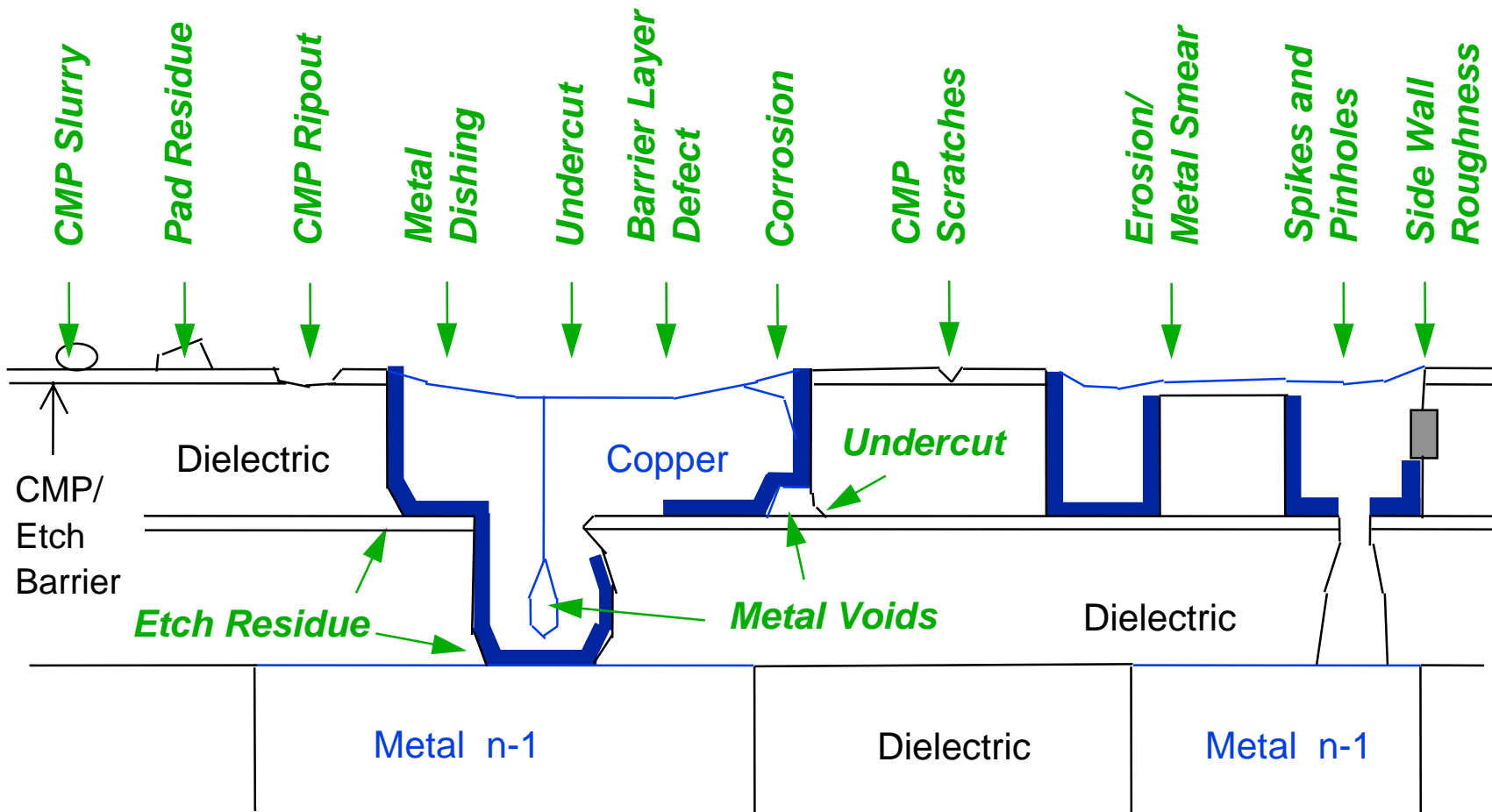
Thanks to Joe Griffith

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Systematic Failure Modes in Dual Damascene Processes



David Jensen - AMD/SEMATECH

International Technology Roadmap for Semiconductors

Tokyo, Japan; November 1999



Depth of Focus Requirements for Litho

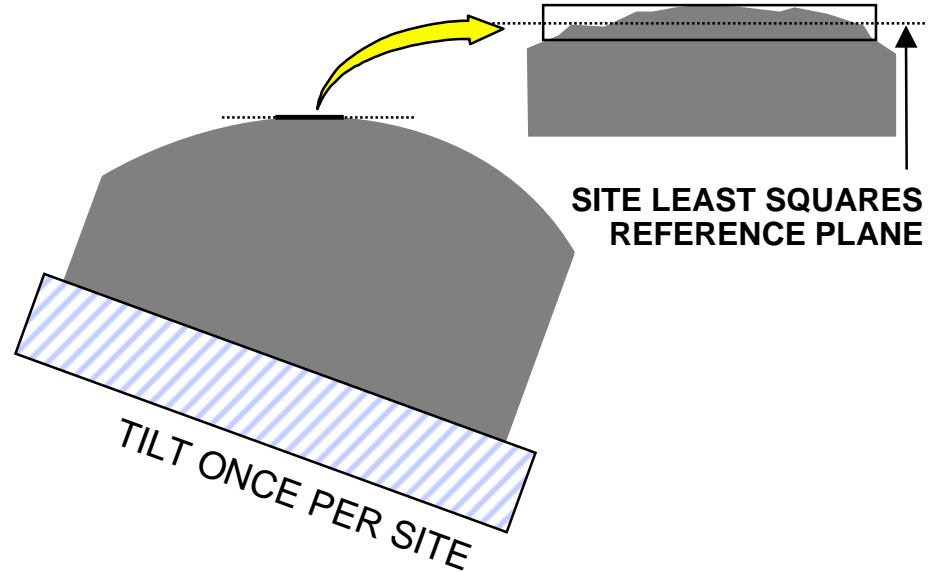
CMP Metrology tool should measure what litho tool “sees”

Full Field Steppers

SEMI STD

Site Frontside
least-sQuared
site reference

Range = SFQR
Deviation = SFQD

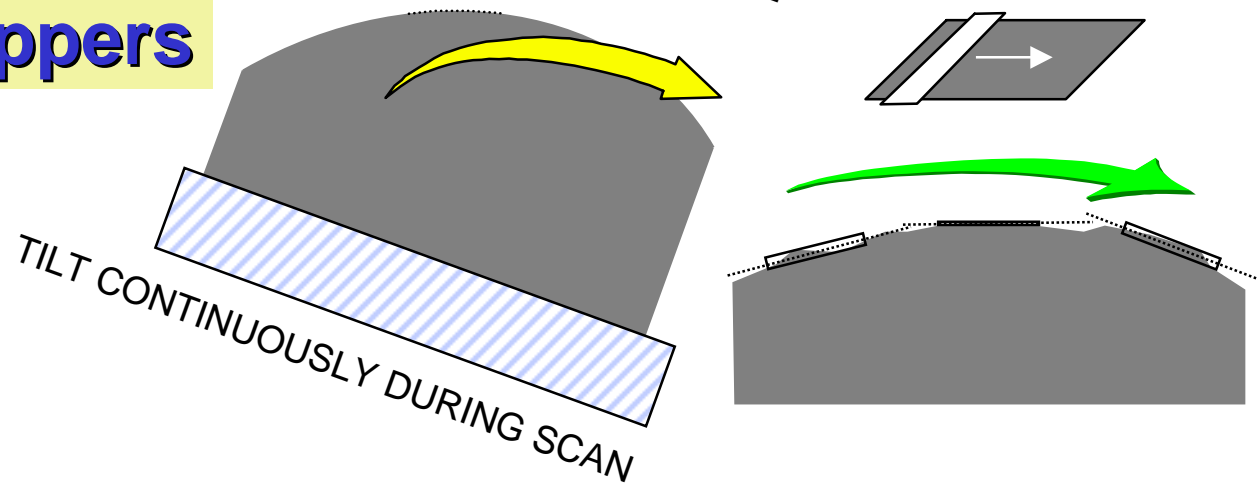


Scanning Steppers

SEMI STD

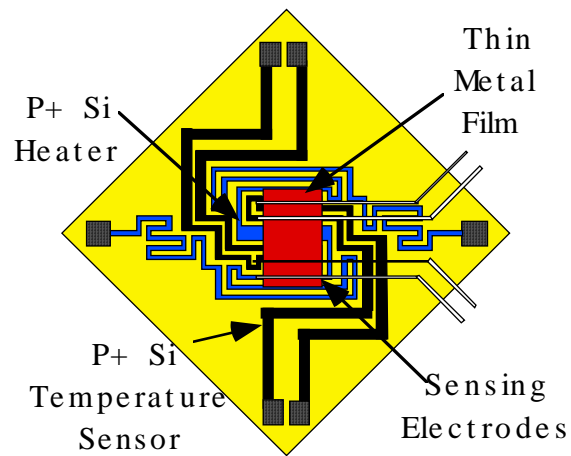
Site Frontside
Scanning*
site reference

Range = SFSR
Deviation = SFSD

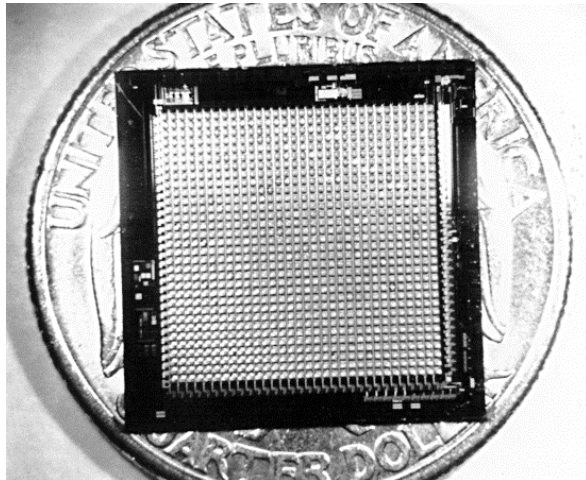


SENSOR based Integrated Metrology

MEMS : Sensor Technology of the Future



A MONOLITHIC DETECTOR FOR PROCESS GAS PURITY



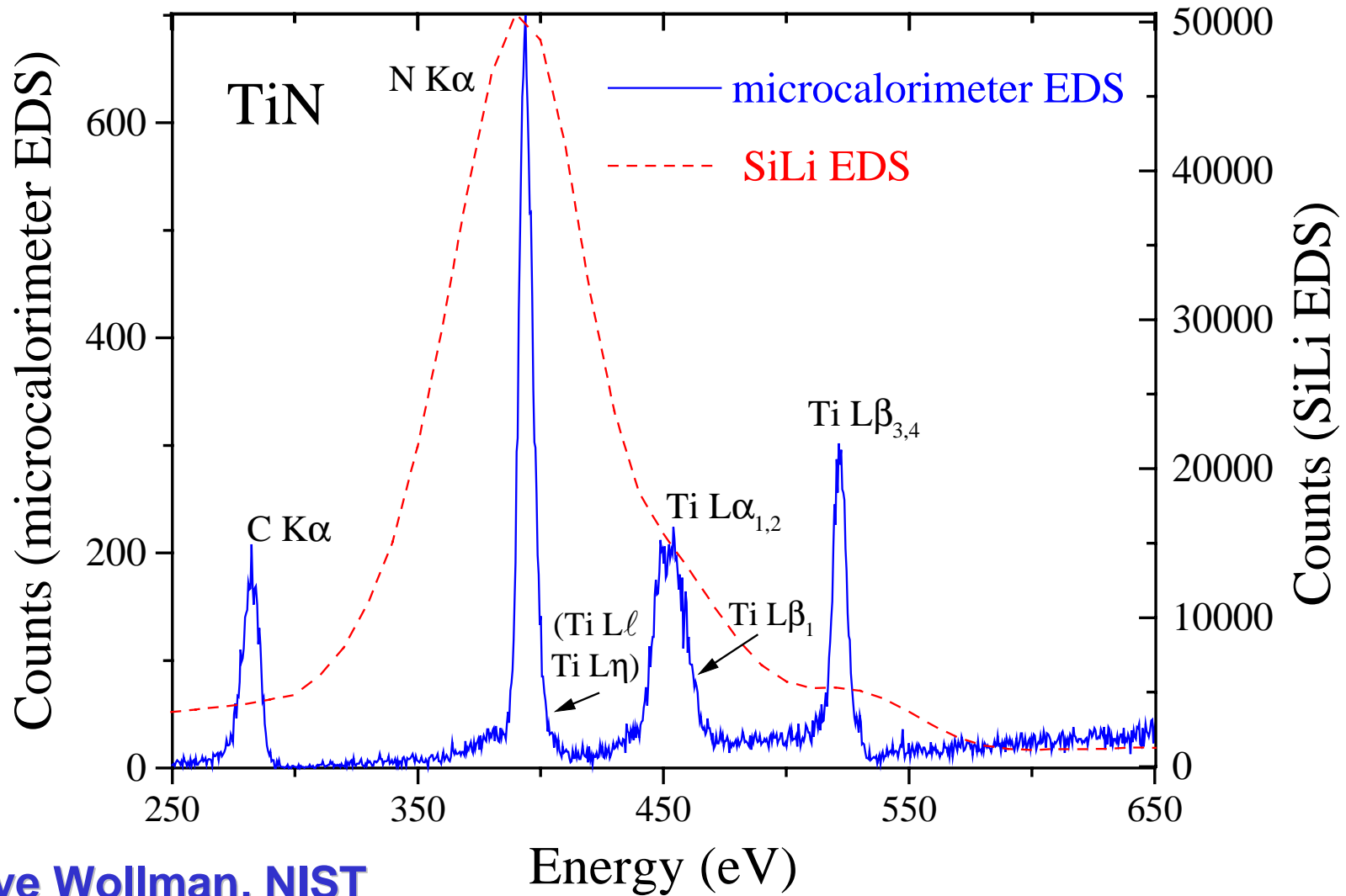
Infrared Imager for RTP

GOAL:

measure temp & uniformity

$\pm 1^{\circ} \text{C}$ to 1000°C

Microcalorimeter EDS vs EDS



Dave Wollman, NIST

International Technology Roadmap for Semiconductors

Tokyo, Japan; November 1999



Accelerated MPU Gate impacts all GAPS

Key Drivers \Leftrightarrow GAPS

Shrinking Dimensions	\Leftrightarrow	< 100 nm Microscopy for CD, Detection
	\Leftrightarrow	High Aspect Ratio Capability
	\Leftrightarrow	Metrology with adequate precision and correlation w/electrical tests
	\Leftrightarrow	Process Control for Processes at Statistical Limits
	\Leftrightarrow	3-D Dopant Profiling

New Materials in Transistor, Capacitor, and Interconnect	\Leftrightarrow	Measure High Frequency Dielectric Constant
	\Leftrightarrow	Measurements and standards for new materials stacks