

**Lithography ITWG Report
for
ITRS '99 Japan Conference**

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Lithography ITWG Report

Outline

- ◆ Key Changes from 1997
- ◆ Format
- ◆ Key Issues / Concerns
- ◆ Difficult Challenges
- ◆ Lithography Requirements
- ◆ Potential Solutions
- ◆ Summary

1999 ITRS Roadmap Update

Key Changes from 1997

- ◆ International Roadmap process successfully implemented. Agreement reached on key elements:
 - ⇒ Timing pulled in one year and remains on 3 year cycle
 - ⇒ Chip size growth rate cut from ~14% per year to ~5% per year
- ◆ Optical lithography extends domain of applications
 - ⇒ 248nm + PSM added at 130nm node
 - ⇒ 157nm added at 100nm and 70nm nodes
- ◆ NGL options pushed out to 100nm node and below
- ◆ Increased emphasis placed on masks: addressed mask error function, enhanced PSM requirements and dropped requirement for 230mm mask
- ◆ Changes supported by all five regions (Europe, Japan, Korea, Taiwan, USA) and to be published by year end 1999

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Format

- ◆ Revised “Lithography Requirements” table based on input of ITWG meeting 12/7/98 in Colorado.
 - ⇒ Focus on DRAM, MPU and ASIC unique needs.
 - ⇒ Include new chip sizes.
- ◆ Revised “Mask Requirements” table to differentiate Optical needs from NGL.
 - ⇒ Address mask error function (MEF) for advanced optical low k_1 applications.
 - ⇒ Enlarge PSM requirements.

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Key Issues - Roadmap Timing

- ◆ Timing has been one of biggest concerns for the Lithography TWGS.
- ◆ Discussed extensively among Japan, USA, Korea, Europe and Taiwan. Industry surveys conducted in Japan and USA.
- ◆ Tentative agreement reached in Munich, April 13th, with IRC and finalized at July 7th Workshop in Santa Clara:

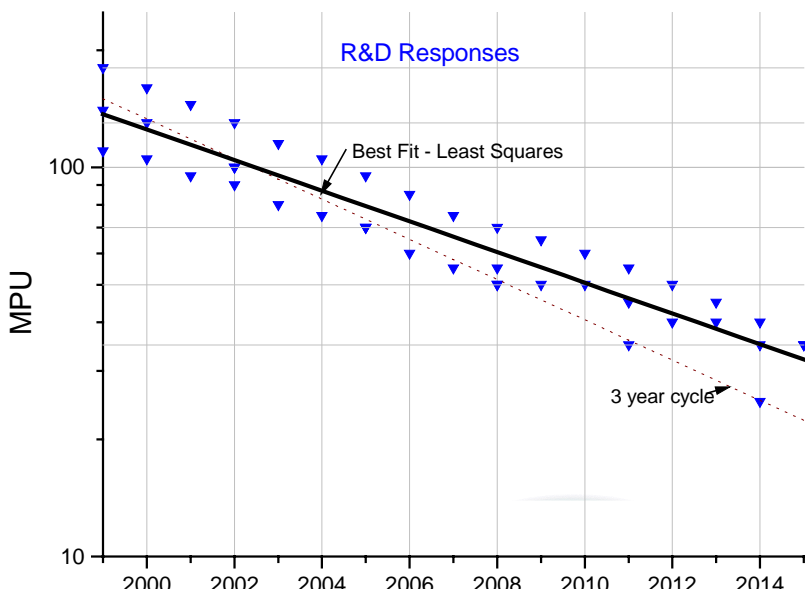
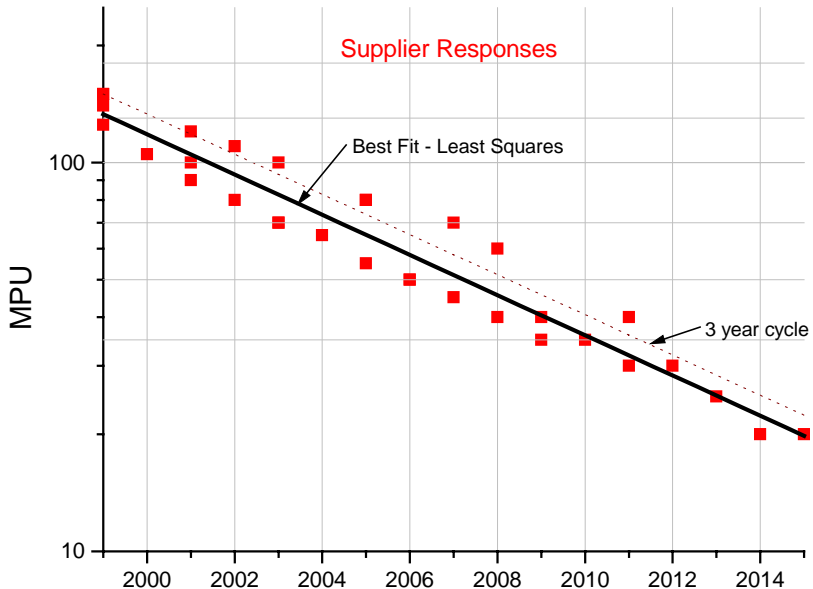
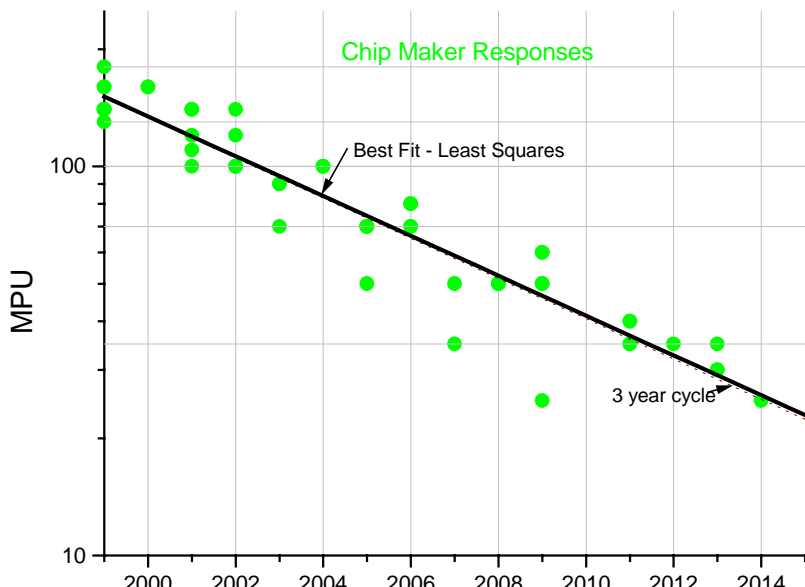
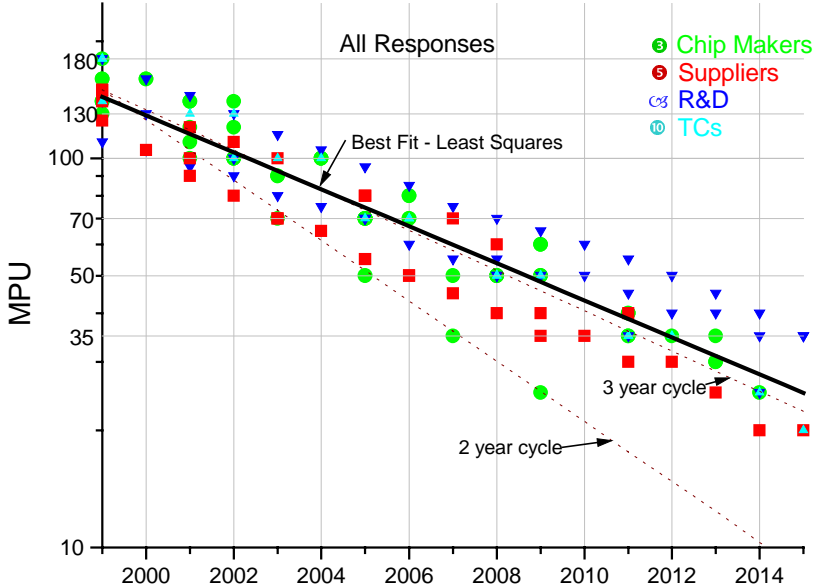
Feature Size (printed in resist)	1999	2002	2005	2008	2011	2014
DRAM Half Pitch (nm)	180	130	100	70	50	35
MPU Gate (nm)	140	90	65	45	30	20

➡ Best case opportunity to accelerate the 130nm node is 2001

➡ DRAM is on a 3 year cycle

US Litho TWG Roadmap Timing Survey - 3/99 Results

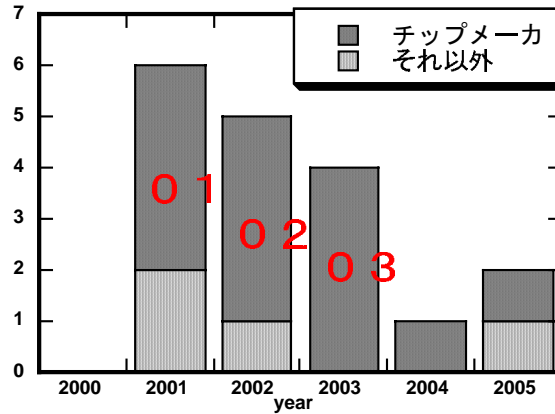
MPU Gate Length (in Resist) - 20 Responses



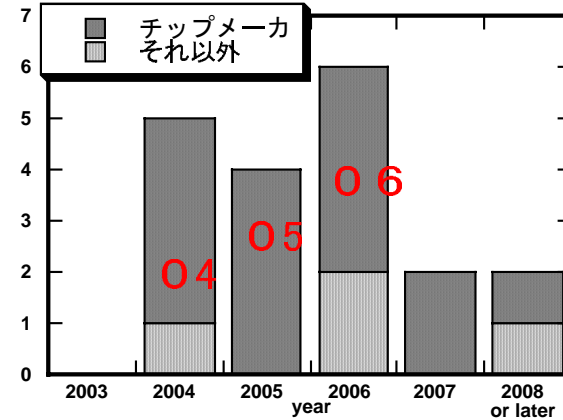
Tokyo, Japan: November 1999

Japan Litho TWG Roadmap Timing Survey

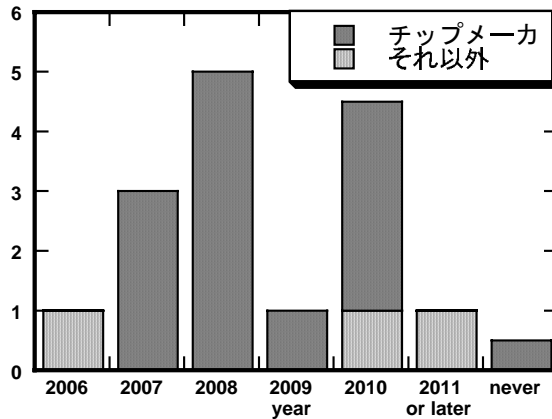
130nm



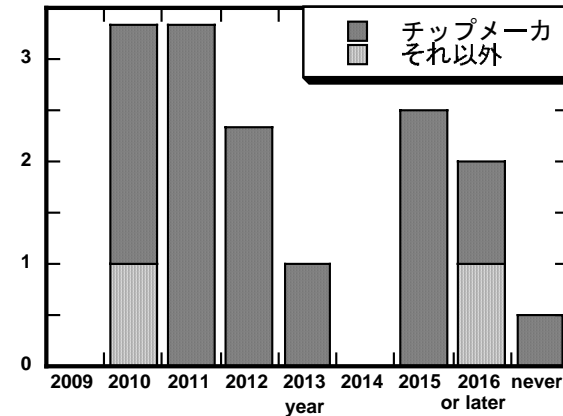
100nm



70nm



50nm

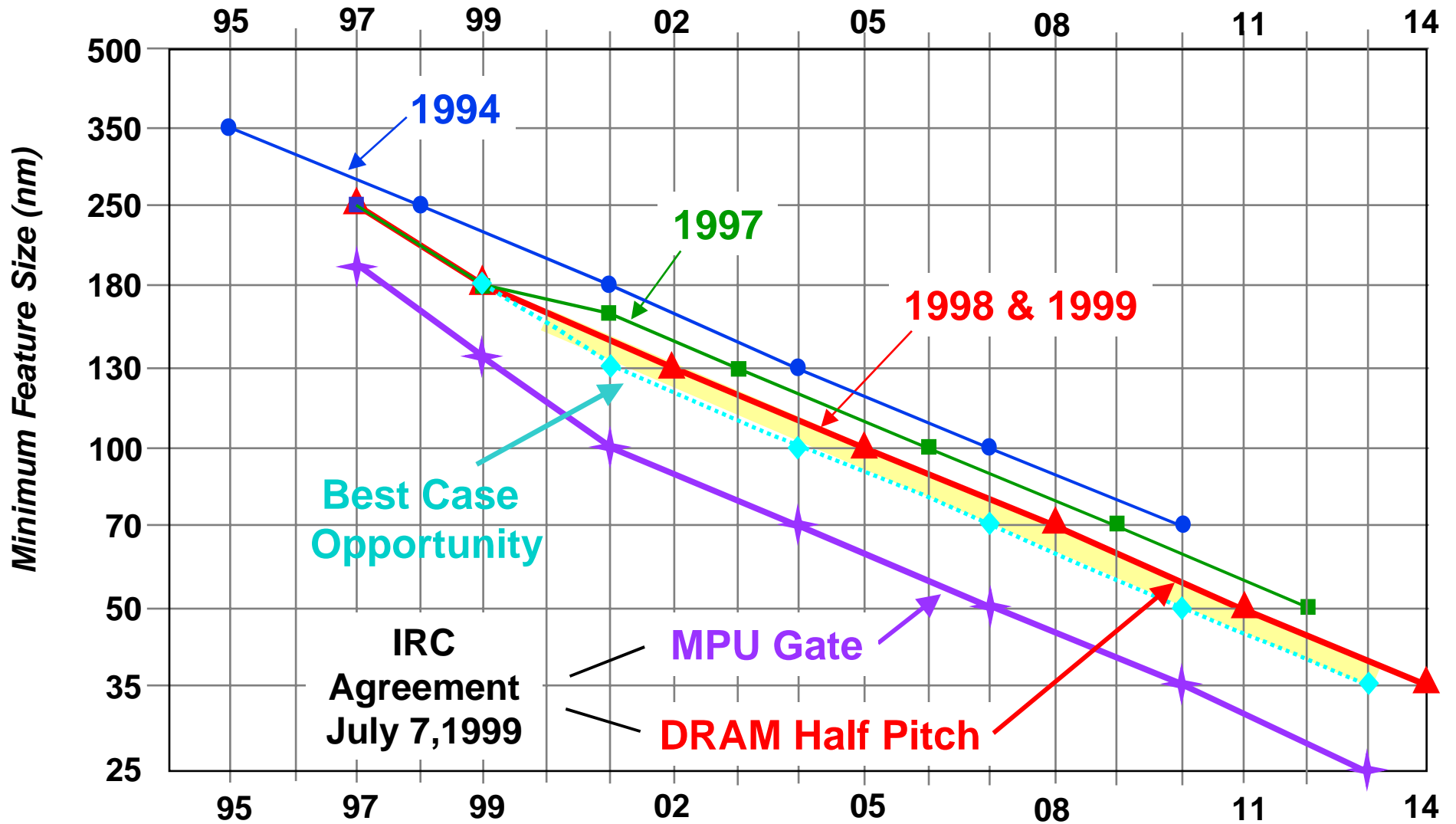


Future is divided

30 Responses

STRJ-WG5

ITRS Roadmap Acceleration



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Mask Capability

◆ Mask capability is a major limiter to progress.

⇒ Writers: Accuracy, CD Control, Feature Size, OPC, Data Volume, MEF, Image Placement

⇒ Inspection: Defect size, Actinic Capability and PSM

⇒ Repair: Lacking technology/supplier and PSM

⇒ Cost/Price: Rapid Escalation \$5k ➔ \$50k

➔ Needs major focus, paradigm shift, global collaboration!

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Key Issue - Chip Size

- ◆ Chip sizes (1.4x increase/generation) in 1997 and 1998 Roadmaps are much too large.
- ◆ Drives mask and stepper suppliers in wrong direction.
- ◆ RCG subcommittee formed 1Q99 to study issue and make recommendations. Findings are:
 - ⇒ Chip designs are driven by performance and cost.
 - Cost to first order is driven by chip size.
 - ⇒ In DRAM and MPU business, next generation chips are introduced to production when cost/function approaches that of current generations. This drives constant chip size. (1.0x increase/generation)
- ◆ Japan study group and PIDS (STRJ) proposal recommends 1.2x increase/generation.
 - ⇒ Gives the most probably and practical chip size in DRAM
 - ⇒ 4x bit capacity increase extended from 3 years to 4 years matching recent and future trend of 2x bit capacity increase every 2 years.
- ◆ IRC adopted 1.2x increase/generation (every 4 years) for both DRAM and MPU.

 ***Further opportunity to understand high performance MPU drivers.***

Lithography Difficult Challenges - Before 2005

<i>Five Difficult Challenges ≥ 100 nm Before 2005</i>	<i>Summary of Issues</i>
Optical mask fabrication with resolution enhancement techniques for ≤ 130 nm and post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (i.e., 157nm substrates and films; defect free multi-layer substrate or membranes). Development of equipment infrastructure (writers, inspection, repair) for relatively small market.
Lithography technology consensus (193nm + RET, 157nm, NGL)	Narrowing of Roadmap options for 100–50 nm nodes. Achieving global consensus among technology developers and chip manufacturers.
Cost control and return on investment (ROI)	Achieving constant/improved throughput with larger wafers Development of cost-effective resolution enhanced optical masks and post-optical masks including an affordable ASIC solution, i.e. low cost masks. Achieving ROI for industry (chipmakers, E+M suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 7 nm, 3 sigma.
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option.

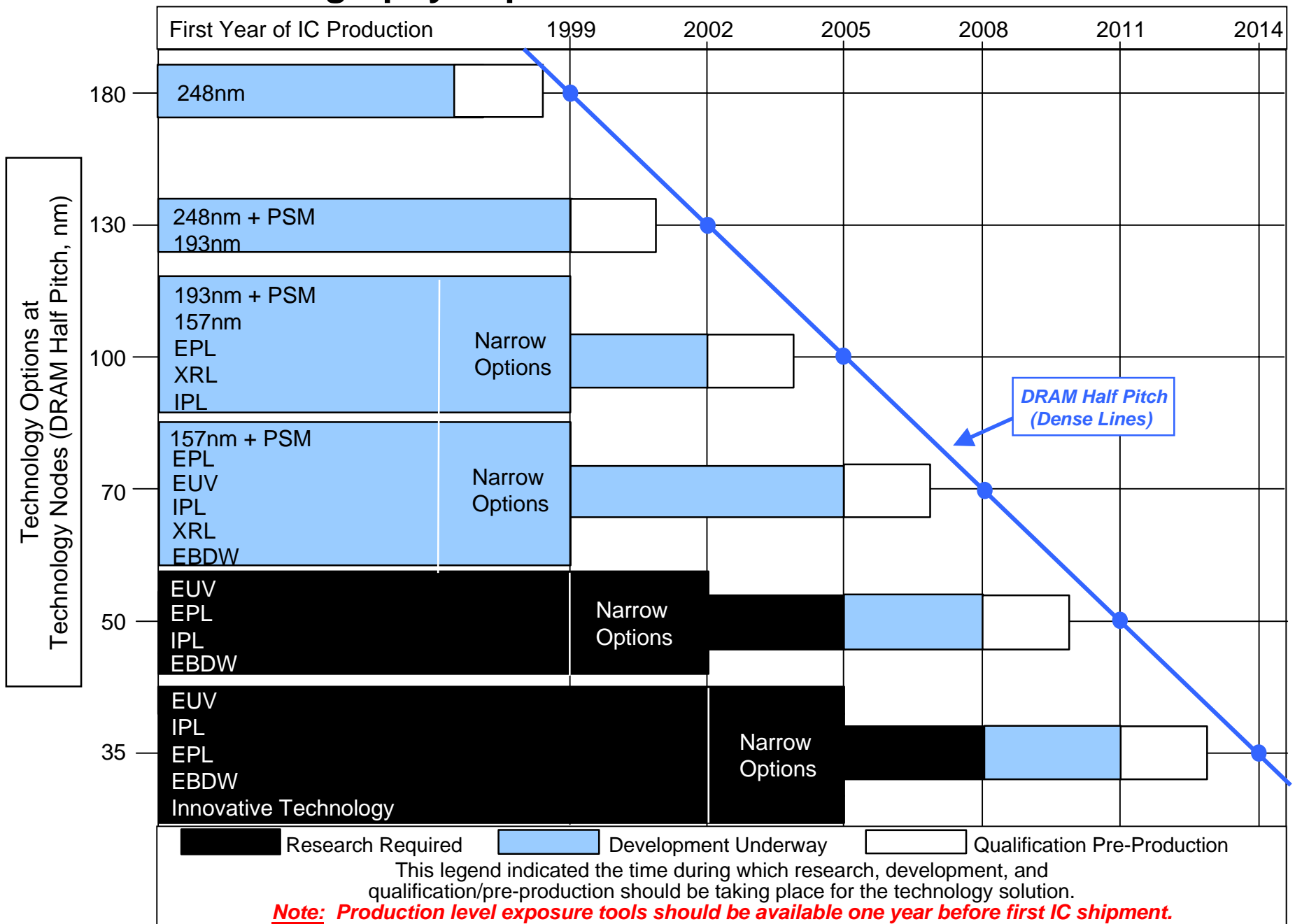
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Lithography Difficult Challenges - Beyond 2005

Five Difficult Challenges < 100nm Beyond 2005	Summary of Issues
Mask fabrication and process control	<p>Development of commercial mask manufacturing processes to meet requirements of Roadmap options (i.e., 157nm substrates and films; defect free multi-layer substrate or membranes)</p> <p>Development of equipment infrastructure (writers, inspection, repair) for relatively small market</p> <p>Development of mask process control methods to achieve critical dimension, image placement, and defect density control below 100 nm nodes</p>
Metrology and defect inspection	R&D for critical dimension and overlay metrology, and patterned wafer defect inspection for defects < 40nm.
Cost control and return on investment (ROI)	<p>Development of innovative technologies, tools, and materials to maintain historic productivity improvements</p> <p>Achieving constant/improved throughput with post-optical technologies</p> <p>Achieving ROI for industry (chipmakers, E+M suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100nm and below.</p>
Gate CD control improvements	Development of processes to control minimum feature size to less than 5 nm, 3 sigma, and reducing line edge roughness
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option

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Lithography Exposure Tool Potential Solutions



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Summary

- ◆ New format adopted to focus on unique requirements for DRAM, MPU, ASIC, and optical masks requirements.
- ◆ Roadmap timing is biggest challenge / issue for lithography.
 - ⇒ Mask capability is key limiter to progress.
 - ➔ **IRC decision reached - stay on 3 year cycle.**
- ◆ Chip size proposals afford significant relief for lithography tools and masks.
 - ➔ **IRC adopted 1.2x increase/generation.**
- ◆ Optical lithography extends domain with 157nm technology. NGL options moved to 100nm node and below.
- ◆ Best case opportunity to accelerate the 130nm node is 2001.
 - ⇒ Cost control and ROI are major concerns for acceleration at 100nm-50nm nodes (single node solutions).

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