1999 Test Roadmap

1999 TTWG Members

US Members

Name	Company
Mark Baber	Lucent
Bill Ortner	Lucent
Marc Mydill	TI
Suresh Nadig	Compaq
Don Weater	IBM
Paul Roddy	Motorola
Uli Schoettmer	HP
Peter Maxwell	HP
Steve Strauss	Intel
Brad Robbins	Teradyne
Phil Nigh	IBM
Anne Gattiker	IBM
Robert Nesbitt	Schluberger
Jody Van Horn	IBM
Rochit Rajsuman	Advantest

International Members

Name	Company
Peter Muhmenthaler	Infineon
Rene Seger	Philips
Kazumi Hatayama	Hitachi
Takeshi Onodera	Sony
Takashi Aikyo	Fujitsu

DIFFICULT TEST CHALLENGES THROUGH 2005

FIVE DIFFICULT CHALLENGES ≥ 100 nm / THROUGH 2005	SUMMARY OF ISSUES
BIST and DFT	• Test equipment costs will rise toward $20M and wafer yields may suffer without DFT and BIST. • DFT required for at-speed test with a low-speed tester. • Tools required for inserting DFT and BIST and estimating cost. • Analog BIST needed. • Access to SOC cores needed when using DFT and BIST.
DUT to ATE interface	• A major roadblock will be the need for high frequency, high pin count probes and test sockets; research and development is urgently required to lower inductance and cost. • Increasing pin-counts lead to larger test heads and longer I/O round-trip-delays (RTD). This problem can be avoided using two transmission lines but I/O pins must then drive 25 ohms. • Power and thermal management problems. Non-uniform wafer temperatures. • Simulation needed for the path from the device through the package to the ATE pin electronics. • Interface circuits must not degrade ATE accuracy or introduce noise. Especially for high-frequency differential DUT I/O. • Faster automatic package handlers are required.
Mixed-Signal instruments	• These will require more bandwidth, higher sample rates, and lower noise. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits.
Failure analysis	• 3-D CAD and FA systems for isolation of defects in multi-layer metal processes. • New fault models, e.g. for crosstalk. • Automatic test generators for fault diagnosis.
Test development.	• Automatic test program generators to reduce test development time. • Standard test software, e.g. STIL , IEEE P1500 • Reuse of test software for embedded SOC cores to reduce test development time. • Simulation of the ATE, interface, and DUT to avoid test development on expensive ATE. (virtual testing). • New test methods required.

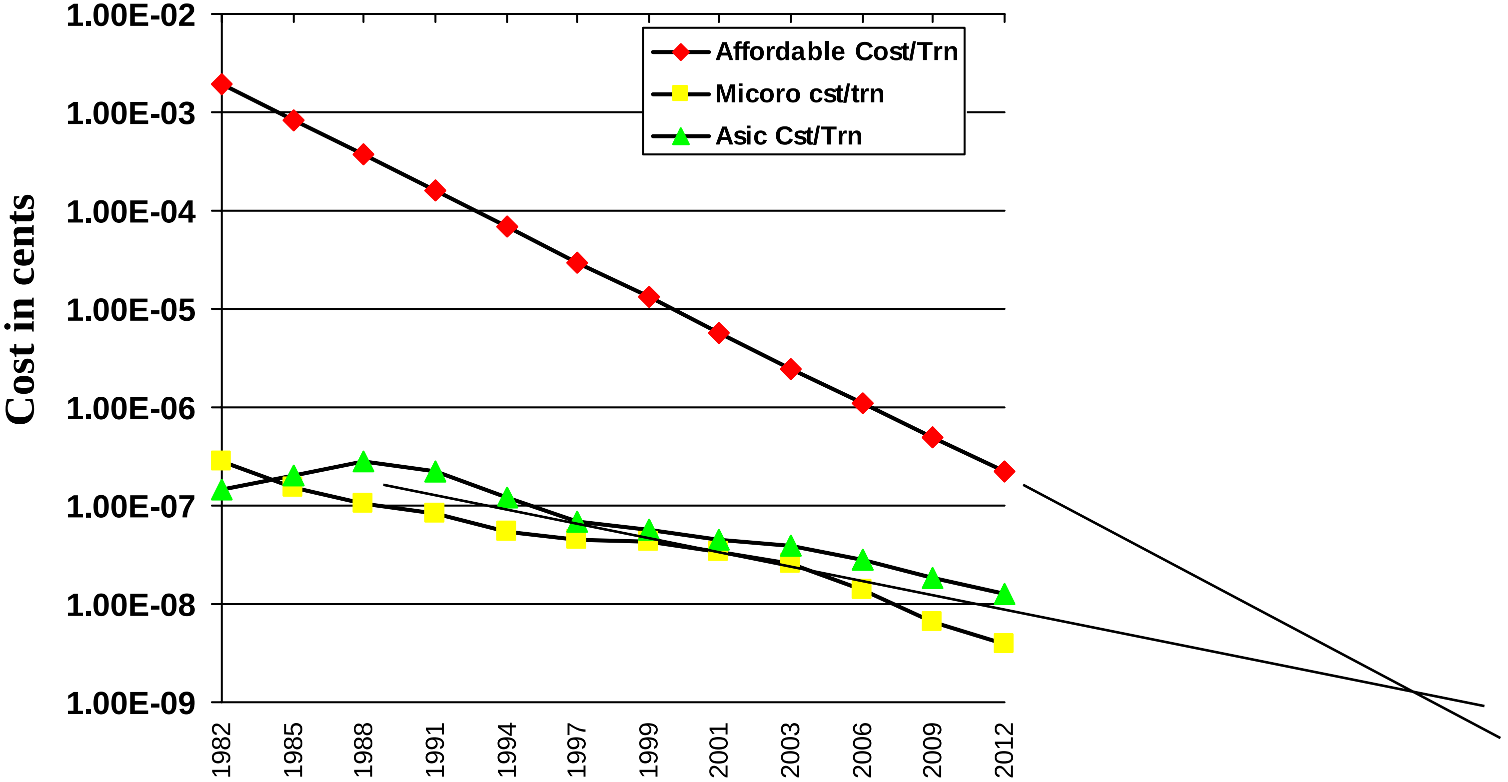
DIFFICULT CHALLENGES BEYOND 2005

FIVE DIFFICULT CHALLENGES < 100 nm / BEYOND 2005	
DUT to ATE interface	• Optical probing techniques. • Full wafer test. • Power and thermal management problems, especially with 300 mm wafers. • Contactless probing using BIST (see DFT/BIST ATE section).
SOC test methods	• New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Possibly test should be developed utilizing the design hierarchy. • Analog BIST. • Logic BIST for new fault models. • Deterministic self-test instead of pseudo random test patterns. • EDA tools for DFT selection considering cost/performance issues.
MEMs, Sensors, and new IC technologies	• Develop new test methods.
New burn-in techniques.	• Research is required. The promise of IDDQ testing as a burn-in replacement method has not been fulfilled.
Failure analysis.	• Real-time analysis of defects in multi-layer metal processes. • New fault models, e.g. cross-talk. • Failure analysis for analog devices.

TEST TWG - GENERAL ISSUES

- **FORCASTEING THE DEMISE OF @SPEED FUNCTIONAL TESTING**
  - **When will DFT/BIST eliminate the need for expensive @speed functional testing**
  - **The 1997 roadmap forecasted the $20 M TEST SYSTEM**

Tester Cost/Transistor/Socket



TEST TWG - GENERAL ISSUES

- **FORCASTEING THE DEMISE OF @SPEED FUNCTIONAL TESTING**
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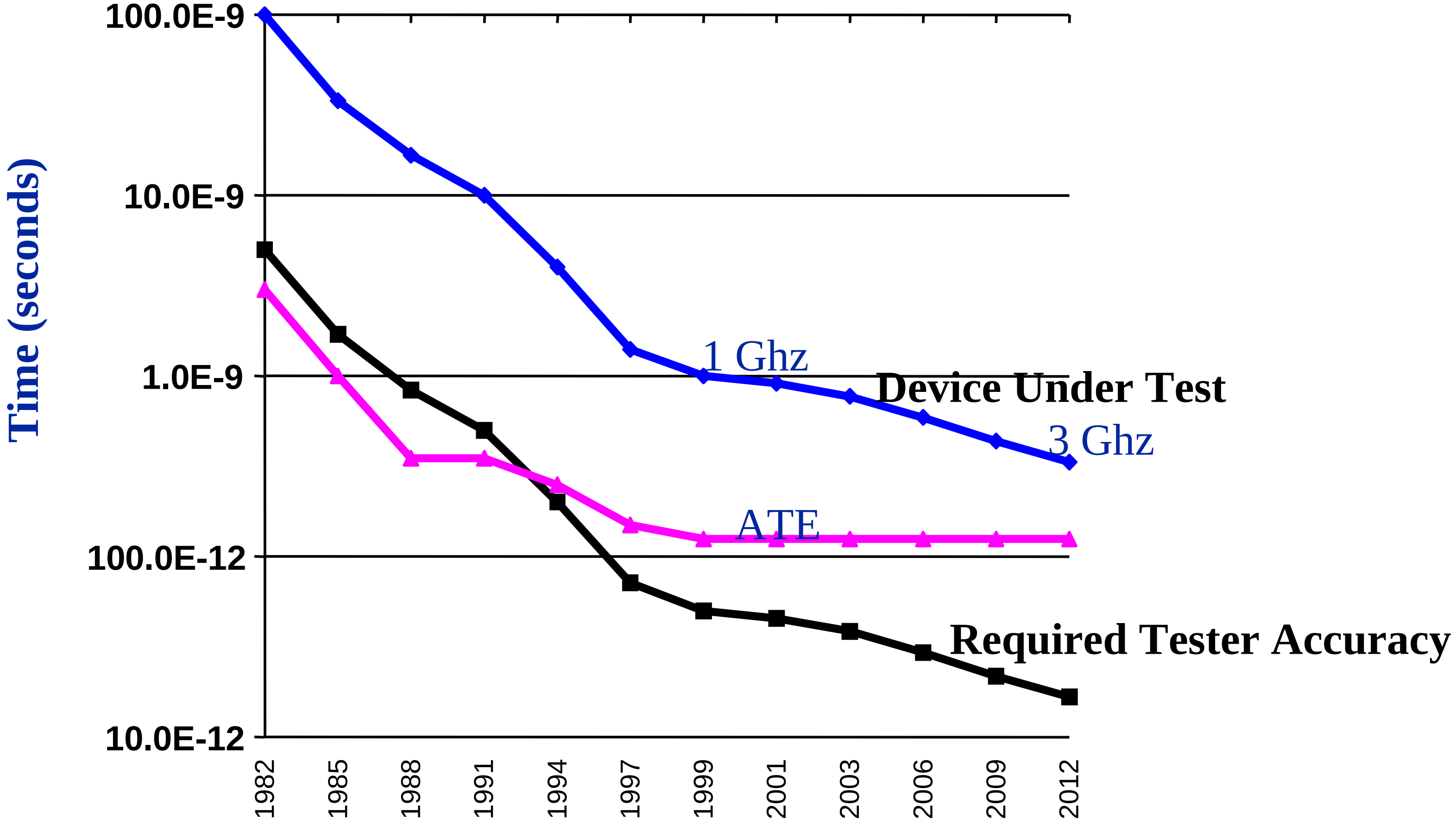
  - **The 1997 roadmap forecasted the $20 M TEST SYSTEM**

- **To avoid falling wafer and package yields due to automatic test equipment (ATE) accuracy limitations.**

Tester Accuracy impact of Yield



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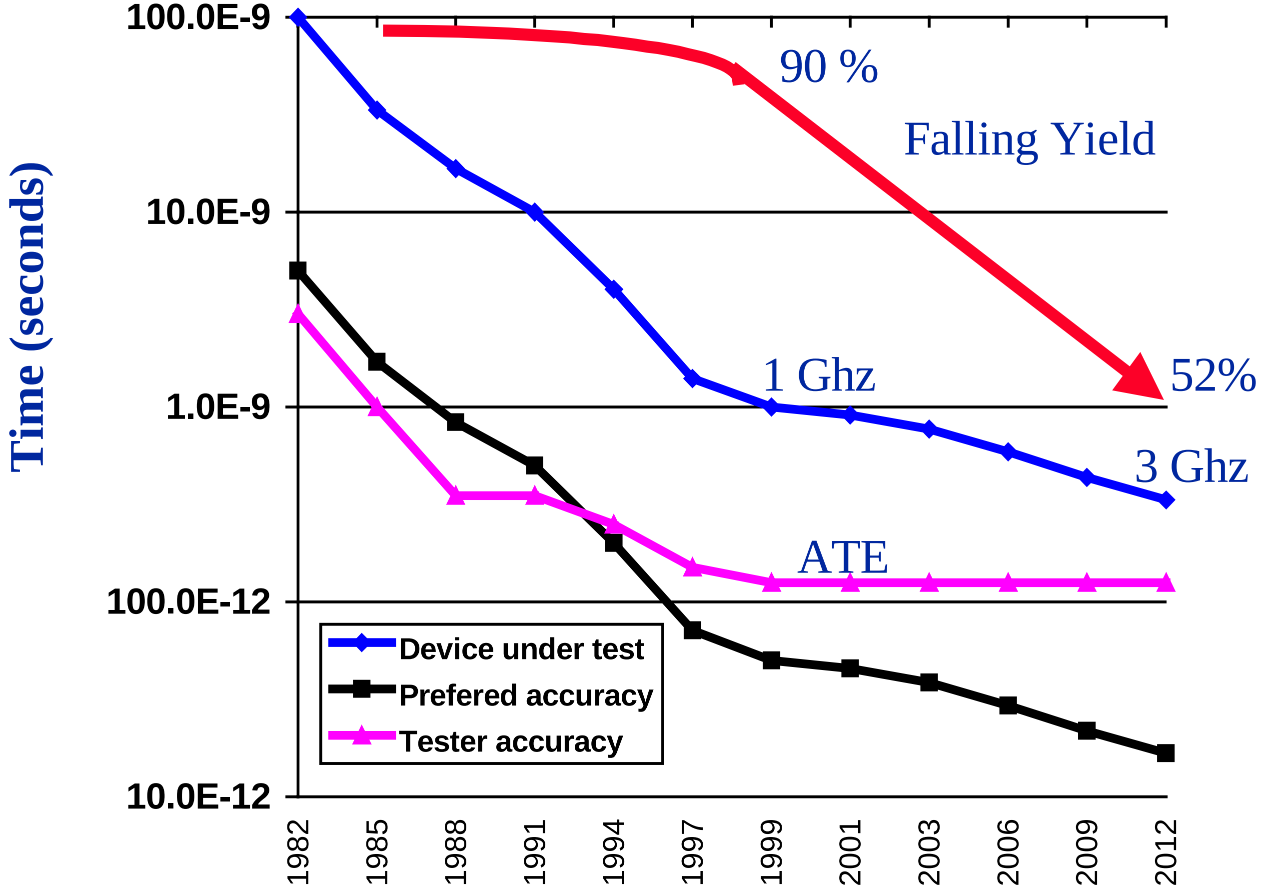

TEST TWG - GENERAL ISSUES

- **Forecasting The Demise Of @Speed Functional Testing**
  - **When will DFT/BIST eliminate the need for expensive @speed functional testing**
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- **To Avoid Falling Wafer and Package Yields Due to Automatic Test Equipment (ATE) Accuracy Limitations.**

- **What Is the Future Impact for IDDQ As a Test**

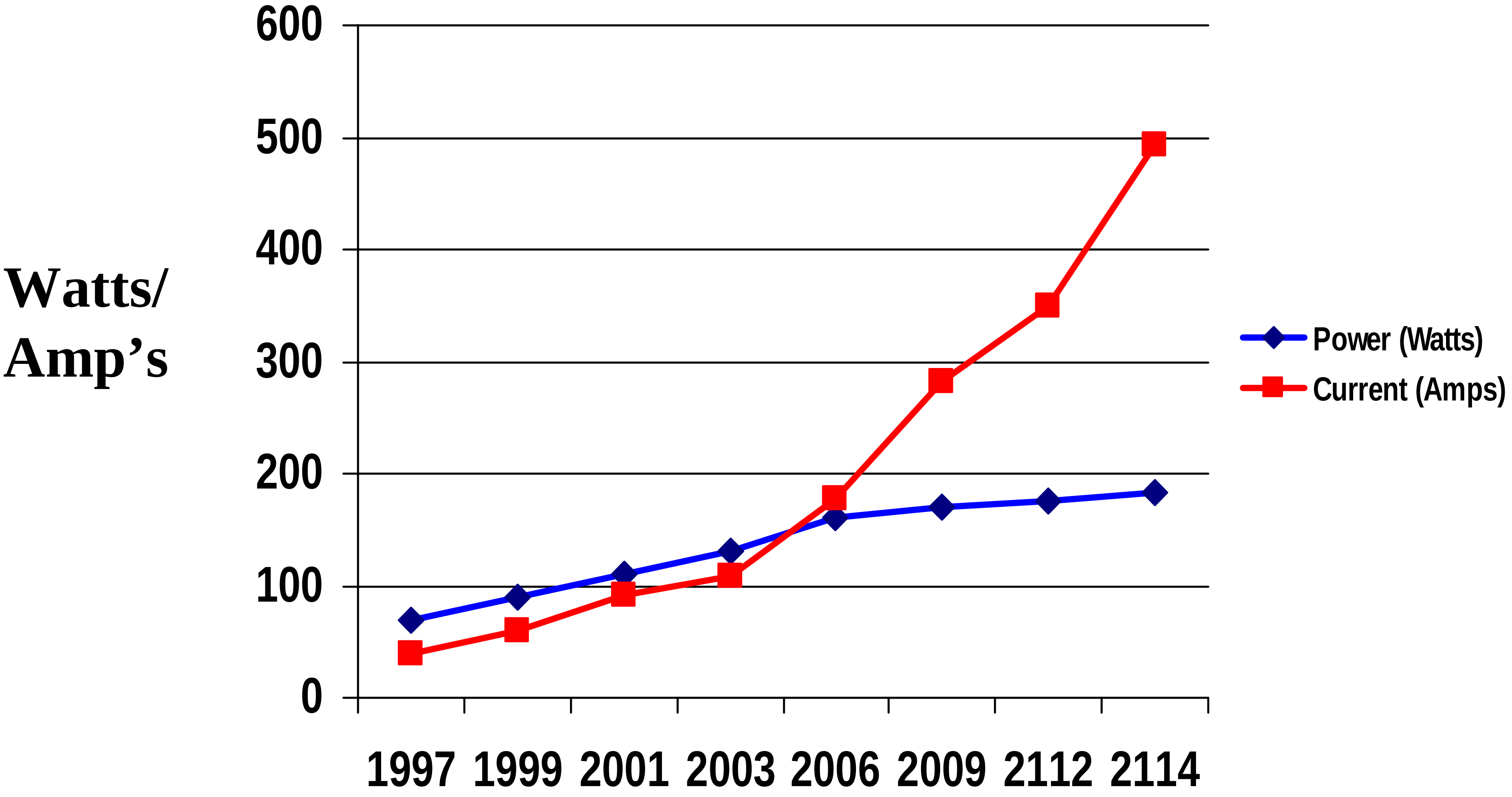
IDDQ TESTING
PROJECTED MAX. IDDQ IN HIGH-PERF. ICs

Year	Maximum IDDQ
1997	1 - 10 mA
1999	1 - 10 mA
2001	10 - 20 mA
2003	20 - 30 mA
2006	30 - 60 mA
2009	100 - 400 mA
2012	100 - 1,000 mA
2014	??????

TEST TWG - GENERAL ISSUES

- Forecasting The Demise Of @Speed Functional Testing
    - When will DFT/BIST eliminate the need for expensive @speed functional testing
    - The 1997 roadmap forecasted the $20 M TEST SYSTEM
- To Avoid Falling Wafer and Package Yields Due to Automatic Test Equipment (ATE) Accuracy Limitations.
- What Is the Future Impact for IDDQ As a Test
- Power Management May Be the Biggest Single TEST Challenge

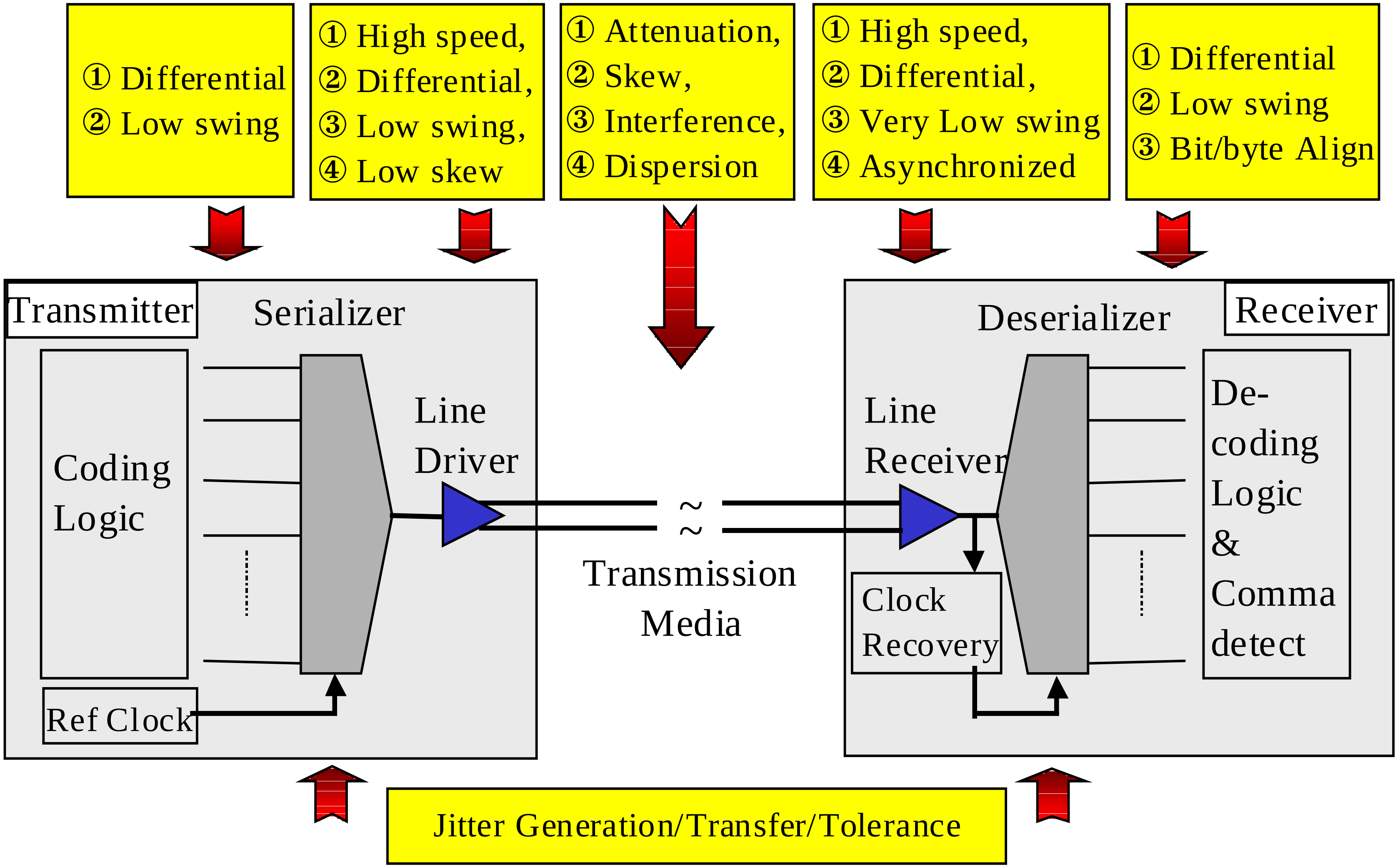
Power Management



HIGH-FREQ. SERIAL COMMUNICATIONS

- **A NEW SECTION ON HIGH-FREQUENCY, SERIAL COMMUNICATIONS DEVICE TESTING HAS BEEN ADDED.**
  - **IT EXPLAINS THE SPECIAL PROBLEMS ASSOCIATED WITH TESTING LOW-VOLTAGE (~ 100 mV), DIFFERENTIAL SIGNALS AT FREQUENCIES RANGING FROM 624 Mb/s - 10 Gb/s FOR SYSTEMS SUCH AS SONET FIREWIRE, FIBRE CHANNEL, & GIGABIT ETHERNET ETC.**

Challenges for Testing Serial Communication Devices



① Differential
② Low swing

① High speed,
② Differential,
③ Low swing,
④ Low skew

① Attenuation,
② Skew,
③ Interference,
④ Dispersion

① High speed,
② Differential,
③ Very Low swing
④ Asynchronized

① Differential
② Low swing
③ Bit/byte Align

Transmitter

Serializer

Coding Logic

Ref Clock

Line Driver

Transmission Media

Deserializer

Receiver

Line Receiver

Clock Recovery

De-coding Logic & Comma detect

Jitter Generation/Transfer/Tolerance

TEST EQUIPMENT TABLES HAVE BEEN INCREASED FROM 2 TO 8

HIGH-PERFORMANCE ASICS

HIGH-PERFORMANCE MICROPROCESSORS

LOW-END MICROCONTROLLERS

MIXED-SIGNAL AND WIRELESS

ATE FOR ICs WITH DFT

COMMODITY DRAMS

EMBEDDED DRAMS

EMBEDDED FLASH MEMORIES

HIGH PERFORMANCE ASIC TEST REQUIREMENTS

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003
On-chip local clock freq. MHz RZ*	**1250**	**1500**	**1800**	**2100**	**2500**
Off-chip data freq. MHz NRZ**	**1000**	**1200**	**1400**	**1600**	**1730**
Overall timing accuracy (% period)	**+/-5**	**+/-5**	**+/-5**	**+/-5**	**+/-5**
ATE RMS clock jitter peak – peak ps	**20**	**20**	**10**	**10**	**5**
Signal pk-pk range V.	**1.5 – 3.3**	**1.4 – 3.3**	**1.3 – 3.3**	**1.2 – 3.3**	**1.0 – 3.3**
Power/device DC with heat sink W.	**90**	**100**	**115**	**130**	**140**
Transient power with heat sink W.	**135**	**150**	**170**	**195**	**210**
Tester cost per high-frequency signal pin $K.	**4 - 8**	**3 - 7**	**3 - 7**	**3 - 6**	**3 - 6**
Maximum number of I/O signal pads, plus power and ground for wafer test.	**1850**	**2100**	**2300**	**2550**	**2850**
IDDQ	**Test**	**Test**	**Test**	**Test**	**Analysis**

MICROPROCESSOR TEST REQUIREMENTS

YEAR OF INTRODUCTION	*1999 180 nm*	*2000*	*2001*	*2002 130 nm*	*2003*	*2004*
Pin Count						
Pin Count I/O Tester Channels (Max) Note2	**768**	**1024**	**1024**	**1024**	**1024**	**1024**
Pin Count Power and Ground (Max Pins)	**1536**	**1536**	**2018**	**2018**	**2018**	**2018**
Busses						
Clock input Frequency (Mhz) *(Note 3)*	**800**	**933**	**1066**	**1200**	**1333**	**1466**
Clock Accuracy (ps) *(Note 4)*	**62**	**53**	**47**	**42**	**37**	**34**
Off-chip Bus Data Rate (Mb/s)	**600**	**700**	**800**	**900**	**1000**	**1100**
Accuracy OTA (ps)	**75**	**70**	**67**	**62**	**60**	**57**
Embedded Memory (Mbits)	**32**	**32**	**64**	**64**	**128**	**128**
Algorithmic Pattern Generator (#X, Y Addresses)	**16**	**16**	**16**	**16**	**32**	**32**
Algorithmic Pattern Generator (#Z Addresses)	**4**	**4**	**4**	**4**	**8**	**8**
Power Supplies						
Max Current (A)	**200.0**	**200.0**	**220**	**220**	**242**	**242**
Patterns						
Vector Memory (Meg – Vectors per pin)	**64**	**64**	**128**	**128**	**256**	**256**
Cost						
Tester Cost per pin ($)	**8000**	**7500**	**7000**	**6500**	**6000**	**5500**

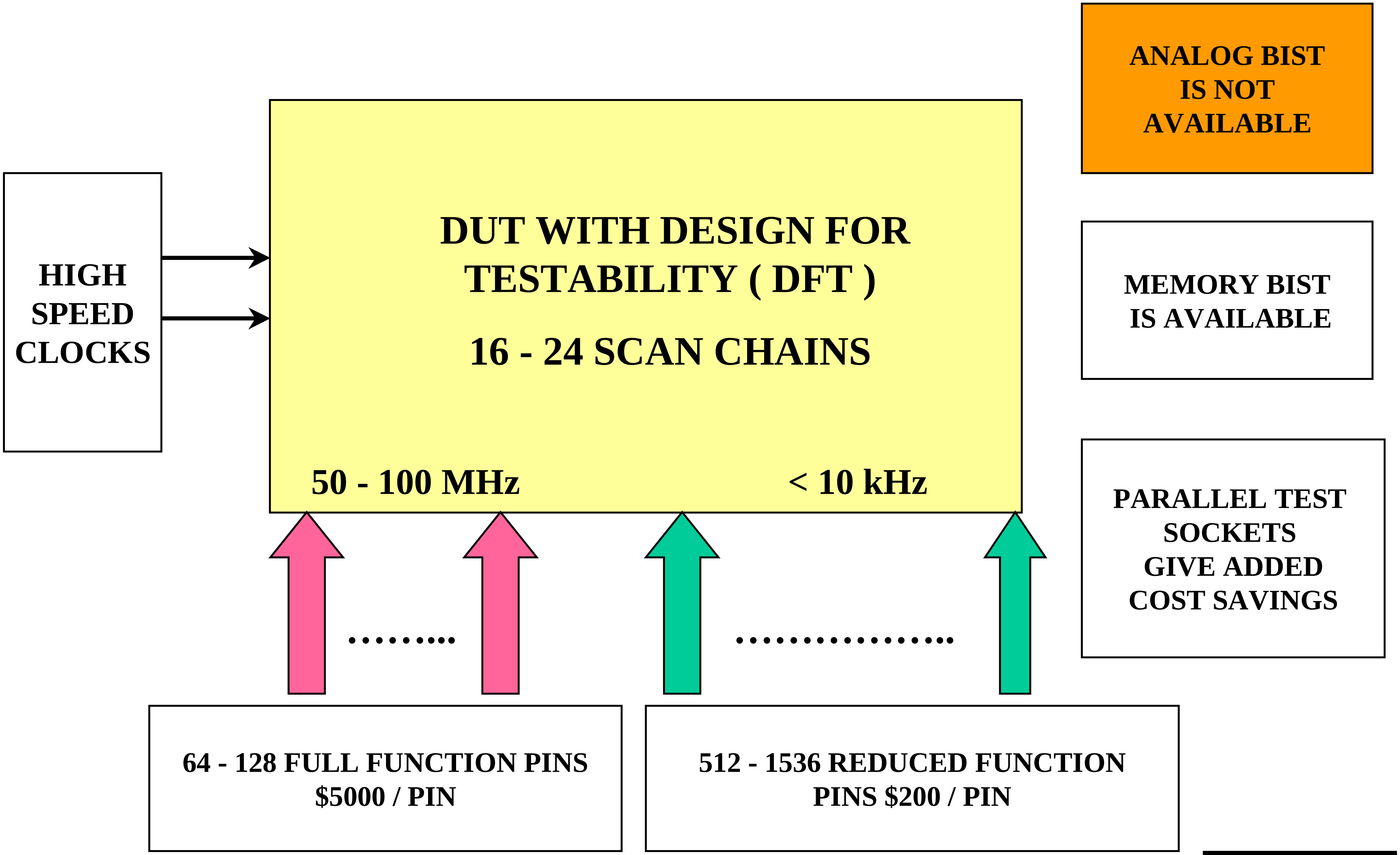
MICROCONTROLLER TEST REQUIREMENTS

YEAR OF INTRODUCTION	*1999*	*2000*	*2001*	*2002*	*2003*	*2004*
Device Characteristics						
Pin Count: min/max pins	**3/160**	**3/180**	**3/200**	**3/210**	**3/220**	**3/230**
Clock Frequency (MHz)	**60**	**70**	**80**	**85**	**90**	**95**
Device power (mW)	**300**	**300**	**300**	**300**	**300**	**300**
Max driver level (V) (note A)	**8**	**10**	**12**	**12**	**15**	**20**
Max comparator level (V) (note A)	**8**	**10**	**12**	**12**	**15**	**20**
Embedded Memory (Mbits)	**8**	**12**	**16**	**20**	**32**	**32**
Tester Characteristics						
External Test Vectors (M) (Note B)	**8**	**8**	**8**	**12**	**12**	**12**
Tester Cost range ($K/per pin)	**2-4**	**2-4**	**2-4**	**1.5-3**	**1.5-3**	**1.3-3**
Max # of DPS in tester	**16**	**32**	**32**	**48**	**48**	**64**
Max # of devices for parallel testing (Note C)	**8**	**16**	**16**	**16**	**24**	**24**
Max number of tester pins	**1024**	**1024**	**1024**	**1024**	**1536**	**1536**
Mixed-signal instrumentation	**A/D, D/A**		**Audio Fre-quency**		**Video Fre-quency**	

MIXED-SIGNAL & RF/MICROWAVE TEST REQUIREMENTS

- **TABLES ARE ESSENTIALLY THE SAME AS THOSE POSTED IN 1998 ON THE SEMATECH WEB PAGE.**
- **YEARS HAVE BEEN ADJUSTED TO COVER 1999 - 2014.**
- **REQUIRED NOISE FLOORS FOR HIGH-FREQ. SOURCE AND DIGITIZER HAVE BEEN LOWERED**
  - **THE LOWER LEVELS (-140 dB/RT/Hz) REQUIRE DEVELOPMENT EFFORTS BY ATE MANUFACTURERS.**

LOW COST TESTING OF DEVICES DESIGNED WITH DFT



ANALOG BIST
IS NOT
AVAILABLE

HIGH
SPEED
CLOCKS

DUT WITH DESIGN FOR
TESTABILITY (DFT)

16 - 24 SCAN CHAINS

50 - 100 MHz

< 10 kHz

MEMORY BIST
IS AVAILABLE

PARALLEL TEST
SOCKETS
GIVE ADDED
COST SAVINGS

……….

………………..

64 - 128 FULL FUNCTION PINS
$5000 / PIN

512 - 1536 REDUCED FUNCTION
PINS $200 / PIN

ATE FOR TESTING ICs WITH DFT

YEAR OF INTRODUCTION	1999 180 nm	2000	2001	2002 130 nm	2003	2004
DFT/BIST ATE Characteristics						
Scan Chains (Chains)	**16-24**	**16-24**	**24-32**	**24-32**	**32-64**	**32-64**
Scan Vectors (M-Vectors) (3 bits/ vector min) At max width	**4-16**	**4-16**	**8-32**	**8-32**	**8-32**	**8-64**
DFT Req'd to Cap test application time "Logic BIST"			**Logic BIST to 90%**	**Logic BIST to 93%**	**Logic BIST to 95%**	**Logic BIST to 98%**
DFT Req'd to prevent addition of APG into ATE "SRAM + DRAM BIST"	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Vector Rate (Mhz)	**50-100**	**100-200**	**100-200**	**100-200**	**100-200**	**200**
Non-scan pin vectors (M-Vectors)	**4-8**	**4-16**	**4-16**	**4-16**	**4-16**	**8-24**
Total "Full function" Pin Count Scan+ nonscan per Socket (pins)	**64-128**	**64-128**	**64-256**	**64-256**	**64-256**	**64-256**
System Base Data Rate (MHz)	**100-200**	**100-200**	**200**	**200**	**200**	**200**
Number of Parallel Sites (sites)	**2-4**	**4-16**	**4-16**	**4-16**	**4-16**	**4-16**
Specialized functions						
Total "Reduced Function" Pin count	**512-1536**	**512-2048**	**512-2200**	**512-2400**	**512-2600**	**512-2800**

COMMODITY DRAM TESTING

YEAR OF INTRODUCTION DRAM half-pitch (nm)	1999 180	2000	2001	2002 130	2003	2004
Table: Testing of Commodity DRAMs						
DRAM Capacity (Gega-bits): R&D Mass Production	**1** **0.256**		**1 1**		**4 1**	
DRAM Data Rate (Gega-Hz): R&D Mass Production	**1.0** **0.250**		**1.3** **1.0**		**1.6** **1.3**	
DRAM Access Time (ns): R&D Mass Production	**2.5 8**		**2 4**		**1** **2.5**	
DRAM Bit Width/device (Mass Production)	**8**		**16**		**16**	
Tester Data Rate (Gega-Hz): R&D Mass Production	**1.0 0.25**		**1.3** **1.0**		**1.6** **1.3**	
Overall Timing Accuracy (ps): R&D Mass Production	**100** **300**		**60 80**		**50 60**	
Simultaneous Testing (Devices/test head)	**32**		**32/64**		**64**	
Test Channels (Mass Production)	**1500***		**1200** **2 2300****		**2300**	

SYSTEM-ON-A-CHIP (SOC) TESTING

- A section on technology requirements for SOC testing will be included in the Design Chapter. Seven areas will be highlighted:
  - **New fault models for cross-talk and new failure modes.**
  - **New test methods involving BIST, IDDQ etc.**
  - **DFT at gate-level, RTL, behavioural level etc.**
  - **Logic BIST with repair, analog BIST etc.**
  - **Standards for test data, test methods, fault models. Allows test reuse.**
  - **Test cost reduction.**
  - **Failure analysis.**

EMBEDDED DRAM TESTING

YEAR OF INTRODUCTION *DRAM half-pitch (nm)*	*1999* *180*	*2000*	*2001*	*2002* *130*	*2003*	*2004*
Table: Testing of Embedded DRAMs						
Embedded DRAM size (Mega-bits): R&D Mass Production	**64** **16**		**128** **32**		**256** **64**	
Failure Concerns	**Particle defects; data retention**		**Particle defects; array noise; data retention**		**Particle defects; array noise; sense-amp imbalance**	
Wafer Level Test	**Single insertion**		**Double insertion**		**Double insertion**	
On-Chip Test	**50% BIST** **50% BISR**		**100% BIST** **100% BISR**		**100% BIST** **100% BISR**	

EMBEDDED FLASH TESTING

YEAR OF INTRODUCTION *DRAM half-pitch (nm)*	*1999* *180*	*2000*	*2001*	*2002* *130*	*2003*
Table: Testing of Embedded Flash Memories					
Embedded Flash size (Mega-bits): R&D Mass Production	**4** **2**		**16** **4**		**32** **16**
Embedded Mixed Memory Size (Mega-bits): Flash DRAM	**0.256** **1**		**1** **4**		**4** **16**
Failure Concerns	**Oxide defects; # of erase cycles**		**Oxide defects; ONO scaling**		**Oxide defects; ONO scaling; over erase**
Wafer Level Test	**Single insertion**		**Single insertion**		**Double insertion**
On-Chip Test	**50%BIST** **50%BISR**		**100%BIST** **100%BISR**		**100%BIST** **100%BISR**