Lithography ITWG Report for ITRS Roadmap Conference

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Santa Clara, California

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Lithography ITWG Report

Outline

- Format
- Key Issues / Concerns
- Difficult Challenges
- Lithography Requirements
- Potential Solutions
- Summary

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Lithography ITWG Report

Format

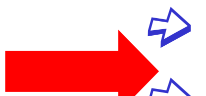
- Revised “Lithography Requirements” table based on input of ITWG meeting 12/7/98 in Colorado.
  - Focus on DRAM, MPU and ASIC unique needs.
  - Include new chip sizes.
- Revised “Mask Requirements” table to differentiate Optical needs from NGL.
  - Address mask error function (MEF) for advanced optical low k_1 applications.
  - Enlarge PSM requirements.

Lithography ITWG Report

Roadmap Timing

- Timing has been one of biggest concerns for the Lithography TWGS.
- Discussed extensively among Japan, USA, Korea, Europe and Taiwan.
- Tentative agreement reached in Munich, April 13th, with IRC:
- Agreement reached with IRC at 7/7/99 Roadmap Workshop

Feature size (printed in resist)	1999	2002	2005	2008	2011	2014
DRAM Half Pitch (nm)	180	130	100	70	50	35
MPU Gate (nm)	140	90	65	45	30	20



- Best case opportunity to accelerate the 130nm node is 2001
- DRAM is on a 3 year cycle

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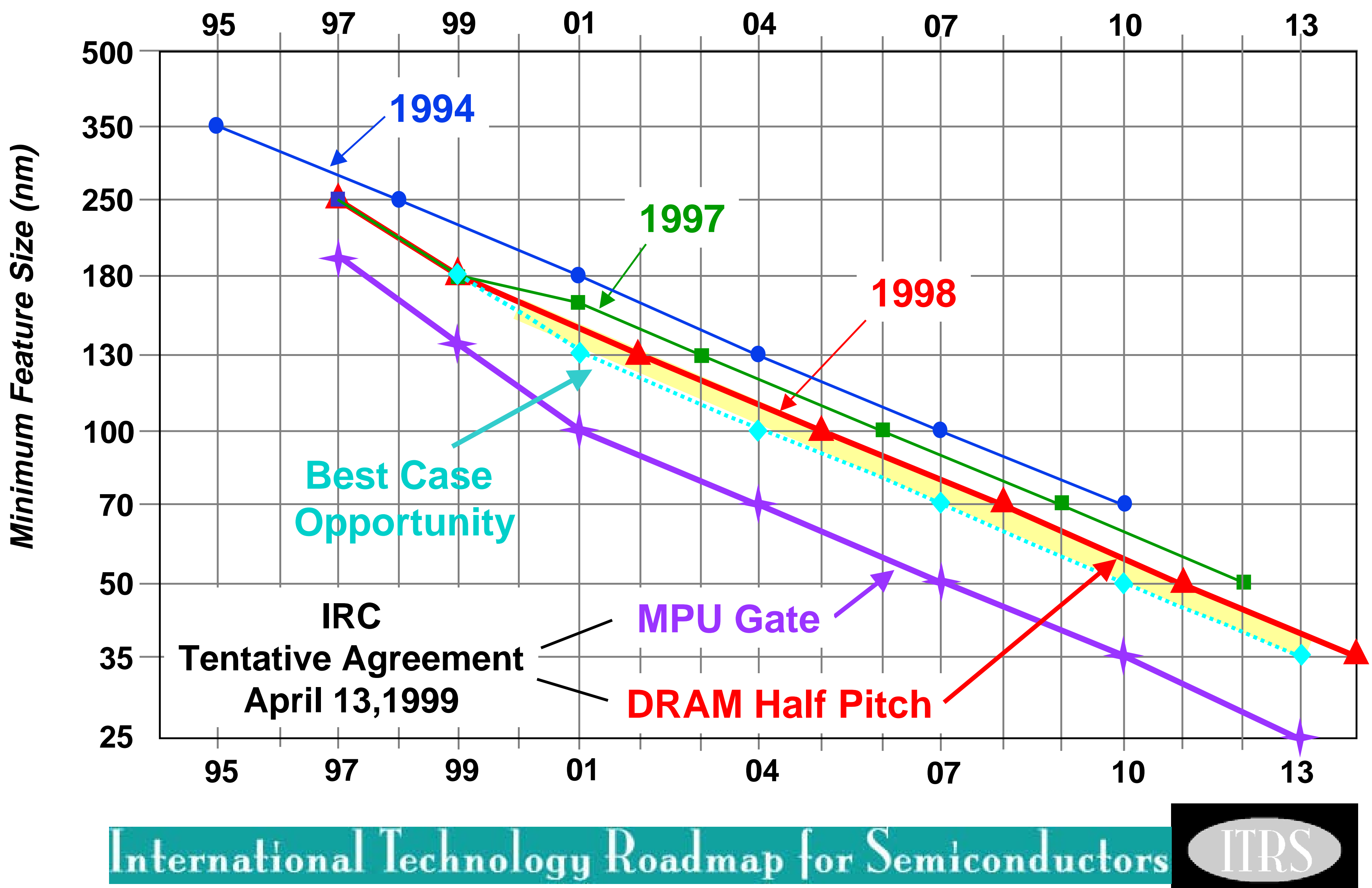
SIA Roadmap Acceleration



International Technology Roadmap for Semiconductors

ITRS

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Mask Capability

- Mask capability is a major limiter to progress.
  - Writers: Accuracy, CD Control, Feature Size, OPC, Data Volume, MEF, Image Placement
  - Inspection: Defect size, Actinic Capability and PSM
  - Repair: Lacking technology/supplier and PSM
  - Cost/Price: Rapid Escalation $5k ➨ $50k

➡ ***Needs major focus, paradigm shift, global collaboration!***

Lithography ITWG Report

Chip Size

- Chip sizes in 1997 and 1998 Roadmaps are much too large.
- Drives mask and stepper suppliers in wrong direction.
- RCG subcommittee formed 1Q99 to study issue and make recommendations. Findings are:
  - Chip designs are driven by performance and cost.
    - Cost to first order is driven by chip size.
  - In DRAM and MPU business, next generation chips are introduced to production when cost/function approaches that of current generations. This drives constant chip size.
  - Recommended chip sizes are:

Area (mm^2)		Sample	Production	Ramp	Peak
DRAM (Flat)		300	150	75	38
MPU (Flat)	CP		340	160	75
	MP			195	92
	HP			440	215

  - 22x22mm field captures all requirements.
- Proposal affords significant relief for lithography tools and masks.

Need industry feedback, IRC adoption!

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Table 23 Lithography Difficult Challenges

Five Difficult Challenges ≥ 100 nm Before 2005	*Summary of Issues*
Optical mask fabrication with resolution enhancement techniques for ≤ 130 nm and post-optical mask fabrication	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (i.e., 157nm substrates and films; defect free multi-layer substrate or membranes). Development of equipment infrastructure (writers, inspection, repair) for relatively small market.
Lithography technology consensus (193nm + RET, 157nm, NGL)	Narrowing of Roadmap options for 100–50 nm nodes. Achieving global consensus among technology developers and chip manufacturers.
Cost control and return on investment (ROI)	Achieving constant/improved throughput with larger wafers Development of cost-effective resolution enhanced optical masks and post-optical masks including an affordable ASIC solution, i.e. low cost masks. Achieving ROI for industry (chipmakers, E+M suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 7 nm, 3 sigma.
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option.

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Table 23 Lithography Difficult Challenges

Five Difficult Challenges < 100nm Beyond 2005	*Summary of Issues*
Mask fabrication and process control	Development of commercial mask manufacturing processes to meet requirements of Roadmap options (i.e., 157nm substrates and films; defect free multi-layer substrate or membranes) Development of equipment infrastructure (writers, inspection, repair) for relatively small market Development of mask process control methods to achieve critical dimension, image placement, and defect density control below 100 nm nodes
Metrology and defect inspection	R&D for critical dimension and overlay metrology, and patterned wafer defect inspection for defects < 40nm.
Cost control and return on investment (ROI)	Development of innovative technologies, tools, and materials to maintain historic productivity improvements Achieving constant/improved throughput with post-optical technologies Achieving ROI for industry (chipmakers, E+M suppliers, and infrastructure) on large investments necessary for Roadmap acceleration, especially single node solutions at 100nm and below.
Gate CD control improvements	Development of processes to control minimum feature size to less than 5 nm, 3 sigma, and reducing line edge roughness
Overlay improvements	Development of new and improved alignment and overlay control methods independent of technology option

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Table 24 Lithography Requirement - Overview

Year of Introduction	1999	2002	2005	2008	2011
Minimum Feature Size (nm) Dense Lines (printed in resist)	180	130	100	70	50
Isolated Lines (nm) (printed in resist)	140	90	65	45	30
Gate CD Control (nm) (3 sigma post etch)	13	8	6	4	3
Overlay (nm) (mean + 3 sigma)	65	45	35	25	20
Minimum Field Size (mm x mm)	22 x 22	22 x 22	22 x 22	22 x 22	22 x 22
Mask Size (mm) (square / diameter)	152	152	152 / 200	152 / 200	152 / 200
Defect Density (Defects per layer/m^2 @ nm)	80 @ 60nm	60 @ 40nm	50 @30nm	40 @20nm	30 @15nm

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Table 24a Short Term Lithography Requirements

Year of Introduction *"Technology Node"*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*	*Driver*
DRAM								
Half Pitch (nm)	180	165	150	130	120	110	100	
Contacts (nm)	200	185	170	150	145	140	130	
Overlay (nm, mean + sigma)	65	58	52	45	42	38	35	
CD Control (nm, 3 sigma, post-etch)	18	17	15	13	12	11	10	
Chip Size (mm^2)		*See*	*Table*	*24c*				
MPU								
Half Pitch	230	210	180	160	145	130	115	
Gate Length (nm, in resist)	140	120	100	90	80	70	65	
Gate Length (nm, post-etch)	125	108	90	81	72	63	59	
Contacts (nm, in resist)	230	210	180	160	145	130	115	
Gate CD Control (nm, 3 sigma, post-etch)	13	11	9	8	7	6	6	
Chip Size (mm^2)		*See*	*Table*	*24c*				
ASIC (SOC)								
Half Pitch	230	210	180	160	145	130	115	
Gate Length (nm, in resist)	180	165	150	130	120	110	100	
Gate Length (nm, post-etch)	180	165	150	130	120	110	100	
Contacts (nm, in resist)	230	210	180	160	145	130	115	
Gate CD Control (nm, 3 sigma, post-etch)	23	21	19	16	15	13	12	
Chip Size (mm^2)		*See*	*Table*	*24c*				
Development Capability								
Minimum Feature Size (nm)	100	85	70	60	55	50	45	
Minimum Field Size (mm)	22 x 22	22 x 22	22 x 22	22 x 22	22 x 22	22 x 22	22 x 22	
Minimum Field Area (mm^2)	484	484	484	484	484	484	484	
Depth of Focus (µm)	0.7	0.7	0.7	0.6	0.6	0.6	0.5	
Defect Density (defect/layer/m^2 @ nm)	80 @ 60	70 @ 50	65 @ 45	60 @ 40	56 @ 36	53 @ 33	50 @ 30	
Mask Size (mm, square optical/diameter non-optical)	152	152	152	152	152	152	152/200	
Wafer Size (mm, diameter)	200	200	300	300	300	300	300	

NOTE: ***The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists and masks for manufacturing must be available one (1) year earlier. Development capability must be available 2-3 years earlier.***

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

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Table 24b Long Term Lithography Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
DRAM				
Half Pitch (nm)	70	50	35	
Contacts (nm)	100	70	50	
Overlay (nm, mean + sigma)	25	20	15	
CD Control (nm, 3 sigma, post-etch)	7	5	4	
Chip Size (mm^2)	*See*	*Table*	*24d*	
MPU				
Half Pitch	80	55	40	
Gate Length (nm, in resist)	45	33	23	
Gate Length (nm, post-etch)	40	30	20	
Contacts (nm, in resist)	80	55	40	
Gate CD Control (nm, 3 sigma, post-etch)	4	3	2	
Chip Size (mm^2)	*See*	*Table*	*24d*	
ASIC (SOC)				
Half Pitch	80	55	40	
Gate Length (nm, in resist)	70	50	35	
Gate Length (nm, post-etch)	70	50	35	
Contacts (nm, in resist)	80	55	40	
Gate CD Control (nm, 3 sigma, post-etch)	7	5	4	
Chip Size (mm^2)	*See*	*Table*	*24d*	
Development Capability				
Minimum Feature Size (nm)	33	23	16	
Minimum Field Size (mm)	22 x 22	22 x 22	22 x 22	
Minimum Field Area (mm^2)	484	484	484	
Depth of Focus (µm)	0.5	0.5	0.5	
Defect Density (defect/layer/m^2 @ nm)	40 @ 20	30 @ 15	25 @ 10	
Mask Size (mm, square optical/diameter non-optical)	152/200	152/200	152/200	
Wafer Size (mm, diameter)	300	450	450	

NOTE: ***The dates in this table are the year of first product shipment of integrated circuits from a manufacturing site with volume exceeding 10,000 units. Exposure tools, resists and masks for manufacturing must be available one (1) year earlier. Development capability must be available 2-3 years earlier.***

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 24c Short Term Lithography Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Chip Size (mm^2)								
DRAM								
Sample	300	300	300	300	300	300	300	
Production	150	150	150	150	150	150	150	
Ramp	75	75	75	75	75	75	75	
Peak	38	38	38	38	38	38	38	
MPU Cost Performance								
Production	340	340	340	340	340	340	340	
Ramp	160	160	160	160	160	160	160	
Peak	75	75	75	75	75	75	75	
MPU Mid-Range Performance								
Ramp	195	195	195	195	195	195	195	
Peak	92	92	92	92	92	92	92	
MPU High Performance								
Ramp	440	440	440	440	440	440	440	
Peak	215	215	215	215	215	215	215	
ASIC/SOC								
Dependent on design, AISC/SOC will use up to the maximum field size available	484	484	484	484	484	484	484	

Solutions Exist | *Solutions Being Pursued* | *No Known Solutions*

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Table 24d Long Term Lithography Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	*2008 70 nm*	*2011 50 nm*	*2014 35 nm*	*DRIVER*
Chip Size (mm^2)				
DRAM				
Sample	**300**	**300**	**300**	
Production	**150**	**150**	**150**	
Ramp	**75**	**75**	**75**	
Peak	**38**	**38**	**38**	
MPU Cost Performance				
Production	**340**	**340**	**340**	
Ramp	**160**	**160**	**160**	
Peak	**75**	**75**	**75**	
MPU Mid-Range Performance				
Ramp	**195**	**195**	**195**	
Peak	**92**	**92**	**92**	
MPU High Performance				
Ramp	**440**	**440**	**440**	
Peak	**215**	**215**	**215**	
ASIC/SOC				
Dependent on design, AISC/SOC will use up to the maximum field size available	**484**	**484**	**484**	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

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Table 25a Short Term Resist Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
Resist meets lithography requirements for resolution and CD control (nm)	13	11	9	8	7	7	6	
Resist thickness (μm, imaging layer)*	0.54-0.72	0.50-0.66	0.45-0.60	0.39-0.52	0.36-0.48	0.33-0.44	0.3-0.4	
Ultra thin resist (μm)**	--	--	--	--	--	--	0.15	
Post-exposure bake sensitivity (nm/ºC)	5	4	4	3	3	2	2	
Backside particles (particles/m^2 @ critical size, nm)	3000 @ 200	3000 @ 200	2500 @ 200	2000 @ 200	2000 @ 200	2000 @ 200	2000 @ 100	
Resist film particles	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	
Other Requirements	- Need for positive or negative resist will depend on the critical feature density - Slope should be 90 +0-2 degrees - Thermal stability should be in the range of 130-150ºC - Etch selectivity should be comparable to or exceed polyhydroxystyrene (PHOST) - Strippability with no detectable residues - Airborne amine contamination ≤ 1000 pptM - Ionic/metal contaminants ≤ 5 ppb							

EXPOSURE DEPENDENT REQUIREMENTS

Exposure Technology	Sensitivity
248 nm	20-50 mJ/cm^2
193 nm	10-20 mJ/cm^2
157 nm	~ 10 mJ/cm^2
Extreme ultraviolet	10 mJ/cm^2
E-beam projection	5-10 μC/cm^2 @ 100 kV***
E-beam direct write	1-5 μC/cm^2 @ 50 kV***
Ion-beam projection	0.2-2.0 μC/cm^2

* *Resist thickness determined by aspect ratio range of 3:1 to 4:1.*

** *Lower limit for ultra thin resist (UTR) determined by opacity to exposure source.*

*** *Linked with resolution.*

Solutions Exist | *Solutions Being Pursued* | *No Known Solutions*

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Table 25b Long Term Resist Requirements

YEAR OF INTRODUCTION "TECHNOLOGY NODE"	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
Resist meets lithography requirements for resolution and CD control (nm)	4	3	2	
Resist thickness (μm, imaging layer)*	0.21-0.28	0.15-0.20	0.11-0.14	
Ultra thin resist (μm)**	0.10	0.07	0.07	
Post-exposure bake sensitivity (nm/ºC)	2	1	1	
Backside particles (particles/m^2 @ critical size, nm)	2000 @ 100	2000 @ 100	2000 @ 100	
Resist film particles	TBD	TBD	TBD	
Other Requirements	- Need for positive or negative resist will depend on the critical feature density - Slope should be 90 +0-2 degrees - Thermal stability should be in the range of 130-150ºC - Etch selectivity should be comparable to or exceed polyhydroxystyrene (PHOST) - Strippability with no detectable residues - Airborne amine contamination ≤ 1000 pptM - Ionic/metal contaminants ≤ 5 ppb			

EXPOSURE DEPENDENT REQUIREMENTS

Exposure technology	Sensitivity
248 nm	20-50 mJ/cm^2
193 nm	10-20 mJ/cm^2
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Extreme ultraviolet	10 mJ/cm^2
E-beam projection	5-10 μC/cm^2 @ 100 kV***
E-beam direct write	1-5 μC/cm^2 @ 50 kV***
Ion-beam projection	0.2-2.0 μC/cm^2

* *Resist thickness determined by aspect ratio range of 3:1 to 4:1.*

** *Lower limit for ultra thin resist (UTR) determined by opacity to exposure source.*

*** *Linked with resolution.*

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

Table 26a Short Term Mask Requirements

Year of Introduction "Technology Node"	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*		Driver
Wafer minimum Half Pitch (nm)	180	165	150	130	120	110	100		
Wafer minimum Isolated Line (nm, in resist)	140	120	100	90	80	70	65		
Wafer minimum Contact Hole (nm, in resist)	200	185	170	150	145	130	115		
							Opt	NGL	
Magnification	4	4	4	4	4	4	≥4	≥4	
Mask Minimum Image Size (nm)	560	480	400	360	320	280	260	260	
Mask OPC Feature Size (nm)	280	240	200	180	160	140	130	--	
Image Placement (nm, multi-point)	39	35	31	27	25	23	21	21	
CD Uniformity (nm, 3 sigma)									
Isolated lines (MPU gates)	16	14	12	10/20*	9/18*	8/16*	7/14*	10	
Dense lines (DRAM half pitch)	24	21	17	13/26*	12/24*	11/22*	10/20*	16	
Contact/vias	24	21	17	14	13	12	11	18	
Linearity (nm)	28	26	23	20	18	16	14		
CD Mean to Target (nm)	14	13	12	10	9	9	8		
Defect Size (nm)	144	132	120	104	96	88	80		
Data Volume (GB)	16	24	40	64	100	160	256		
Mask Design Grid (nm)	10	10	10	8	8	8	4		
Attenuated PSM Transmission Mean Deviation from Target (+/− % of target)	6	6	5	5	5	5	5	--	
Attenuated PSM Transmission Uniformity (+/− % of target)	4	4	4	4	4	4	4	--	
Attenuated PSM Phase Mean Deviation from 180° (+/− degree)	5	5	5	5	4	4	3	--	
Attenuated PSM Phase Uniformity (+/− degree)	2	2	2	2	2	2	2	--	
Alternating PSM Phase Mean Deviation from 180° (+/− degree)	--	--	--	2	2	2	2	--	
Alternating PSM Phase Uniformity (+/− degree)	--	--	--	2	2	2	2	--	

Mask Materials and Substrates (Exposure Tool Dependent)		
	Optical	- Absorber on fused silica, except for 157nm optical which will be absorber on modified fused silica square with pellicles - Primary PSM choices are attenuated shifter and alternating aperture
	X-Ray	- Refactory metal on Si Carbide Membrane (100 mm diameter) - "Pellicle" definition required
	E-Beam Projection	- Refractory metal scatterer on strutted SiN_x membrane (200 mm diameter) - "Pellicle" definition required
	EUV	- Absorber on multilayer reflector substrate (200 mm diameter) - "Pellicle" definition required
	Ion Projection	- Carbon coated silicon membrane stencil mask (200 mm diameter) - "Pellicle" definition required

Note: The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.

** This number applies to alternating PSM only. Delta between NGL & Opt is due to optical MEF at low k_1*

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

Table 26b Long Term Mask Requirements

Year of Introduction *"Technology Node"*	*2008* *70 nm*		*2011* *50 nm*	*2014* *35 nm*	*Driver*
Wafer minimum Half Pitch (nm)	70		50	35	
Wafer minimum Isolated Line (nm, in resist)	45		33	23	
Wafer minimum Contact Hole (nm, in resist)	80		55	40	
	Opt	NGL			
Magnification	≥4	≥4	≥4	≥4	
Mask Minimum Image Size (nm)	180	180	132	92	
Mask OPC Feature Size (nm)	90	--	--	--	
Image Placement (nm, multi-point)	15	15	12	9	
CD Uniformity (nm, 3 sigma)					
Isolated lines (MPU gates)	10*	7	5	3.3	
Dense lines (DRAM half pitch)	14*	11	8	5.6	
Contact/vias	8	12	9	6.4	
Linearity (nm)	10		7	5	
CD Mean to Target (nm)	6		5	4	
Defect Size (nm)	55		40	28	
Data Volume (GB)	1024		2048	8196	
Mask Design Grid (nm)	4		4	4	
Attenuated PSM Transmission Mean Deviation from Target (+/− % of target)	4	--	--	--	
Attenuated PSM Transmission Uniformity (+/− % of target)	4	--	--	--	
Attenuated PSM Phase Mean Deviation from 180° (+/− degree)	3	--	--	--	
Attenuated PSM Phase Uniformity (+/− degree)	2	--	--	--	
Alternating PSM Phase Mean Deviation from 180° (+/− degree)	1	--	--	--	
Alternating PSM Phase Uniformity (+/− degree)	1	--	--	--	

Mask Materials and Substrates (Exposure Tool Dependent)		
	Optical	- Absorber on fused silica, except for 157nm optical which will be absorber on modified fused silica square with pellicles - Primary PSM choices are attenuated shifter and alternating aperture
	X-Ray	- Refactory metal on Si Carbide Membrane (100 mm diameter) - "Pellicle" definition required
	E-Beam Projection	- Refractory metal scatterer on strutted SiN_x membrane (200 mm diameter) - "Pellicle" definition required
	EUV	- Absorber on multilayer reflector substrate (200 mm diameter) - "Pellicle" definition required
	Ion Projection	- Carbon coated silicon membrane stencil mask (200 mm diameter) - "Pellicle" definition required

Note: The requirements are for critical layers at defined year. Early volumes are assumed to be relatively small and difficult to produce.

** This number applies to alternating PSM only. Delta between NGL & Opt is due to optical MEF at low k_1*

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"Work-in-Progress"

** NOT FOR PUBLICATION**

Figure 18 Lithography Exposure Tool Potential Solutions

First Year of IC Production 1999 2002 2005 2008 2011 2014

Technology Options at Technology Nodes (DRAM Half Pitch, nm)

180
248nm

130
248nm + PSM
193nm

100
193nm + PSM
157nm
EPL
XRL
IPL
Narrow Options

70
157nm + PSM
EPL
EUV
IPL
XRL
EBDW
Narrow Options

50
EUV
EPL
IPL
EBDW
Narrow Options

35
EUV
IPL
EPL
EBDW
Innovative Technology
Narrow Options

DRAM Half Pitch (Dense Lines)

Research Required
Development Underway
Qualification Pre-Production

This legend indicated the time during which research, development, and qualification/pre-production should be taking place for the technology solution.

***Note:* Production level exposure tools should be available one year before first IC shipment.**

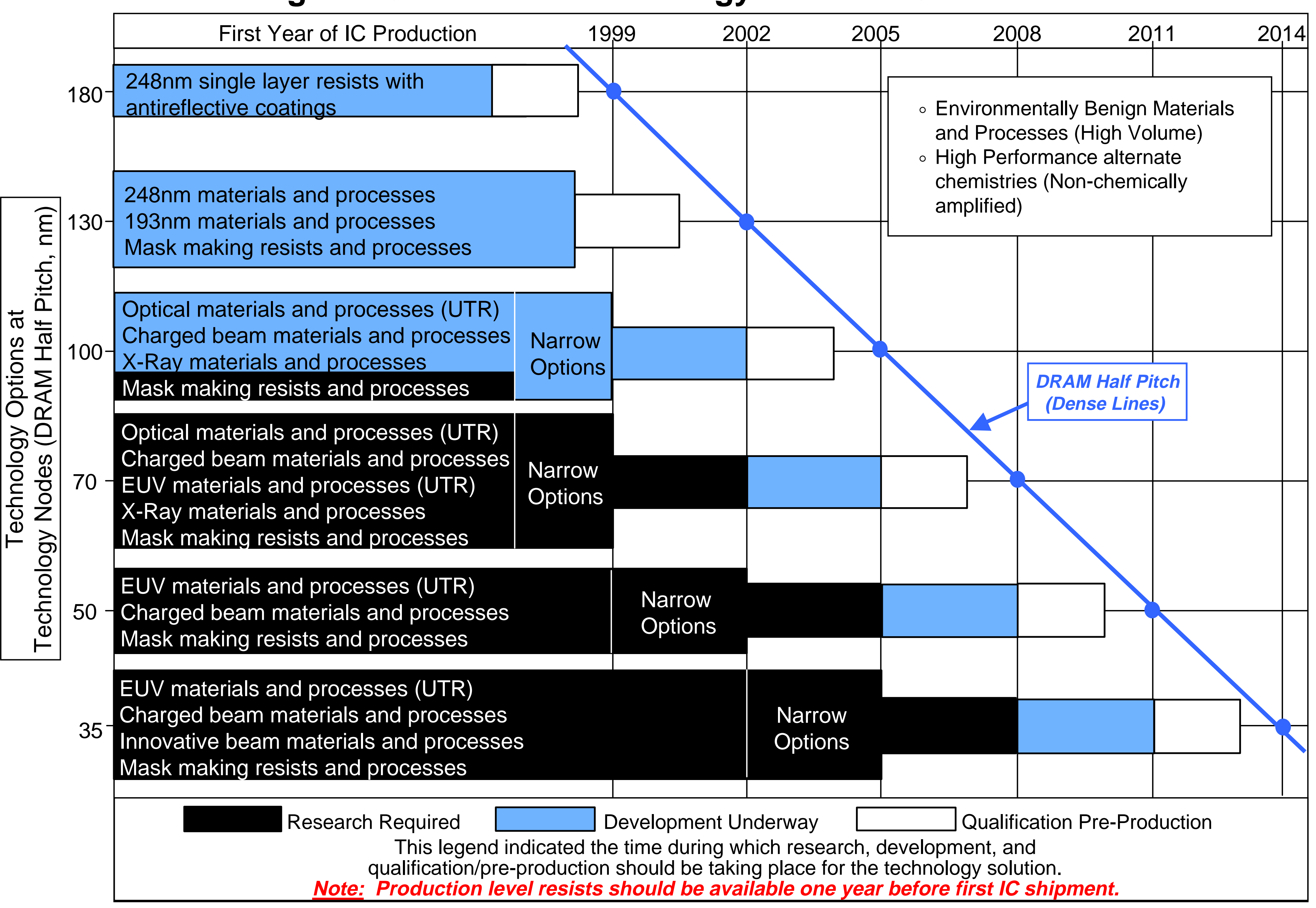
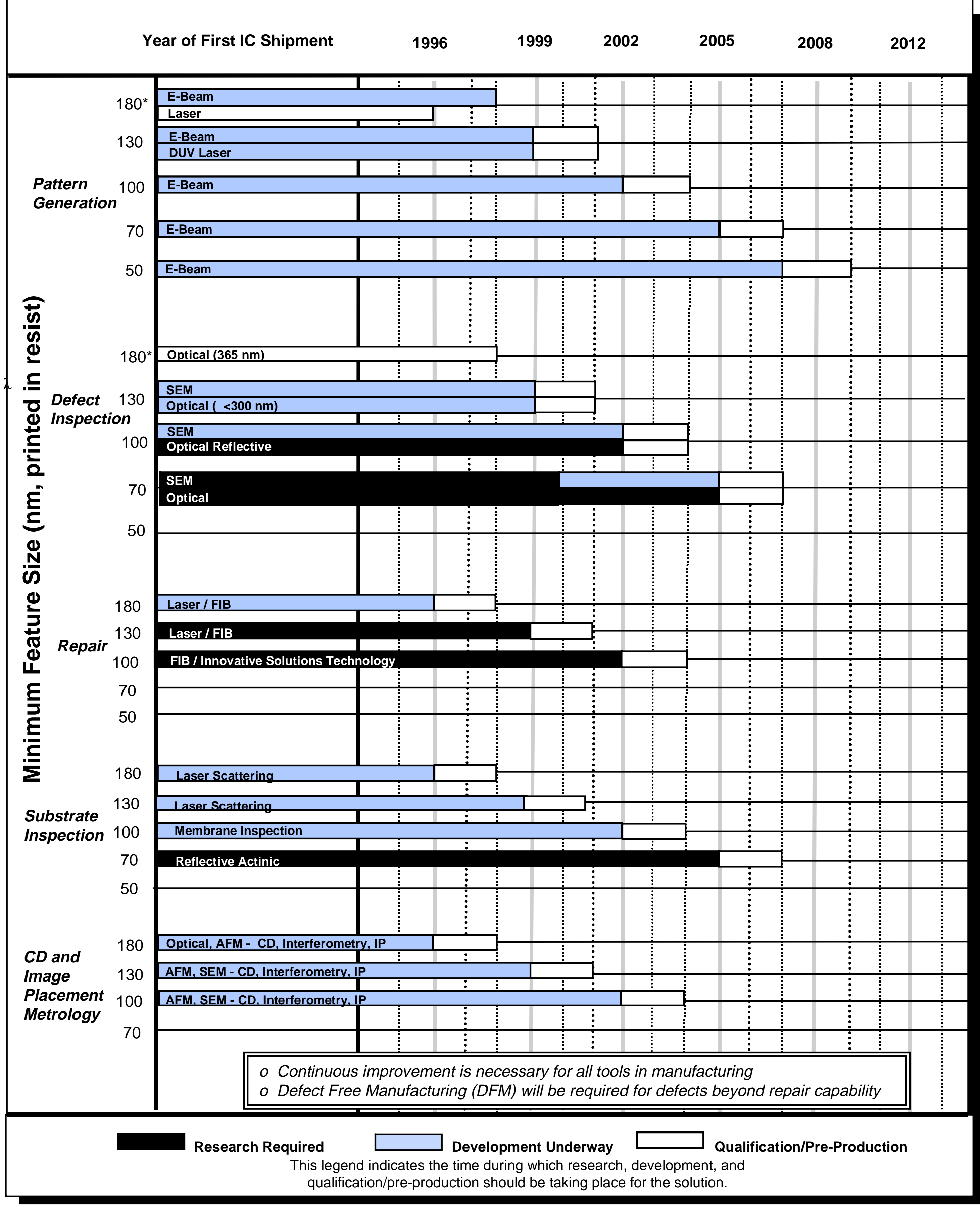


Figure 19 Resist Technology Potential Solutions
First Year of IC Production
1999
2002
2005
2008
2011
2014
Technology Options at Technology Nodes (DRAM Half Pitch, nm)
180
130
100
70
50
35
248nm single layer resists with antireflective coatings
248nm materials and processes
193nm materials and processes
Mask making resists and processes
Optical materials and processes (UTR)
Charged beam materials and processes
X-Ray materials and processes
Mask making resists and processes
Narrow Options
Optical materials and processes (UTR)
Charged beam materials and processes
EUV materials and processes (UTR)
X-Ray materials and processes
Mask making resists and processes
Narrow Options
EUV materials and processes (UTR)
Charged beam materials and processes
Mask making resists and processes
Narrow Options
EUV materials and processes (UTR)
Charged beam materials and processes
Innovative beam materials and processes
Mask making resists and processes
Narrow Options
Environmentally Benign Materials and Processes (High Volume)
High Performance alternate chemistries (Non-chemically amplified)
DRAM Half Pitch (Dense Lines)
Research Required
Development Underway
Qualification Pre-Production
This legend indicated the time during which research, development, and qualification/pre-production should be taking place for the technology solution.
Note: Production level resists should be available one year before first IC shipment.

1999 Roadmap Update -- 1/7/99 Kickoff



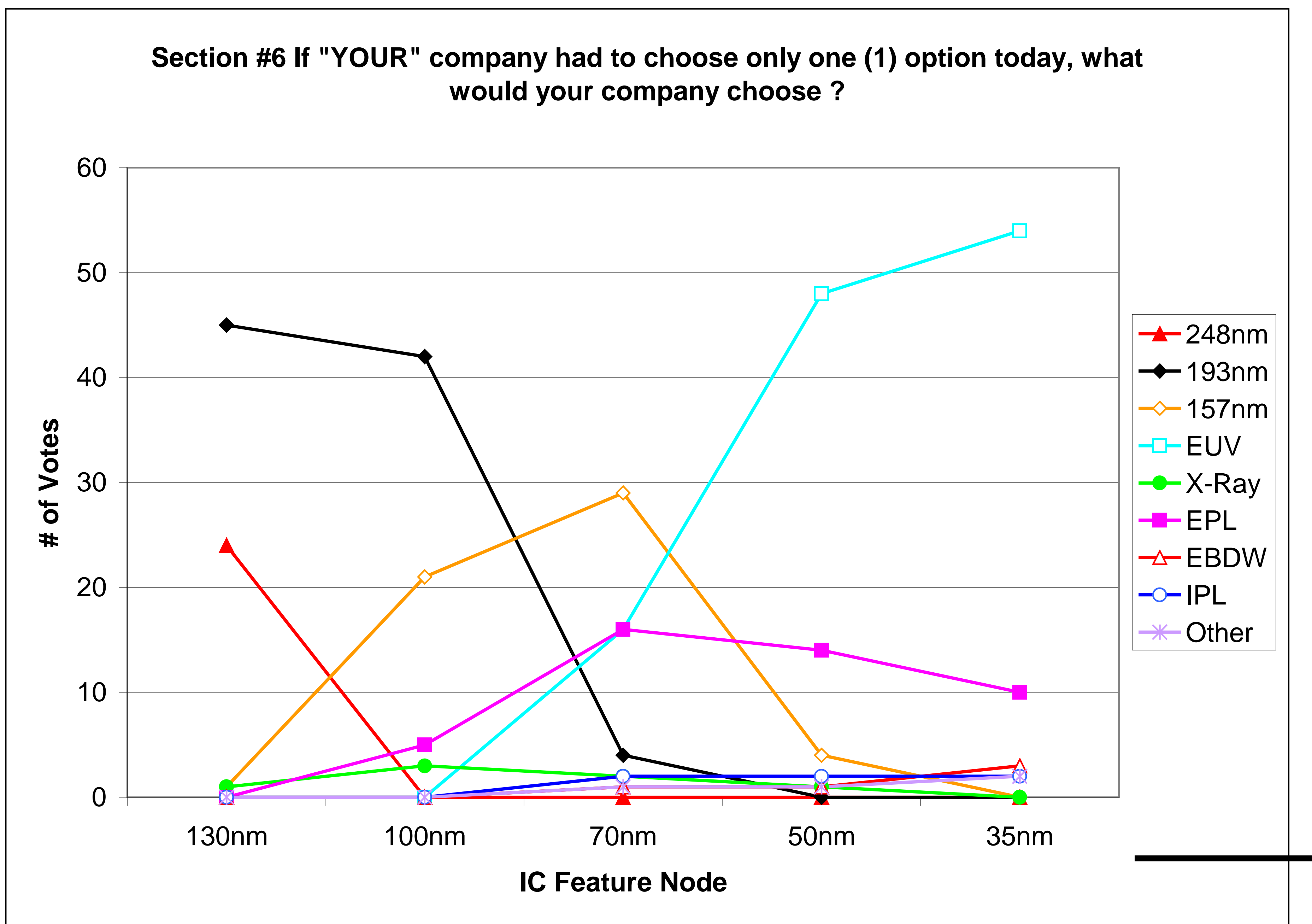
SEM - scanning electron microscope
FIB - focused ion beam

AFM - atomic force microscopy
IP - image placement

Work in Progress Draft: Not for Publication

LITHOGRAPHY - FIGURE 20 CRITICAL LEVEL MASK TECHNOLOGY POTENTIAL SOLUTIONS

Advanced Lithography Critical Review, June 9, 1999, Chicago, IL



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Lithography ITWG Report

Summary

- New format adopted to focus on unique requirements for DRAM, MPU, ASIC and optical masks.
- Roadmap timing is biggest challenge / issue for lithography.

  IRC decision reached on 7/7/99!

  - Mask capability is key limiter to progress.
- Chip size proposal affords significant relief for lithography tools and masks.

  Need industry feedback, IRC adoption!
- Optical lithography extends domain with 157nm technology. NGL options moved to 100nm node and below.
- Cost control and ROI are major concerns for acceleration at 100nm-50nm nodes (single node solutions).

Work in Progress --- Not for Publication