

100 nm High End Microprocessor

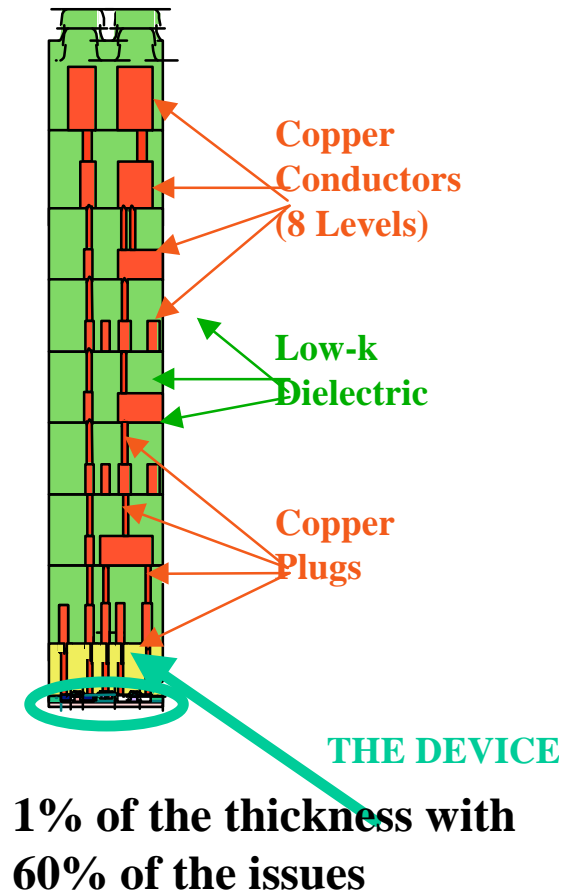
July 8-9 ITRS Conference

FEP TWG Report

Co-Chairs

Rinn Cleavelin, TI

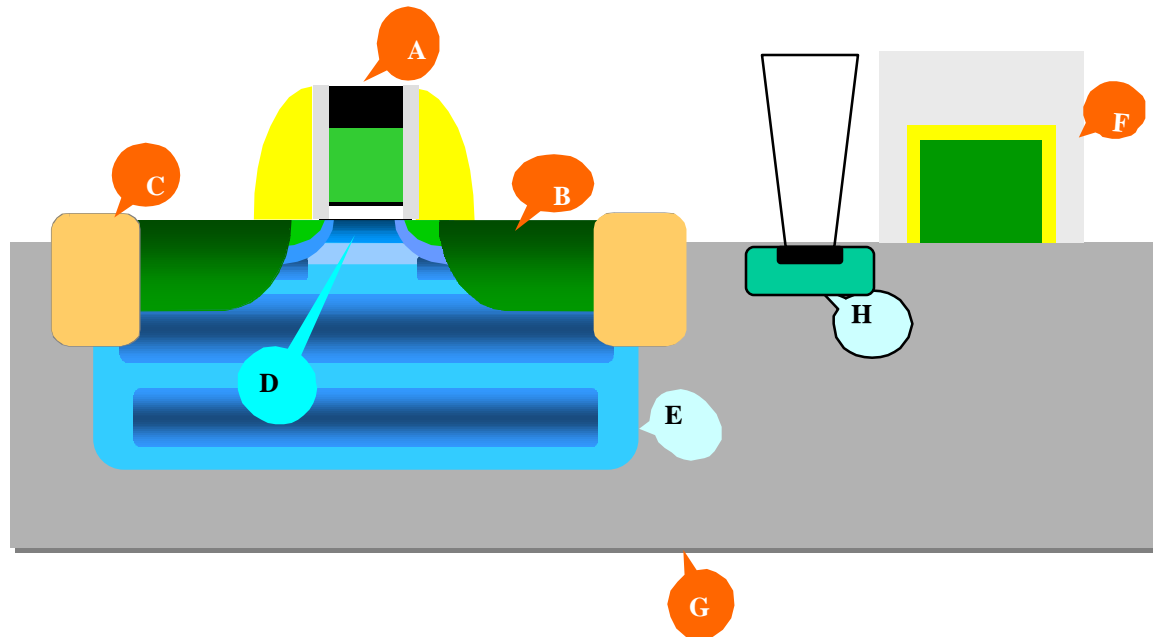
Walter Class, Eaton



Scope of FEP TWG Activities

- Focus on requirements for high performance transistors & storage capacitors for memory and logic products
- Intent is to define comprehensive, integrated solutions needs for the key technology areas in the front-end-of-line (FEOL) wafer fabrication processing of integrated circuits
- Covers starting silicon wafer through contact silicidation processes

FEP Roadmap Scope



A: Gate Stack B: Source/Drain - Extension
C: Isolation D: Channel
E: Wells F: Capacitor Stack/Trench
G: Starting Material H: Contacts

Thrusts & Sub-TWG Organization

- Starting Materials
- Surface Preparation
- Etch
- Doping
- Thermal/Thin Films
- Device Modeling

Sub-TWG Tasks

- **Using an evolutionary approach, address the following issues:**
 - **Establish evolutionary technical requirements through model-based or physical-based extrapolation**
 - **Identify where barriers exist to evolutionary technology extensions**
 - **Identify if work is ongoing to address these barriers (color code yellow)**
 - **Identify if there is no known solution to these barriers (color code red)**
 - **Identify those known potential solutions which are in R&D or pilot production**
 - **Prepare roadmap documentation**
 - **Collaborate with other sub-TWG's re selection of FEP Difficult Challenges**

Sub-TWGW Roadmap Documentation

- **Color-coded Technical Requirements Tables**
 - Yellow means barriers exist but are being addressed in R&D
 - Red means barriers exist and no known solutions have been identified
- **Color-coded Potential Solutions Figures**
 - Black identifies research is required
 - Blue identifies development is underway
 - White identifies work is in pre-production
- **Table of Important Challenges**
- **Text**
- **Inputs to FEP Difficult Challenges**

TWG Membership Affiliations

- Universities
- Government Agencies
- Semiconductor Manufacturers
- Semiconductor Equipment Manufacturers
- Materials Suppliers
- Consultants

International FEP Inputs

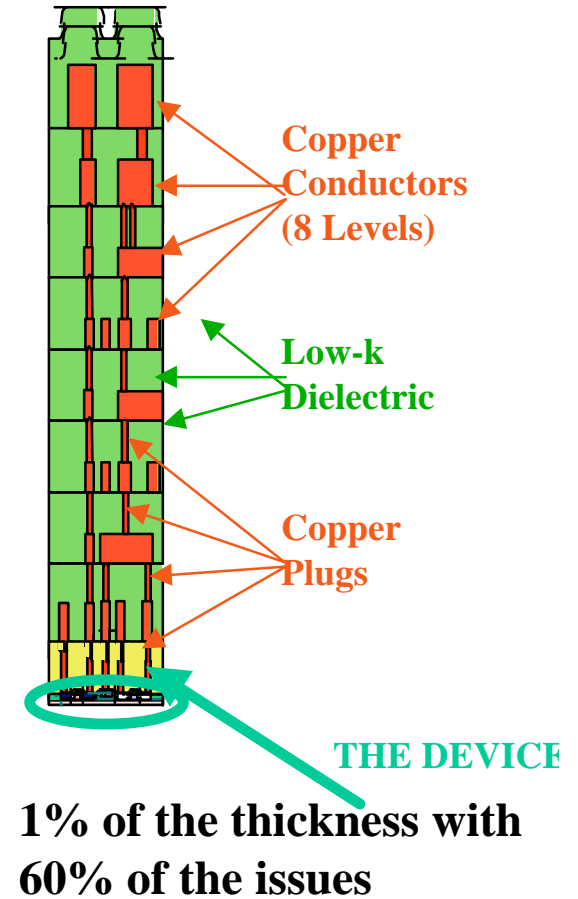
- **Japan FEP TWG-Table 22B Stacked Capacitor**
 - Seiichiro Kawamura, Fujitsu, e-mail: rhd01125@niftyseve.or.jp
 - Masaaki Niwa, Matsushita
- **Europe FEP TWG-Table 22B Trench Capacitor**
 - Bernd Vollmer, Infineon
 - Rene Penning de Vries, Phillips
- **Taiwan FEP TWG-Chip size inputs**
 - H. H. Tsai , Winbond Electronics
- **In addition to Table 22B, International TWG's provided general input/commentary to all tables and figures prepared by US Domestic TWG's**

Where do I send comments/criticism, letters of outrage?

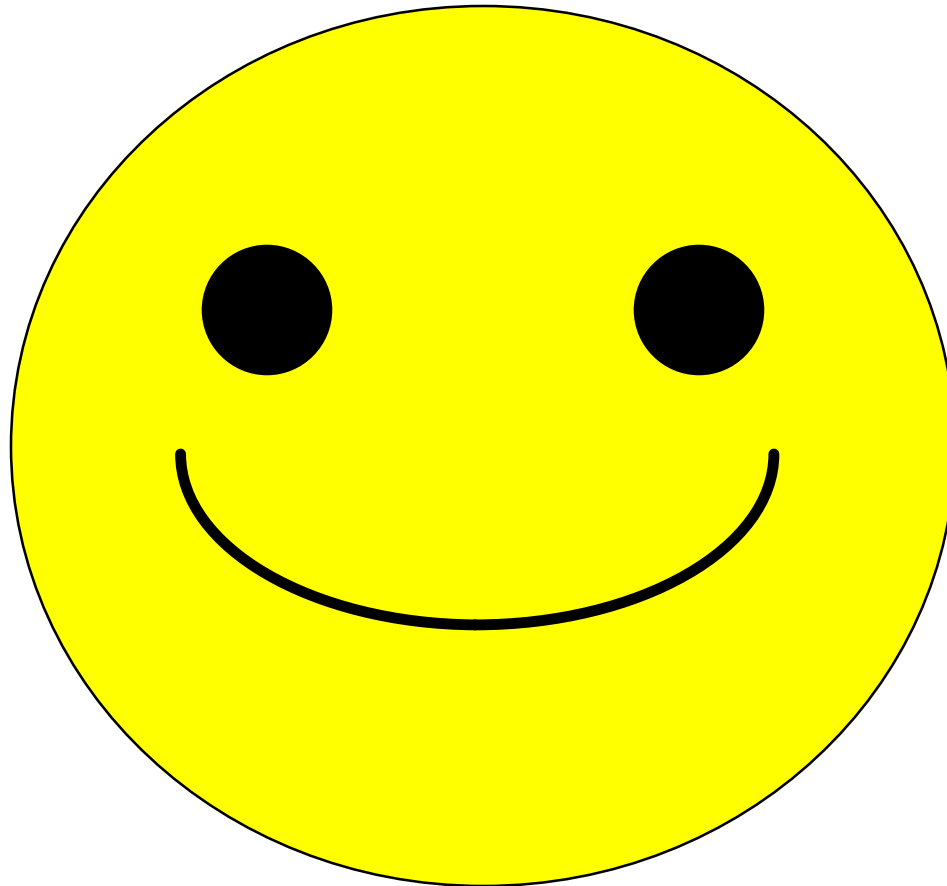
- **TWG Co Chairs:** Rinn Cleavelin- rinn.cleavelin@sematech.org
Walter Class- wclass@bev.etn.com
- **Starting Materials:** Howard Huff- howard.huff@sematech.org
Randy Goodall- randy.goodall@intl.sematech.org
- **Surface Prep:** Bob Kunesh- r-kunesh@ti.com
Scott Becker- sbecker@fsi-intl.com
- **Etch:** Pak Leung- pak.leung@sematech.org
Pat Martin- cptu@ti.com
- **Doping:** Larry Larson- larry.larson@sematech.org
Kevin Jones- kjones@mse.ufl.edu
- **Thermal/Films:** Carl Osburn- osburn@eos.ncsu.edu
Mike Pas- pas@spdc.ti.com

The View from 10,000 Feet

100 nm High End Microprocessor



MOS Transistor Scaling in the 1990's



MOS Transistor Scaling 2000-2008



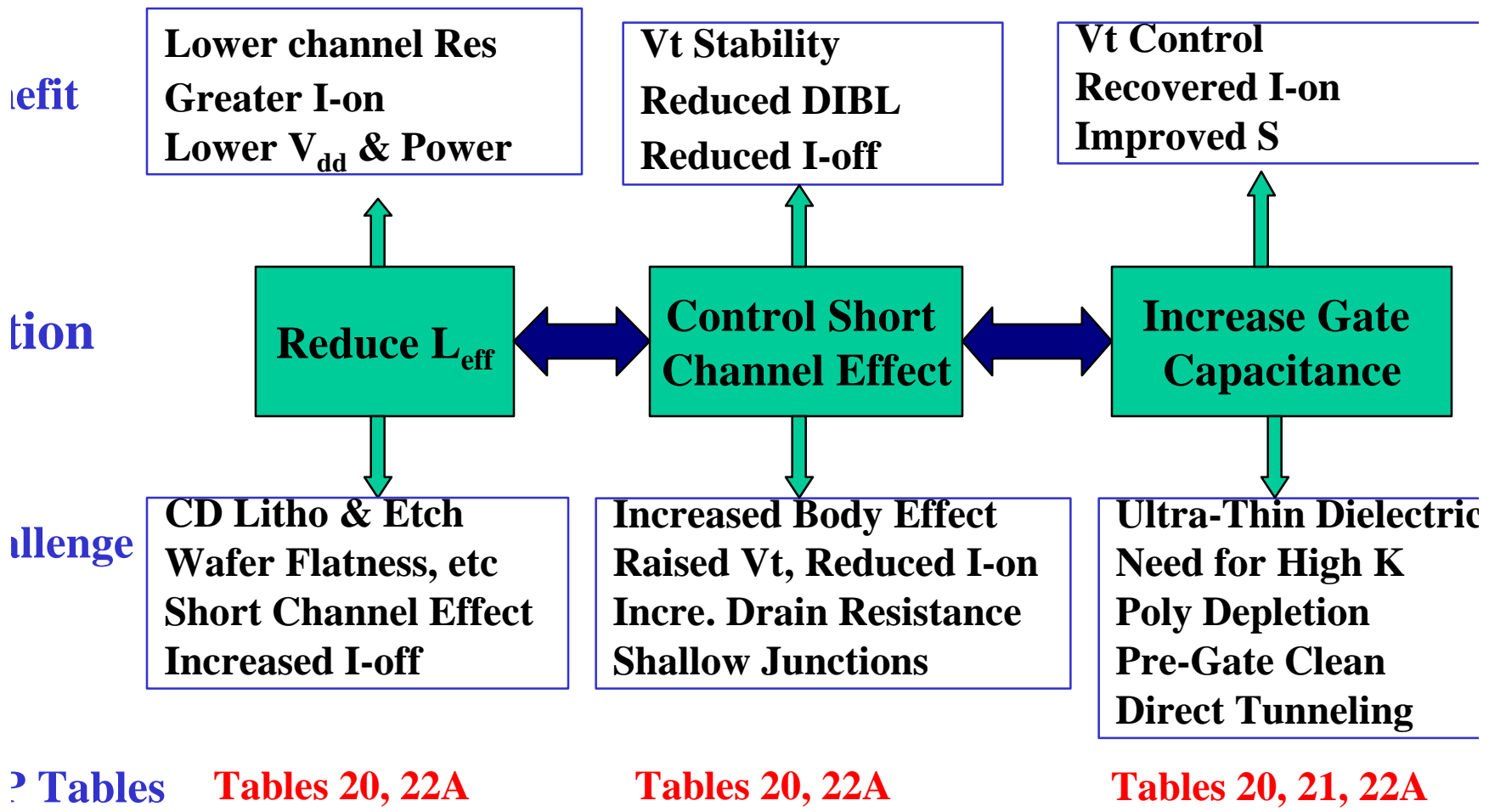
HELP!!!
(read \$\$\$)

MOS Transistor Scaling >2008



Invention Needed: new device architectures!!

Scaling & Relationship w/FEP Tables



<i>Table 20 1999 Short Term Starting Materials Technology Requirements</i>								
<i>Year of First Product Shipment Technology Node</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>	<i>Driver</i>
<i>DRAM 1/2 Pitch (nm)</i>	180	165	150	130	120	110	100	D ½
<i>MPU Gate Length (nm)</i>	140	120	100	85	80	70	65	M
<i>General Characteristics * (A,B)</i>								
Wafer diameter (mm) **	200	300 ***	300	300	300	300	300	
Edge exclusion (mm)	2	1	1	1	1	1	1	
Front surface particle size (nm), latex sphere equivalent (C)	³ 90	³ 82.5	³ 75	³ 65	³ 60	³ 55	³ 50	
Particles (cm ⁻²) (D)	£0.13	£0.12	£0.12	£0.14	£0.13	£0.12	£0.10	D ½, M
Particles (#/wf)	£38	£84	£80	£95	£89	£84	£72	D ½, M
Critical surface metals (at/cm ²) (E)	£1 x 10¹⁰	£9 x 10⁹	£8 x 10⁹	£6 x 10⁹	£5 x 10⁹	£4 x 10⁹	£4 x 10⁹	D ½, M
Site flatness (nm) (F)	£180	£165	£150	£130	£120	£110	£100	
Oxygen (center point value ± 2.0 ppma) (ASTM '79) (G)	19-31	18-31	18-31	18-31	18-31	18-31	18-31	

Table 20 1999 Short Term Starting Materials Technology Requirements

<i>Year of First Product Shipment Technology Node</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>	<i>Driver</i>
<i>DRAM 1/2 Pitch (nm)</i>	180	165	150	130	120	110	100	D ½
<i>MPU Gate Length (nm)</i>	140	120	100	85	80	70	65	M

shed Wafer * (A,B)

Total Allowable Front Surface Light Scattering Defect Density is The Sum of Crystal Originated Pits (COPs) and Particles (see General Characteristics)

surface COPs size (nm), latex sphere equivalent (C)	³ 90	³ 82.5	³ 75	³ 65	³ 60	³ 55	³ 50	
OPs (cm ⁻²) (H)	£ 0.13	£ 0.12	£ 0.12	£ 0.14	£ 0.13	£ 0.12	£ 0.10	D ½, M
OPs (#/wf)	£ 38	£ 84	£ 80	£ 95	£ 89	£ 84	£ 72	D ½, M
surface particle size, latex sphere equivalent (I)	³ 500	³ 450	³ 400	³ 333	³ 300	³ 267	³ 233	D ½
particles (#/cm ²) (D)	£ 0.13	£ 0.12	£ 0.12	£ 0.14	£ 0.13	£ 0.12	£ 0.10	D ½, M
particles (#/wf)	£ 38	£ 84	£ 80	£ 95	£ 89	£ 84	£ 72	D ½, M
bulk Fe (at/cm ³) (J)	£ 1 x 10 ¹⁰	< 1 x 10 ¹⁰	< 1 x 10 ¹⁰	< 1 x 10 ¹⁰	< 1 x 10 ¹⁰	< 1 x 10 ¹⁰	< 1 x 10 ¹⁰	D ½, M
dislocation stacking faults (OSF) (DRAM) (cm ⁻²)	£ 4.4	£ 3.9	£ 3.4	£ 2.8	£ 2.5	£ 2.2	£ 1.9	D ½
dislocation stacking faults (OSF) (MPU) (cm ⁻²) (K)	£ 3.1	£ 2.5	£ 1.9	£ 1.5	£ 1.4	£ 1.1	£ 1.0	M
combination lifetime (µs) (L) (M)	³ 305	³ 350	³ 350	³ 350	³ 350	³ 350	³ 350	

Table 20 1999 Short Term Starting Materials Technology Requirements

<i>Year of First Product Shipment Technology Node</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>	<i>Driver</i>
<i>DRAM 1/2 Pitch (nm)</i>	180	165	150	130	120	110	100	D½
<i>MPU Gate Length (nm)</i>	140	120	100	85	80	70	65	M

axial Wafer * (A,B)

total Allowable Front Surface Defect Density is The Sum of Epitaxial Large Area Defects, Epitaxial Stacking Faults and Particles (see General Characteristics) (N)

num layer thickness (DRAM) (µm) (± % nce) (O)	3 (± 4%)	2 (± 4%)	2 (± 3%)	2 (± 3%)	2 (± 3%)	2 (± 3%)	2 (± 3%)	2 (± 3%)	D½
num layer thickness (MPU) (µm) (± % nce) (O)	2 (± 4%)	2 (± 4%)	1 (± 3%)	1 (± 3%)	1 (± 3%)	1 (± 3%)	1 (± 3%)	1 (± 3%)	M
large area defects (DRAM) (cm ⁻²) (P)	£ 0.007	£ 0.007	£ 0.007	£ 0.007	£ 0.007	£ 0.007	£ 0.007	£ 0.007	D½
large area defects (DRAM) (#/wf)	£ 2.02	£ 4.67	£ 4.67	£ 4.67	£ 4.67	£ 4.67	£ 4.67	£ 4.67	D½
large area defects (MPU) (cm ⁻²) (P)	£ 0.006	£ 0.006	£ 0.006	£ 0.006	£ 0.006	£ 0.006	£ 0.006	£ 0.006	M
large area defects (MPU) (#/wf)	£ 1.78	£ 4.12	£ 4.12	£ 4.12	£ 4.12	£ 4.12	£ 4.12	£ 4.12	M
stacking faults (DRAM) (cm ⁻²) (Q)	£ 0.013	£ 0.013	£ 0.013	£ 0.013	£ 0.013	£ 0.013	£ 0.013	£ 0.013	D½
stacking faults (DRAM) (#/wf)	£ 4.04	£ 9.35	£ 9.35	£ 9.35	£ 9.35	£ 9.35	£ 9.35	£ 9.35	D½
stacking faults (MPU) (cm ⁻²) (Q)	£ 0.012	£ 0.012	£ 0.012	£ 0.012	£ 0.012	£ 0.012	£ 0.012	£ 0.012	M
stacking faults (MPU) (#/wf)	£ 3.57	£ 8.25	£ 8.25	£ 8.25	£ 8.25	£ 8.25	£ 8.25	£ 8.25	M

<i>Table 20 1999 Short Term Starting Materials Technology Requirements</i>								
<i>Year of First Product Shipment Technology Node</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>	<i>Driver</i>
<i>DRAM 1/2 Pitch (nm)</i>	180	165	150	130	120	110	100	D ½
<i>MPU Gate Length (nm)</i>	140	120	100	85	80	70	65	M
<i>Silicon-On-Insulator Wafer* (A,B)</i>								
<i>Silicon final device layer thickness (tolerance ± 5%) nm) (R)</i>	50 - 200	50 - 200	50 - 200	50 - 200	50 - 200	50 - 100	50 - 100	M
<i>Buried oxide (BOX) thickness (tolerance ± 5%) nm) (S)</i>	£ 200	£ 200	£ 200	£ 200	£ 200	£ 100	£ 100	M
<i>λ_{BOX}, BOX defects (MPU) (cm⁻²) (T)</i>	£ 0.359	£ 0.346	£ 0.352	£ 0.344	£ 0.275	£ 0.254	£ 0.208	M
<i>λ_{INC}, inclusions (MPU) (cm⁻²) (U)</i>	£ 0.431	£ 0.415	£ 0.422	£ 0.413	£ 0.330	£ 0.305	£ 0.250	M
<i>λ_{TD}, threading dislocations (MPU) (cm⁻²) (V)</i>	£ 2 x 10⁶	£ 2 x 10⁶	£ 2 x 10⁶	£ 2 x 10⁶	£ 2 x 10⁶	£ 2 x 10⁶	£ 2 x 10⁶	D ½, M

Table 21 1999 Short Term Surface Preparation Technology Requirements

<i>Year of Introduction</i>	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Drive
End of Line (A)								
Min critical area (cm ²) (B)	0.32			0.68			1.6	D 1/2
Max critical area (cm ²) (C)	0.1		0.13			0.19		M
Min GOI D ₀ (cm ²) (D)	0.03			0.015			0.006	
Max GOI D ₀ (cm ²) (D)	0.1		0.08			0.05		
Defect scatterers, front side (E)								
RAM (cm ²)	0.064	0.06	0.058	0.068	0.064	0.06	0.051	D 1/2
Logic (cm ²)	0.064	0.06	0.058	0.068	0.064	0.06	0.051	M
Particle size (nm)	90	82.5	75	65	60	55	50	
Defect scatterers, back side (cm ²)	6.4E-02	6.0E-02	5.8E-02	6.8E-02	6.4E-02	6.0E-02	5.1E-02	
Particle size (nm) (F)	500	450	400	333	300	267	233	
Cal metals (G)	9.8E+09		7.3E+09	5.3E+09			3.00E+09	
Tr metals (atoms/cm ²) (H)	2.50E+10			1.50E+10			1.00E+10	
Al ions (atoms/cm ²) (I)	3.50E+10			3.00E+10			3.5E+10	
Metals/polymers (C atoms/cm ²) (J)	7.3E+13	6.6E+13	6.0E+13	5.3E+13	4.9E+13	4.5E+13	4.1E+13	
Ice Oxygen (O atoms/cm ²) (K)	<1E+14	<1E+14	<1E+14	<1E+14	<1E+14	<1E+14	<1E+12	
Surface Roughness (nm) (L)	0.15			0.12			0.1	
Min Water Marks (/cm ²) (M)	6.70E-03			4.69E-03			3.28E-03	
Max Water Marks (/cm ²) (M)	5.91E-03			4.14E-03			2.90E-03	
End of Line (N)								
Defects (cm ²) (O)	0.15			0.1			0.06	
Particle size (nm)	90	82.5	75	65	60	55	50	
Etch Resistance (P)	>10 years	>10 years	>10 years	>10 years	>10 years	>10 years	>10 years	
Ice Oxygen (O atoms/cm ²) (K)	7.0E+13			5.0E+13			3.5E+13	

Table 22a Thermal/Thin Films, Gate Etch, and Doping Technology Requirements for Logic
SHORT TERM YEARS

Year of Introduction "Technology Node"	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Drive
Isolated Line (nm)	140	120	100	85	80	70	65	<i>M Gate</i>
Equivalent physical Oxide Thickness T_{ox} (nm) (A)	1.9-2.5	1.8-2.3	1.6-2.0	1.3-1.7	1.2-1.6	1.0-1.4	0.9-1.1	<i>M Gate</i>
Gate Dielectric Leakage (A/cm^2) High Performance (B)	3	5	8	11	16	22	30	<i>M Gate</i>
Gate Dielectric Leakage (A/cm^2) Low Power (B)	3.E-03	5.E-03	8.E-03	1.E-02	1.5E-02	2.E-02	3.E-02	<i>M Gate</i>
Thickness control EOT (% 3σ) (C)	< \pm 4	< \pm 4	< \pm 4	< \pm 4	< \pm 4	< \pm 4	< \pm 4	<i>M Gate</i>
Effective Control	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	<i>M Gate</i>
Sidewall Spacer								
Sidewall spacer thickness (nm) Extension Structure (D)	72-144	65-130	59-108	52-104	48-96	44-88	40-80	<i>M Gate</i>
Sidewall spacer thickness (nm) Elevated Contact (E)							20-40	<i>M Gate</i>
Sidewall spacer thickness (nm) Single Drain (F)								<i>M Gate</i>
Sidewall spacer thickness control (nm, 3σ)	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	<i>M Gate</i>
Gate Electrode								
Gate electrode sheet Rs (Wsq) (G)	4-6	4-6	4-6	4-6	4-6	4-6	4-6	<i>M Gate</i>
Gate electrode thickness (H)	140	120	100	85	80	70	65	<i>M Gate</i>
Gate electrode Resistivity ($\mu\Omega$ -cm) (I)	72	65	54	54	48	44	40	<i>M Gate</i>
Gate Depletion Effect (% of EOT)	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	£ 10%	<i>M Gate</i>
Doping (active) @ oxide interface	2.30E+20	2.60E+20	2.80E+20	4.00E+20	4.60E+20	5.00E+20	7.0E+20	<i>M Gate</i>
Silicide thickness (nm) (J)	55	45	40	34	32	28	25	<i>M Gate</i>

Table 22a Thermal/Thin Films, Gate Etch, and Doping Technology Requirements for Logic
SHORT TERM YEARS

Year of Introduction "Technology Node"	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
<i>Isolated Line (nm)</i>	140	120	100	85	80	70	65	<i>MGate</i>
/D Contact & S/D Extension								
Contact silicide sheet Rs (Ω/sq) (K)	2.7	3.3	3.8	4.4	4.7	5.4	6.0	<i>MGate</i>
Contact maximum resistivity ($\Omega\text{-cm}^2$) (L)	$< 3.0 \times 10^{-7}$	$< 2.5 \times 10^{-7}$	$< 2.0 \times 10^{-7}$	$< 1.7 \times 10^{-7}$	$< 1.6 \times 10^{-7}$	$< 1.1 \times 10^{-7}$	$< 1.0 \times 10^{-7}$	<i>MGate</i>
Maximum Silicon consumption (nm) (M)	36-70	32-60	26-50	22-43	20-40	18-36	16-33	<i>MGate</i>
Contact Xj (nm) (N)	75-145	65-125	55-105	45-90	43-85	38-75	35-70	<i>MGate</i>
Drain extension Xj (nm) (O)	42-70	36-60	30-50	25-43	24-40	20-35	20-33	<i>MGate</i>
Drain Extension Sheet Resistance (Ω/sq)	350-800	310-760	280-730	250-700	240-675	220-650	200-625	<i>MGate</i>
Lateral Abruptness for Source Extension (nm/Decade)	5			2.9			2	<i>MGate</i>
Extension Lateral Abruptness (nm/decade) (P)	14	12	10	8.5	8	7	6.5	<i>MGate</i>
Channel								
Potential: Dopant Variation- Position (nm)	15	10	10	2-10	<8	<8	1-7	<i>MGate</i>
Potential: Dopant Variation - Dose	<10% (Halo)	<10% (Halo)	<9% (Halo)	<8%	<7%	<6%	<5%	<i>MGate</i>
Channel conc. for Wdepletion $< 1/4L_{\text{eff}}$ (cm^{-3}) (Q)	2.0×10^{18}			3.0×10^{10}			4.0×10^{10}	<i>MGate</i>
Unif. channel conc. (cm^{-3}), for $V_t=0.4$ (R)	$6\text{-}10 \times 10^{17}$			$1\text{-}2 \times 10^{10}$			$2\text{-}3 \times 10^{10}$	<i>MGate</i>
Retrograde Channel Depth								<i>MGate</i>

Table 22a Thermal/Thin Films, Gate Etch, and Doping Technology Requirements for Logic
SHORT TERM YEARS

Year of Introduction "Technology Node"	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	Driver
<i>Isolated Line (nm)</i>	140	120	100	85	80	70	65	<i>MGate</i>
Minimum Dimension Etch								
Minimum measurable gate dielectric remaining (post gate clean)	>0	>0	>0	>0	>0	>0	>0	<i>MGate</i>
±3σ Variation (nm) (Dense and Isolated lines) (S)	£10%	£10%	£10%	£10%	£10%	£10%	£10%	<i>MGate</i>
Logic (nm)	14	12	10	8.5	8	7	6.5	<i>MGate</i>
± bias between dense and isolated lines (T)	£15%	£15%	£15%	£15%	£15%	£15%	£15%	<i>MGate</i>

TABLE 2.2.2. DRAM Technology Node Roadmap (continued)

Year of First Product Shipment	1999	2002	2005	2008	2011	2014
Technology Node	180 nm	130 nm	100 nm	70 nm	50 nm	35 nm
DRAM Generation (A)	1G	4G	16G	64G	256G	1T
Cell area factor a (B)	10.0	8.0	8.0	7.0	7.0	6.0
Cell area [um ²] (C)	0.32 =0.36*0.9	0.14 =0.26*0.52	0.080 =0.2*0.4	0.034 =0.14*0.25	0.018 =0.1*0.18	0.007 =0.07*0.1
Storage Node area [um ²] (D)	0.130 =0.18*0.72	0.051 =0.13*0.39	0.030 =0.1*0.3	0.012 =0.07*0.18	0.006 =0.05*0.13	0.002 =0.035*0.06
capacitor structure	Cylinder MS Ta ₂ O ₅	Cylinder MM Ta ₂ O ₅	STD-STACK MM BST	STD-STACK MM epi-BST	STD-STACK MM epi-BST	STD-STACK MM ???
dielectric constant	22	50	250	700	800	1500
SN Height H [um]	0.70	0.37	0.35	0.20	0.18	0.12
cylinder factor (E)	1.5	1.5	1.0	1.0	1.0	1.0
total Capa area [um ²]	2.08	0.65	0.31	0.11	0.07	0.028
Structural Coefficient (F)	6.4	4.8	3.9	3.2	4.0	3.8
teq@25fF [nm] (G)	2.9	0.90	0.43	0.15	0.10	0.04
t phy.@25fF [nm] (H)	10.6	11.6	27.4	27.3	19.6	14.7
A/R of SN (OUT) for cell plate depo. (I)	4.4	3.5	7.8	13.0	16.7	21.3
HAC diameter [um] (J)	0.22	0.16	0.12	0.08	0.06	0.04
l Interlevel insulator and metal thickness except SN [um] (K)	1.10	0.99	0.89	0.80	0.72	0.65
HAC depth [um] (L)	1.80	1.36	1.24	1.00	0.90	0.77
HAC A/R	8.3	8.7	10.3	11.9	15.0	18.3
Vdd [V] (M)	1.8	1.5	1.2	0.9	0.6	0.5
Retention Time [ms] (N)	128	256	512	1024	2048	4096
Leak Current [fA/cell] (O)	0.527	0.220	0.088	0.033	0.011	0.005
Leak Current Density (A/cm ²)	2.5E-08	3.4E-08	2.8E-08	3.0E-08	1.6E-08	1.7E-08
Process Temperature [°C]	~ 500	~ 500	< 500	< 500	< 500	< 500
Anneal Temperature [°C]	~ 800	~ 750	< 750	~ 650	< 650	< 650
DRAM Gox [nm] (P)	6	5	4	3	2	1.5
Cgate [F/cell] (Q)	1.9E-16	1.2E-16	8.6E-17	5.6E-17	4.3E-17	2.8E-17
Word line Rs [ohm/sq.] (R)	10	8.3	6.7	5.0	3.3	2.5
Cbitline (S)	1	0.79	0.62	0.49	0.39	0.30
Bit line Rs [ohm/sq.] (T)	10	5.3	4.0	2.2	1.4	0.7

FEP Difficult Challenges before 2005

- Gate Stack with Ultra-Thin Nitride and/or Mid-K dielectric by year 2004
- Stack/Trench DRAM Storage Cell Scaling
- Ultra-shallow Junctions w/Standard Processing
- L_{eff} CD Control
- Metrology

FEP Difficult Challenges Beyond 2005

- Dual Metal High-K gate stack with L_{eff} CD Control
- Memory Storage Cell
- Alternate & Ultra-Scaled Transistor Structures
- Silicon Compatible Materials, including wafers
- Metrology

The FEP Grand Challenge

**CMOS Compatible, Robust, High-
K Dielectric Gate Stack Process**

High-K Gate Stack Timing & Challenge

<i>Year of Introduction "Technology Node"</i>	<i>1999 180 nm</i>	<i>2000</i>	<i>2001</i>	<i>2002 130 nm</i>	<i>2003</i>	<i>2004</i>	<i>2005 100 nm</i>
<i>Isolated Line (nm)</i>	140	120	100	85	80	70	65
Equivalent physical Oxide Thickness T_{ox}(nm) (A)	1.9-2.5	1.8-2.3	1.6-2.0	1.3-1.7	1.2-1.6	1.0-1.4	0.9-1.1
Dielectric Leakage (A/cm^2) (B) Logic	3	3	3	3	3	4	4

- **High K gate stack could be required as early as the year 2004**
- **It is a challenge of substantial scope**
- **Changes of this magnitude have normally taken 10 years to implement**
- **Current resources applied to this task will not achieve 5-year implementation**

Scope of the High-K Challenge

- **Materials Selection (currently underway)**
 - High dielectric constant & high tunneling barrier height requirements
 - Dual Electrodes (Metals?) for CMOS gates
 - Chemical & electrical stability of Dielectric/Silicon interface
 - Chemical & electrical stability of Dielectric/Gate electrode interfaces
 - Will interface Si-O buffer layer be required?
- **Dielectric/Channel Interface characterization & optimization**
 - Achievement of stable MOS transistors meeting ITRS I-on and I-off requirements
- **Establish dielectric high-field and high-frequency reliability and performance**
- **Establish Gate Stack Testing & Metrology methods & standards**

Scope of High K Challenge (con't.)

- **Definition of CMOS process integration plan**
 - **Compatibility of High Temperature Dopant Activation with low temperature High-K requirements**
 - **CMOS integration of dual metal gate process**
 - **Maintenance of Self-Aligned processes**
 - **Compatibility with Elevated S/D device architectures**
- **Definition of Unit Processes & Requirements**
- **Development of alpha and beta tool sets**
- **Demonstration of first silicon**
- **All this within 5-7 years!!!!**

DRAM Scaling Challenges

- **DRAM storage node scaling will require extensive changes in capacitor dielectric materials and electrode materials & structures**
 - High-K and Ultra-high-K Dielectric layers
 - Metal, and conductive Perovskite electrode structures
- **Significant challenges of CMOS integration are also visible**
 - Storage cell limits process temperatures to $<500^{\circ}\text{C}$
 - Cell last process architectures may be required
- **The DRAM challenge rivals the High-K gate stack challenge in magnitude and scope.**

Summary & Highlights

- **Multiple FEP Materials & Process Integration Challenges:**
 - Dual metal/high-**k** CMOS gate stack process
 - High-**k** DRAM Storage Capacitor Structures
 - Solutions are required soon!
 - Challenges are Substantial (~2005)
 - There is reason for optimism
 - Need to achieve node-extendable solutions
- **Innovative new Device concepts needed ~2008**
- **There is the urgent need to dramatically expand our FEP materials knowledge base**

DRAM Stacked Capacitor Films Technology Roadmap (Table 22b)

ITRS Conference on July 8-9, 1999

S.Kawamura

Fujitsu

(rhd01125@nifty.ne.jp)

Parameter	1G	4G	16G	64G	256G	1T
DRAM Generation (A)	1G	4G	16G	64G	256G	1T
Cell area factor a (B)	10.0	8.0	8.0	7.0	7.0	6.0
Cell area [um ²] (C)	0.32	0.14	0.080	0.034	0.018	0.007
	=0.36*0.9	=0.26*0.52	=0.2*0.4	=0.14*0.25	=0.1*0.18	=0.07*0.11
Storage Node area [um ²] (D)	0.130	0.051	0.030	0.012	0.006	0.002
	=0.18*0.72	=0.13*0.39	=0.1*0.3	=0.07*0.18	=0.05*0.15	=0.035*0.07
capacitor structure	Cylinder MIS Ta ₂ O ₅	Cylinder MIM Ta ₂ O ₅	STD-STACK MIM BST	STD-STACK MIM epi-BST	STD-STACK MIM epi-BST	STD-STACK MIM ???
dielectric constant	22	50	250	700	800	1500
SN Height H [um]	0.70	0.37	0.35	0.20	0.18	0.12
cylinder factor (E)	1.5	1.5	1.0	1.0	1.0	1.0
total Capa area [um ²]	2.08	0.65	0.31	0.11	0.07	0.028
Structural Coefficient (F)	6.4	4.8	3.9	3.2	4.0	3.8
teq@25fF [nm] (G)	2.9	0.90	0.43	0.15	0.10	0.04
t _{phy.} @25fF [nm] (H)	10.6	11.6	27.4	27.3	19.6	14.7
A/R or SN (OUT) for cell plate depo. (I)	4.4	3.5	7.8	13.0	16.7	21.3
HAC diameter [um] (J)	0.22	0.16	0.12	0.08	0.06	0.04
Total Interlevel insulator and metal thickness except SN [um] (K)	1.10	0.99	0.89	0.80	0.72	0.65
HAC depth [um] (L)	1.80	1.36	1.24	1.00	0.90	0.77
HAC A/R	8.3	8.7	10.3	11.9	15.0	18.3
Vdd [V] (M)	1.8	1.5	1.2	0.9	0.6	0.5
Retention Time [ms] (N)	128	256	512	1024	2048	4096
Leak Current [fA/cell] (O)	0.527	0.220	0.088	0.033	0.011	0.005
Leak Current Density (A/cm ²)	2.5E-08	3.4E-08	2.8E-08	3.0E-08	1.6E-08	1.7E-08
Process Temperature [C]	<50	<50	<50	<50	<50	<50
Anneal Temperature [C]	<80	<70	<70	<60	<60	<60
DRAM Gox [nm] (P)	6	5	4	3	2	1.5
C _{gate} [F/cell] (Q)	1.9E-16	1.2E-16	8.6E-17	5.6E-17	4.3E-17	2.8E-17
Wordline R _s [ohm/sq.] (R)	10	8.3	6.7	5.0	3.3	2.5
Cbitline (S)	1	0.79	0.62	0.49	0.39	0.30
Bit line R _s [ohm/sq.] (T)	10	5.3	4.0	2.2	1.4	0.7

DRAM Stacked Capacitor Films Potential Solutions

Upper Electrode (U)	poly-Si	TiN	TiN	metal		
high-k dielectric	ON	Ta ₂ O ₅		BST, STO	Epi-BST	
Bottom Electrode (U,V)	poly-Si		metal	perovskite		

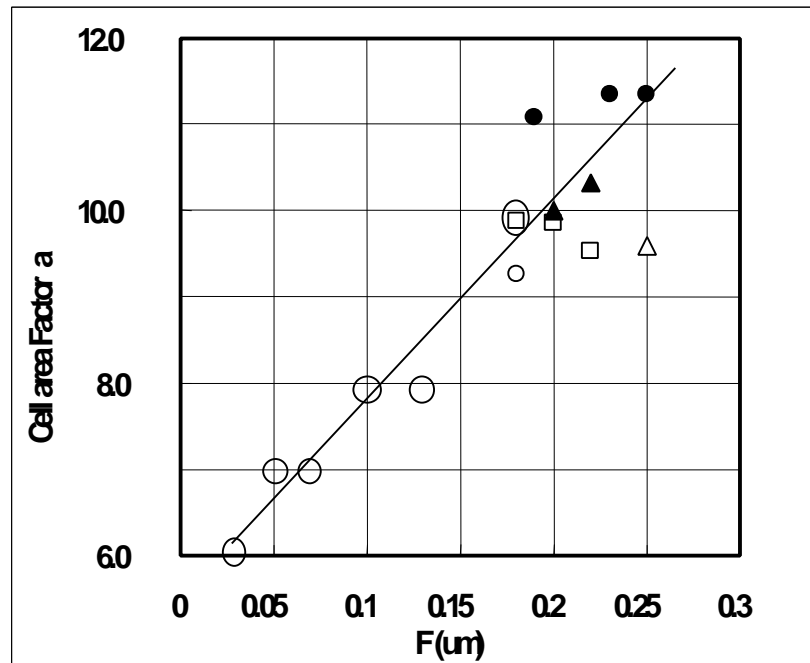
Possible capacitor structure and materials

Assumption: cell capacitance 25fF/cell

Technology Node	180nm	150nm	130nm	110nm	90nm	70nm	50nm
capacitor structure	Cylinder MIS Ta2O5	Cylinder MIM Ta2O5	STD- STACK MIM BST	STD- STACK MIM epi- BST	STD- STACK MIM epi- BST	STD- STACK MIM epi- BST	STD- STACK MIM ???

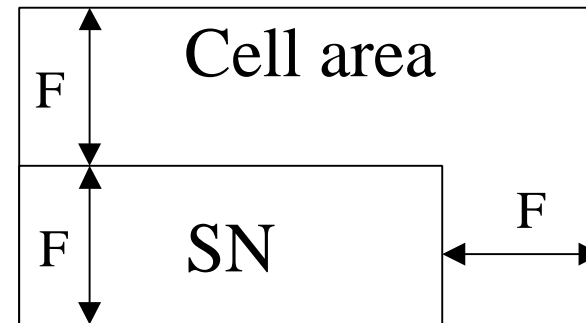
Integration Time (ms) 128 256 512 1024 2048 4096

Cell area factor “a”



The trend of cell area factor (a)

Cell area = $a * F^2$
SN area = $(a/2 - 1) * F^2$
F : minimum feature size
SN : Storage Node

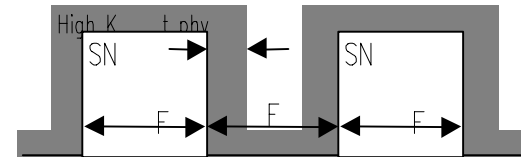


Cell area and projected SN area

Storage Node height

- Calculation of ...
 - total capacitor area (A_c)
 - T_{eq} (SiO_2 equivalent thickness)

$$= 3.9 \times 10^{-3} \text{ nm} \cdot A_c / C_{\text{capacitor}}$$



A/R of SN (for upper electrode depo .)

- A/R of SN (for upper electrode deposition)

$$= \text{SNheight} / (F - 2 \cdot t_{\text{phy}})$$

- A/R of HAC (HAC : High Aspect Ratio Contact)

- $\text{HACdiameter} = 1.2 \cdot F$

- Interlevel insulator and metal thickness is assumed to be 1.2um@180nm node and 10% reduction by each node.

Cell Leakage Current and Process/Anneal Temperature

- Leakage current is calculated on the assumption that ...
 - Sense error occurs when storage charge loss reaches 30%.
 - Process and Temperature margin is x100.

$$\frac{I_{\text{leak}}(t) \cdot t}{C} \leq 0.3 \cdot Q_{\text{init}}$$

$$V_{\text{leak}}(t) \leq 0.3 \cdot V_{\text{init}}$$

- Process temperature for capacitor film deposition and Anneal temperature for capacitor
 - These temperatures are based on the recently reported data

Word line and Bit line Rs

- W/L and B/L Rs are calculated on the assumption that $R \cdot C$ is constant at the same line length.

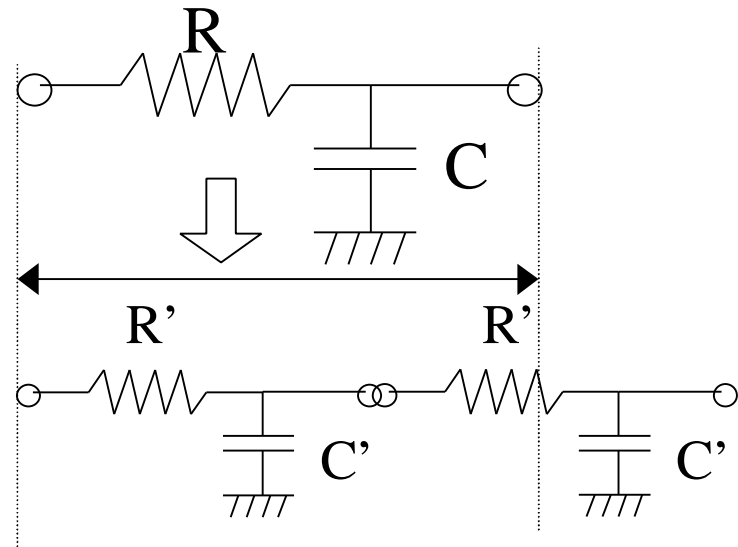
- R_s is assumed to be 10ohm/sq.
@ 180nm node.

- $CW/L = 3.9 \cdot 10^{-15} \cdot F^2 / tox$
(Gate Area = F^2)

- $CB/L \propto F^{2.3}$ (1)

$$R \cdot C \propto 1.4R' \cdot 1.4C'$$

(70% shrink by generation)



(1) A. Nitayama et al., IEDM Technical Digest, pp. 355-358, 1998.

DRAM Capacitor Difficult Challenges

- High-k capacitor dielectrics
- Metal electrode for MIM
- Etching of SN and electrode
- Etching of high aspect ratio contact hole
- Reducing film deposition /anneal temperature
- New cell architecture required
 - open bit-line, cross-point, multi-state, etc.
- New concept memory cell: gain cell, FeRAM, etc.