ITRS
Design DTWG

July 8, 1999
ITRS Roadmap Conference
Santa Clara, CA

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DTWG Members

Richard Howard	Lucent	(Chair)
William Joyner	SRC/IBM	(Co-Chair)
Richard Newton	UC Berkeley	(ITWG)
Steven Schulz	Texas Instr	(ITWG)
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Justin Harlow	SRC	

Test

Robert Aitken	H-P
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Synthesis and System Design

John Darringer	IBM
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Paul Capozza	Mitre
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Design Techniques

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Alfred Dunlop	Lucent
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Physical Design

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Verification

Carl Pixley	Motorola
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Design Environment

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Design Technology Issues

- Design systems are already at the breaking point in dealing with today' products because of:
  - Increasing complexity
    - Process complexity
    - Functional complexity (HW and embedded software)
    - System on a chip heterogeneity
  - Increasing frequency
  - Increasing importance of time-to-market ("Internet Time")
- Failure to address these issues directly will limit our ability to extract the full value from our manufacturing technology

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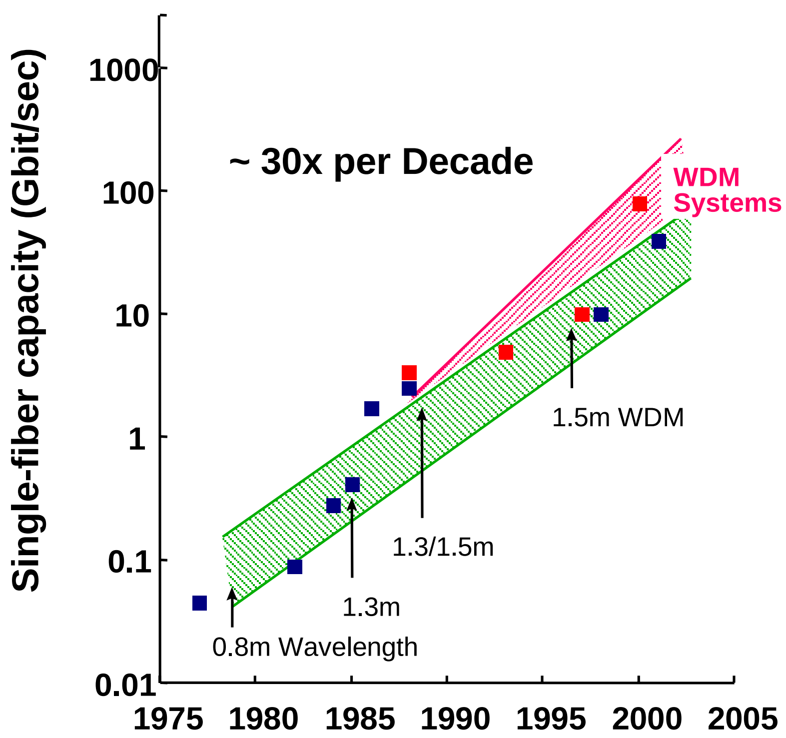
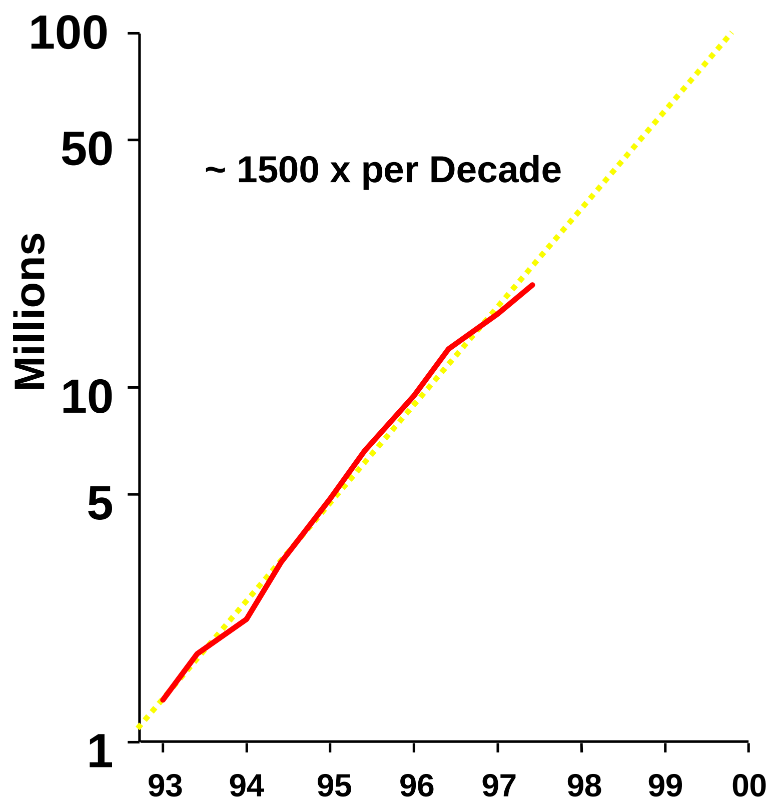
Global Communications Growth

Photonics



Courtesy R. Martin

Internet Hosts



Source: Network Wizards
http://www.nw.com/

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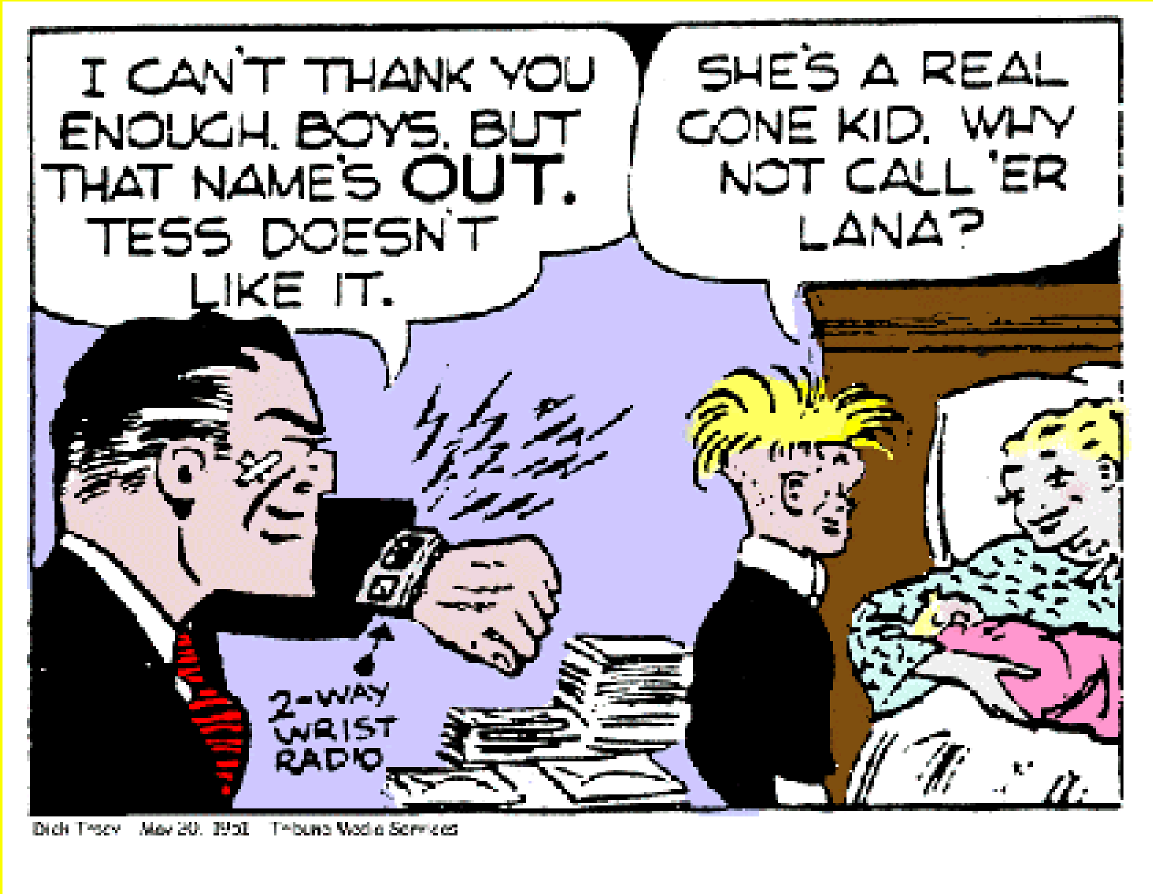
2-Way Wrist Radio--The Vision in 1946



- *Introduced January 13, 1946*

IC Design Roadmap

- Enable users of ICs to create products with the highest value using the current IC manufacturing technology
- Unlike other parts of the Roadmap, all advances in any area can be used to increase productivity and lower cost at any node.
  - No structured timeline of advances, it just gets easier or harder depending on the state of the tools.
  - Cost/difficulty of design will limit the ability to utilize IC manufacturing capability

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Superexponential Design Complexity

1 K

Transistors

1 Billion

- Functionality + Testability
- Functionality + Testability + Wire Delay
- Functionality + Testability + Wire Delay + Power Mgmt
- Functionality + Testability + Wire Delay + Power Mgmt +Embedded software
- Functionality + Testability + Wire Delay + Power Mgmt +Embedded software + Signal Integrity
- Functionality + Testability + Wire Delay + Power Mgmt +Embedded software + Signal Integrity + Hybrid Chips
- Functionality + Testability + Wire Delay + Power Mgmt +Embedded software + Signal Integrity + Hybrid Chips + RF
- Functionality + Testability + Wire Delay + Power Mgmt +Embedded software + Signal Integrity + Hybrid Chips + RF + Packaging
- Functionality + Testability + Wire Delay + Power Mgmt +Embedded software + Signal Integrity + Hybrid Chips + RF + Packaging + Mgmt of Physical Limits

☞Exponentially growing number of devices

☞Design complexity is exponential function of device count

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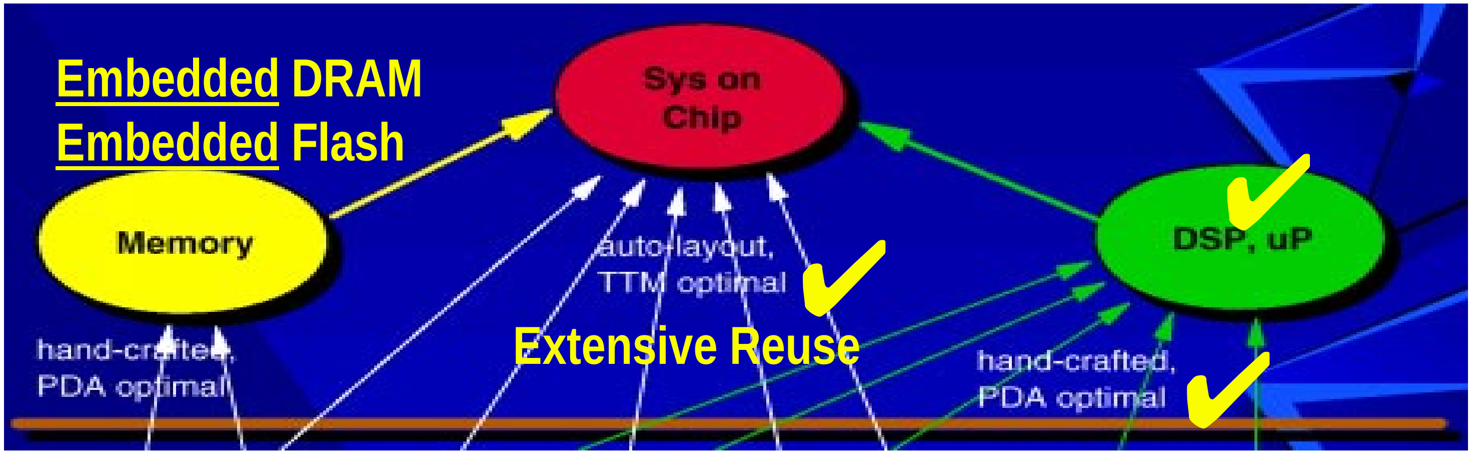
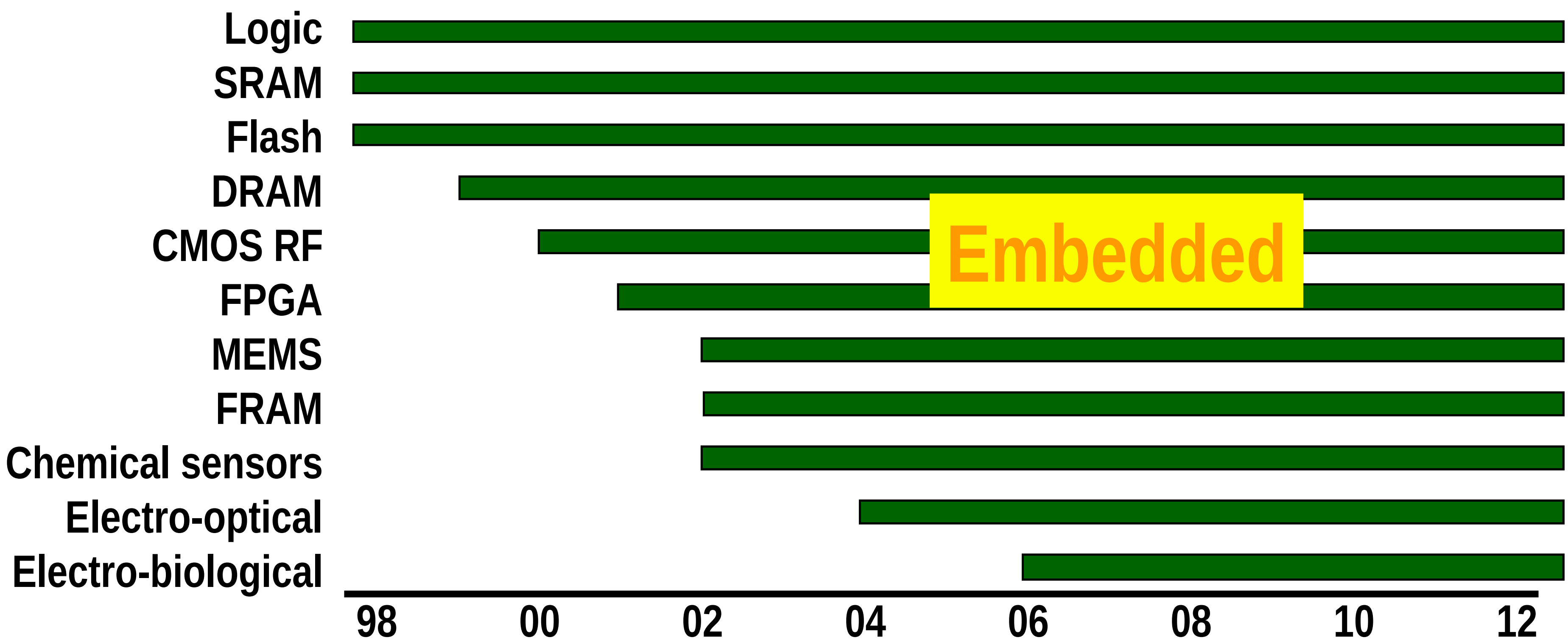
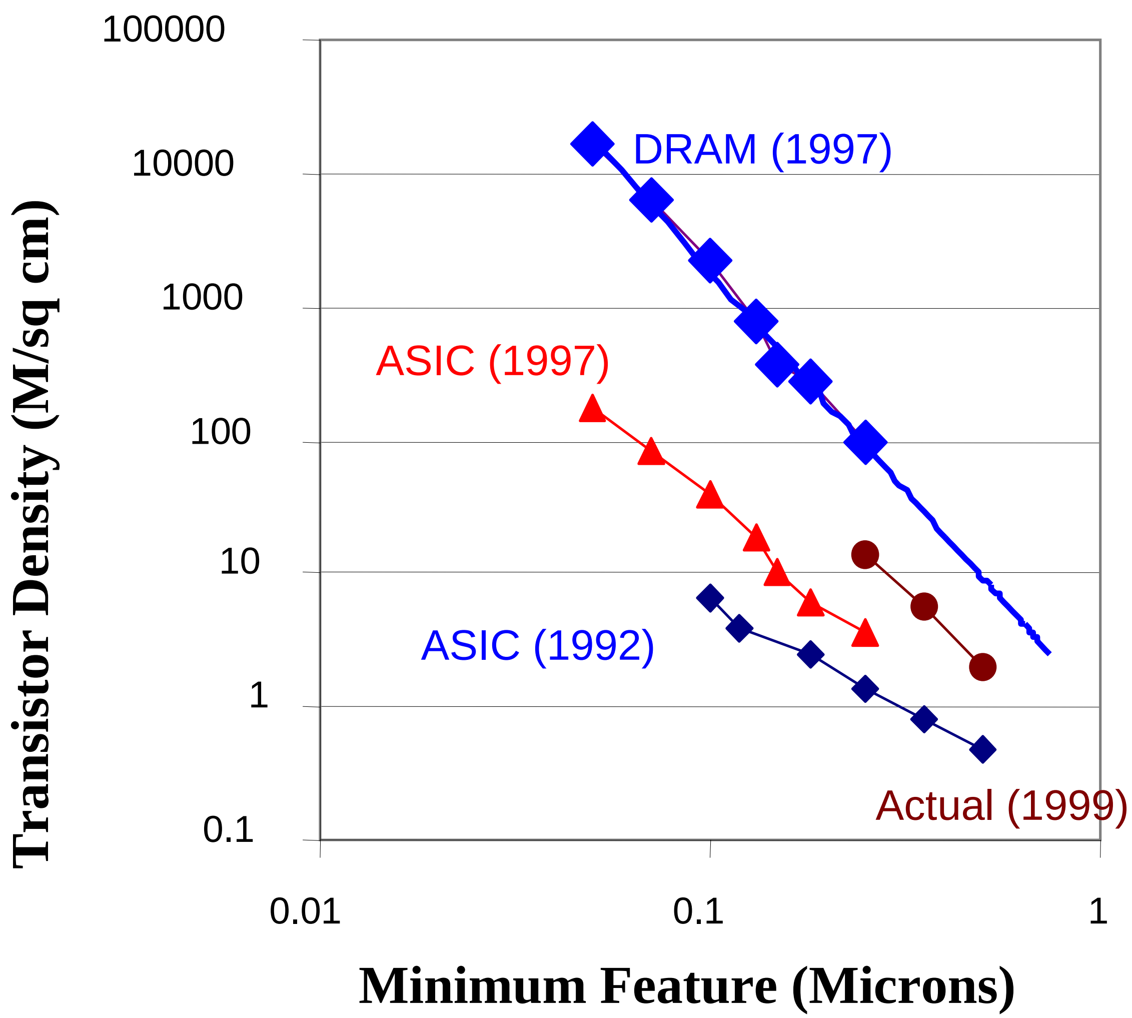
International Technology Roadmap for Semiconductors

System-On-A-Chip Implies Mixed Technologies





ASIC Area Productivity Increases



ASIC densities have increased rapidly over last 3-5 years

New tools and MLM have brought density to 90% of max.

Future scaling will track DRAM

This puts even more pressure on design productivity

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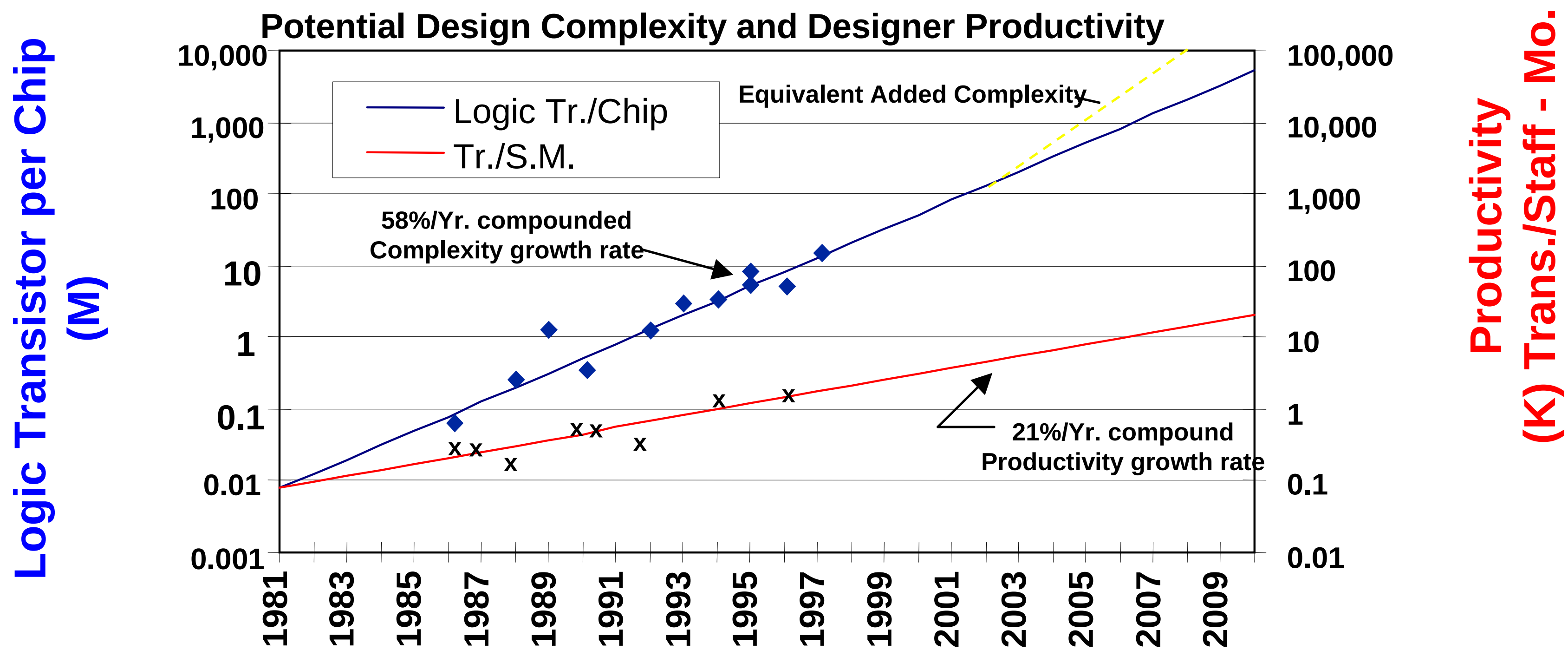
Design Productivity Crisis



Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $150K / Staff Yr. (In 1997 Dollars)

Design Productivity and TTM Drive Revenue

- "Investment Theory 101"
  - Focus human CPU cycles on greatest return (Corollary: automate ***all*** else (or reuse))
  - ***Earliest*** design decisions have largest impact (Corollary: highest abstraction)
  - Products that miss market windows are dead (Corollary: Time-to-market is king)
- Raising working level of abstraction historically offers greatest leverage
  - Architecture, co-design, IP reuse
  - Requires ***bottoms-up*** feedback across flow

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"Moore's Suggestion"

- It's NOT a fundamental law of physics
  - It's now a business proposal for investment
  - laws of physics may constrain its path
- It only works if revenue growth justifies the investment
- Memory density is no longer the driver
  - Objective function = (market value)/chip
  - Embedded software is a major component of the value
- ***Design productivity*** is the primary cost bottleneck moving forward
- This ***is*** a fundamental constraint arising from exploding complexity at all levels of the IC creation process

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Critical Challenges $\geq$ 100 nm

- **Silicon Complexity**
  - Large numbers of interacting devices and interconnects
  - Atomic-scale effects
  - Impact of signal integrity, noise, reliability, manufacturability
  - Need for new logic families to meet performance challenges
  - Power and current management; voltage scaling
  - Alternative technologies (e.g. copper, low K, SOI)

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Critical Challenges $\geq$ 100 nm

- **System Complexity**
  - Greatly increased system and function size
  - System-on-a-chip design with a diversity of design styles (including analog, mixed signal, RF, MEMS, electro-optical)
  - Integrated passive components
  - Embedded software as a key design

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Critical Challenges $\geq$ 100 nm

- **Design procedure complexity**
  - Interacting design levels with multiple, complex design constraints
  - Convergence and predictability of design procedure
  - Specification and estimation needed at all levels
  - Technology re-mapping or migration to maintain productivity
  - Core-based, IP-reused designs and standards for integration
  - Large, collaborative, multi-skilled, geographically distributed teams

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Critical Challenges ≥ 100 nm

- **Verification and analysis complexity**
  - Early high-level timing verification
  - Formal methods for system-level verification
  - Core-based design verification (including analog/mixed signal)
  - Verification of complex processors and architectures
  - System on a chip specification
  - Verification of heterogeneous systems (including mixed signal, MEMS)
- **Test/testability complexity**
  - Quality and yield impact due to test equipment limits
  - Test of core-based designs from multiple sources (including analog, RF)
  - Difficulty of at-speed test with increased clock frequencies
  - Signal integrity testability

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Critical Challenges < 100 nm

- **Silicon complexity**
  - Design with novel devices (multi-threshold, 3D layout, SOI, etc.)
  - Soft errors
  - Uncertainty due to manufacturing variability
  - Uncertainty in fundamental chip parameters ()
- **System complexity**
  - Total system integration including new integrated technologies (e.g. MEMS, electro-optical, electro-chemical, electro-biological)
  - Design techniques for fault tolerance
  - Embedded software and on-chip operating system issues

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Critical Challenges < 100 nm

- **Design procedure complexity**
  - True one-pass design process supporting incremental and partial design specification
  - Integration of design process with manufacturing to address reliability and yield
- **Verification and analysis complexity**
  - Physical verification for novel interconnects (optical, RF, 3-D, etc.)
  - Verification for novel devices (nanotube, molecular, chemical, etc.)
- **Test/testability complexity**
  - Dependence on self-test solutions for SOC (RF, analog, …)
  - System test (including MEMS and electro-optical components)

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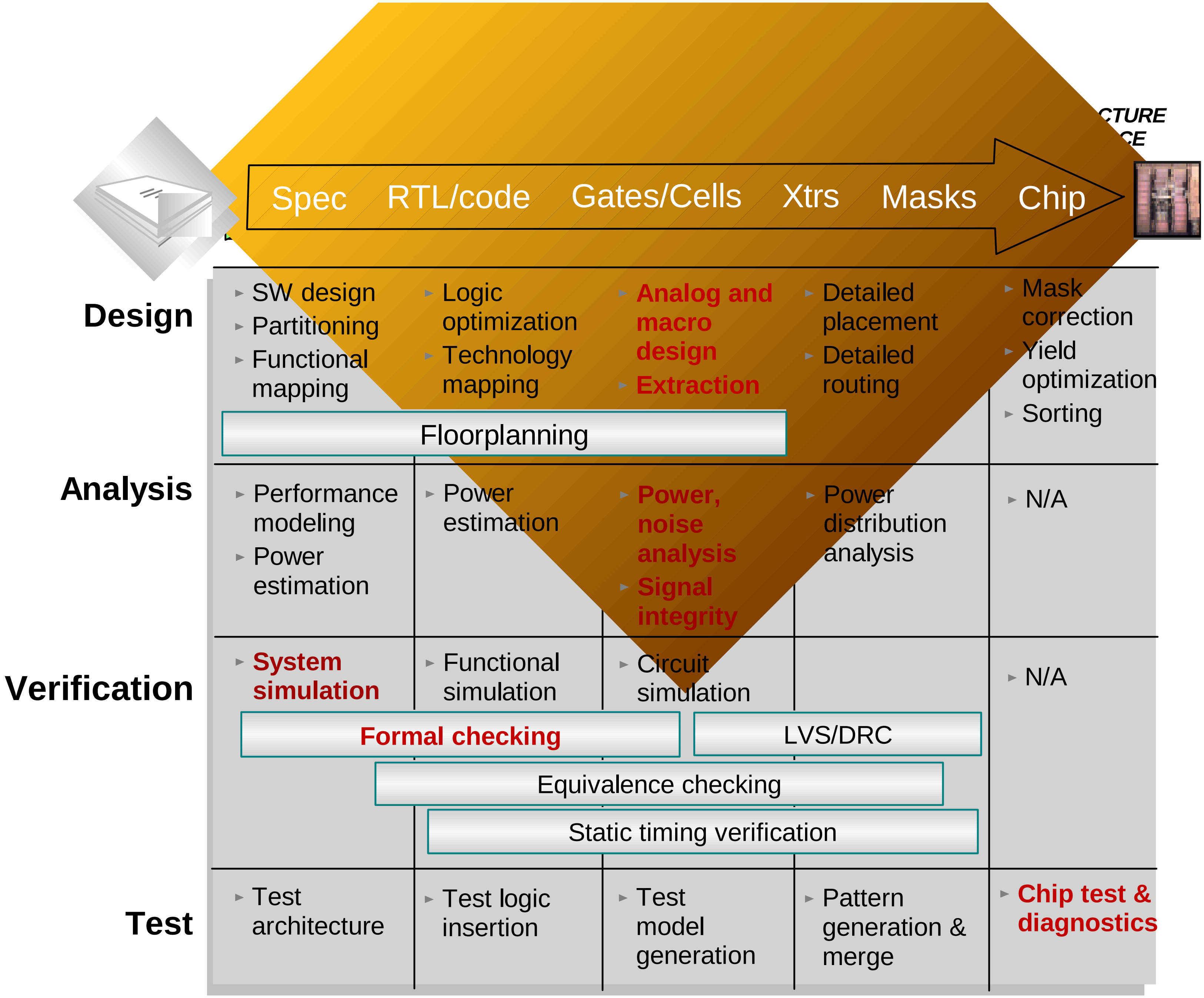
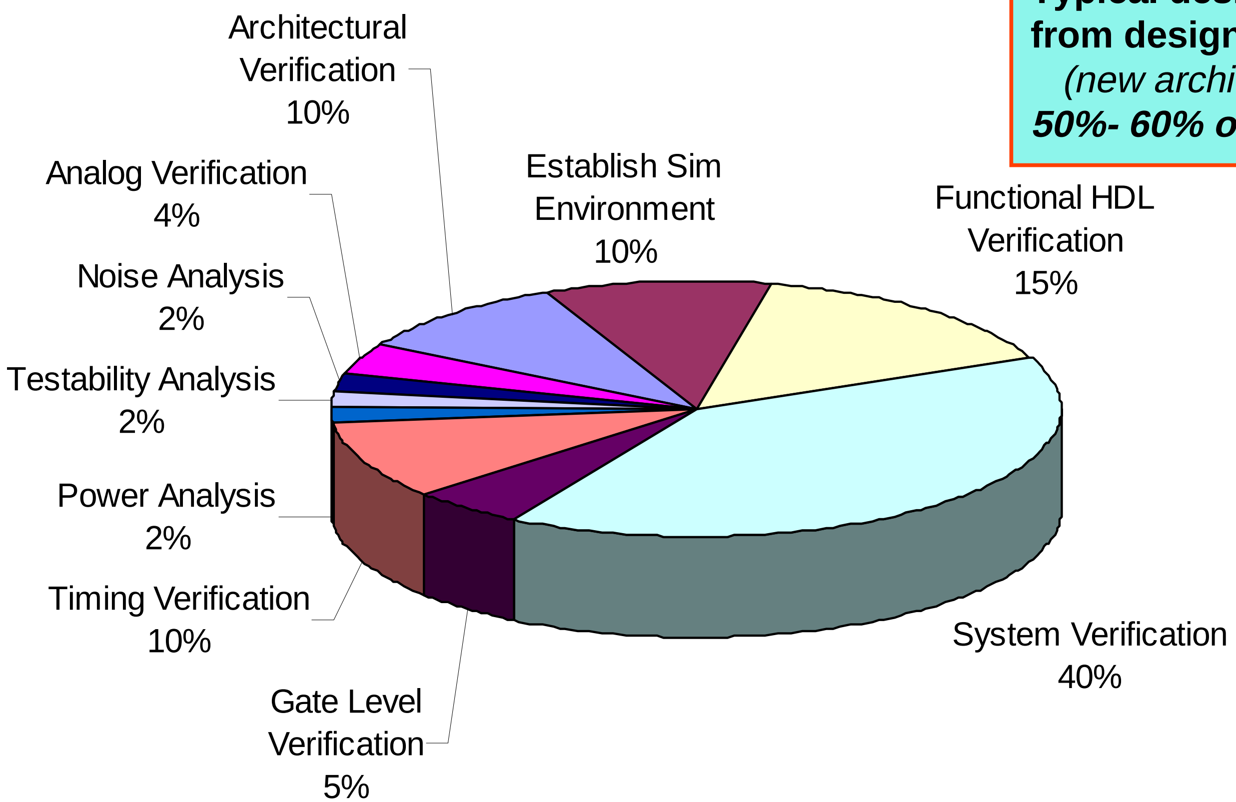


New Figure 4 (Draft Rev. B, 3-12-99)

Red denotes most challenging activity

Verification > 50%of Total Design Effort
(estimated)

Typical design takes 18-24 months from design start to full production
(new architecture, limited reuse)
50%- 60% of this time is verification!



(Note: Design verification relatively node independent)

1999 ITRS Design Difficult Challenges - Verification and Analysis

Before year 2005

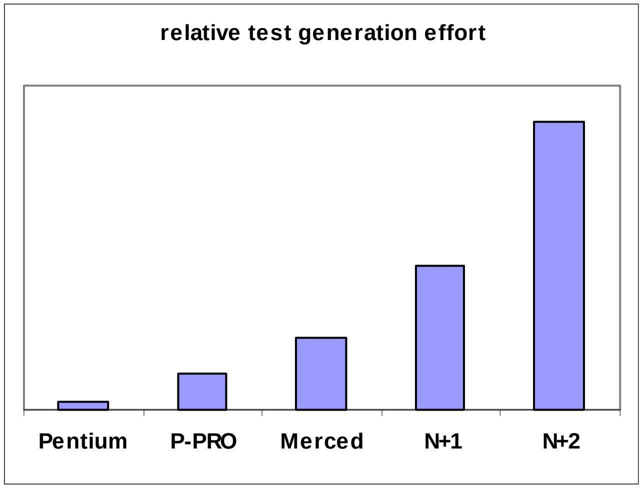
>Timing and function co-verification
>System-level formal verification/spec.
>Core-based design verification
>Complex processors & architectures
>Verification of heterogeneous systems
(mixed-signal, MEMs, etc.)

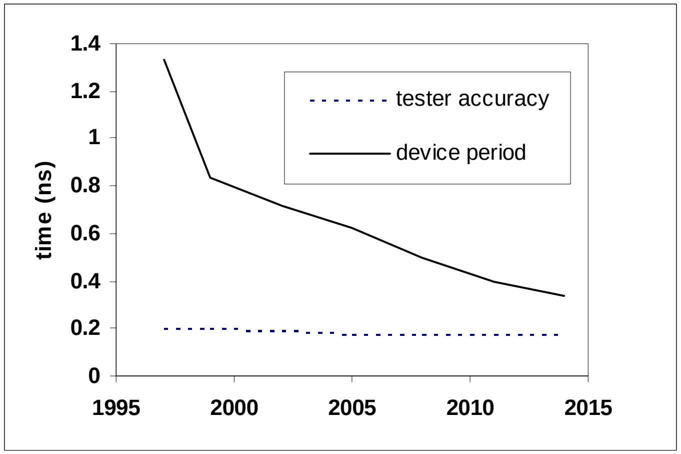
After year 2005

>Physical verification for novel interconnects
(optical, RF, 3D, etc.)
>Verification for novel devices
(nanotube, molecular, chemical etc.)

Design for Test Mandatory

- Cannot trade-off DFT versus functional test
  - too expensive to develop functional tests
  - testers will lack accuracy to apply functional tests
  - testers will lack accuracy to evaluate results of functional tests





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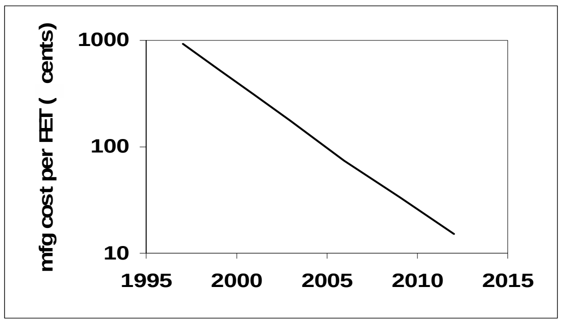
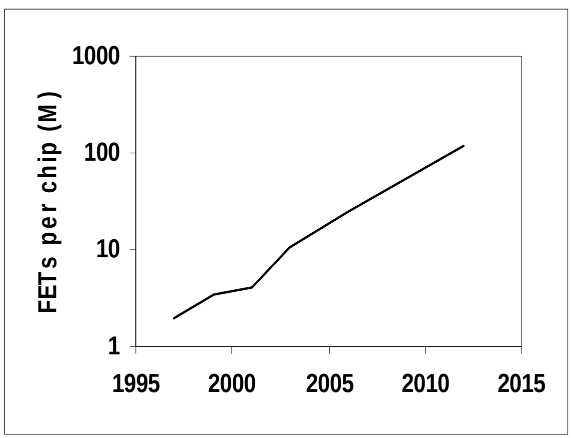
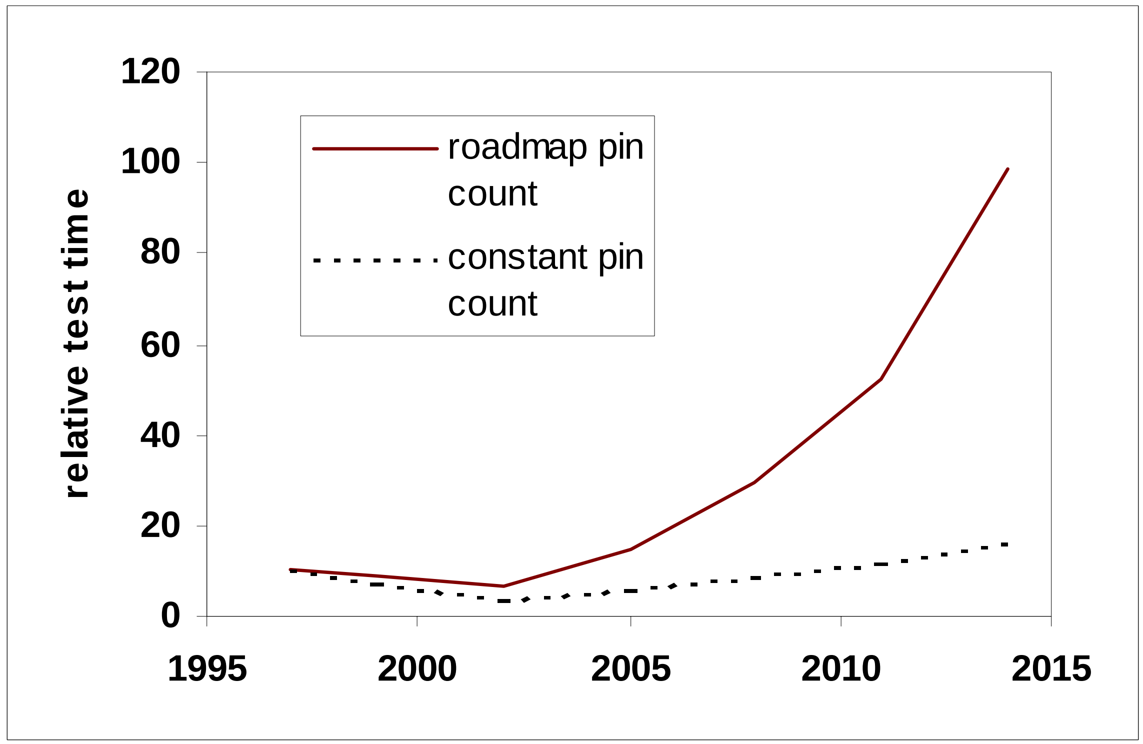
The Need for Built-In Self-Test

- Chip boundary cannot support needed data volumes without increasing test time







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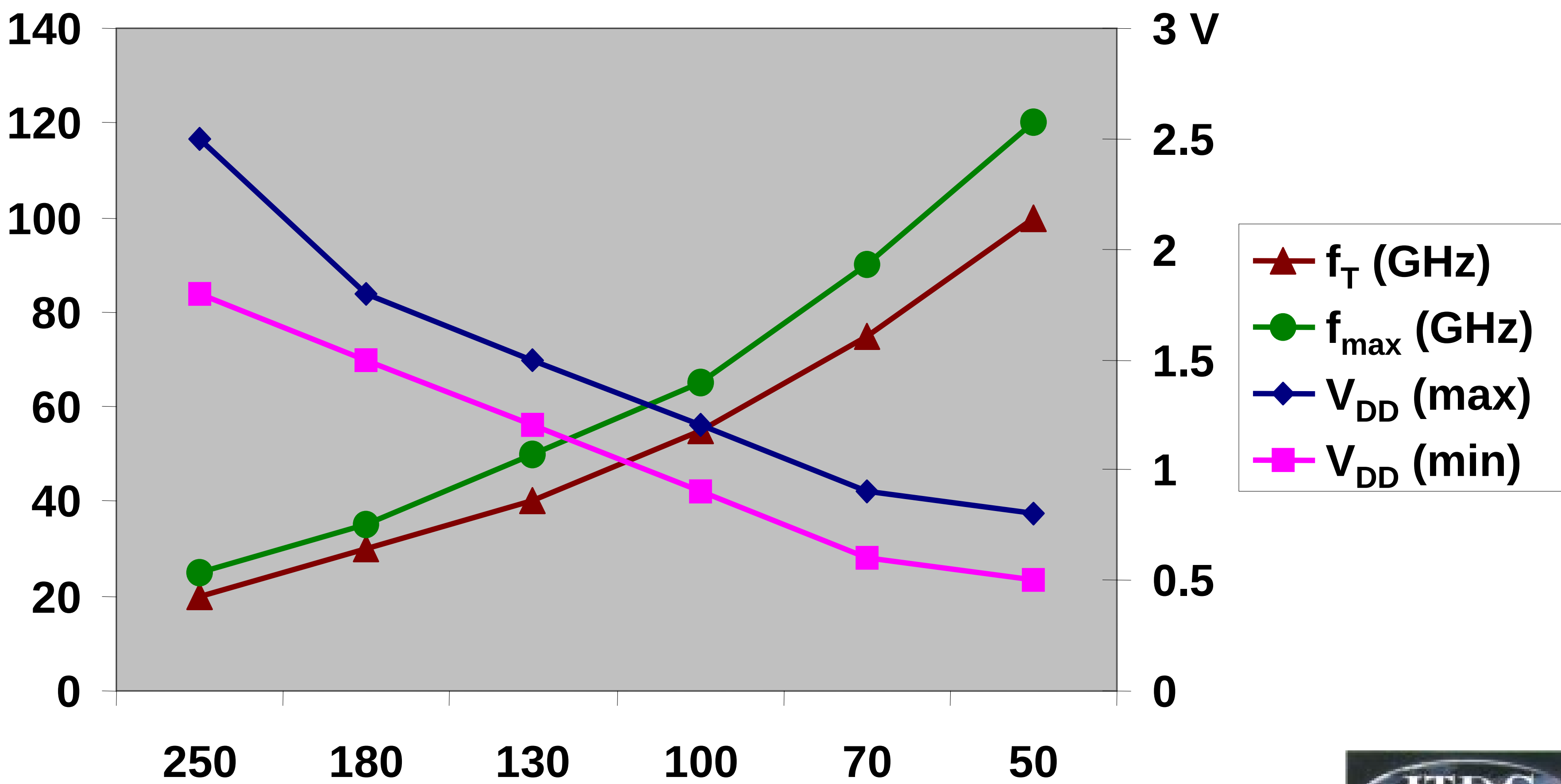
Analog MOS f_T and f_{max} with V_{DD} vs Technology Node



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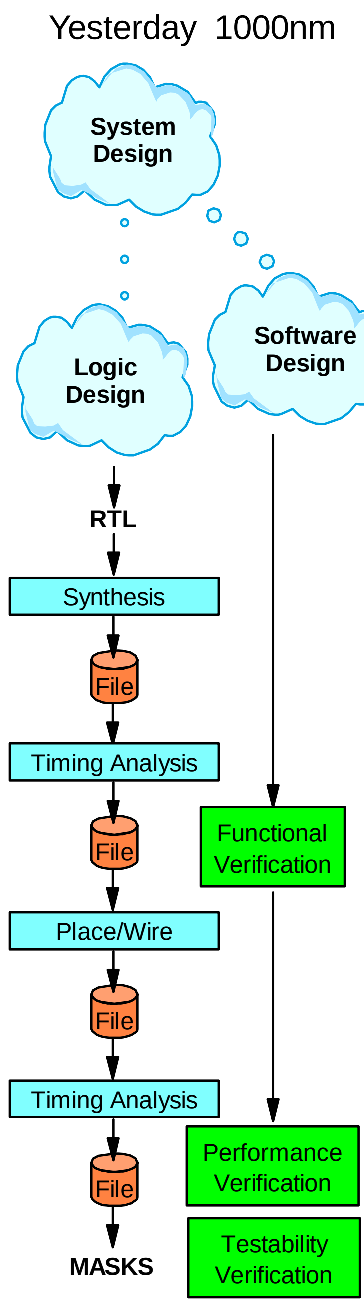
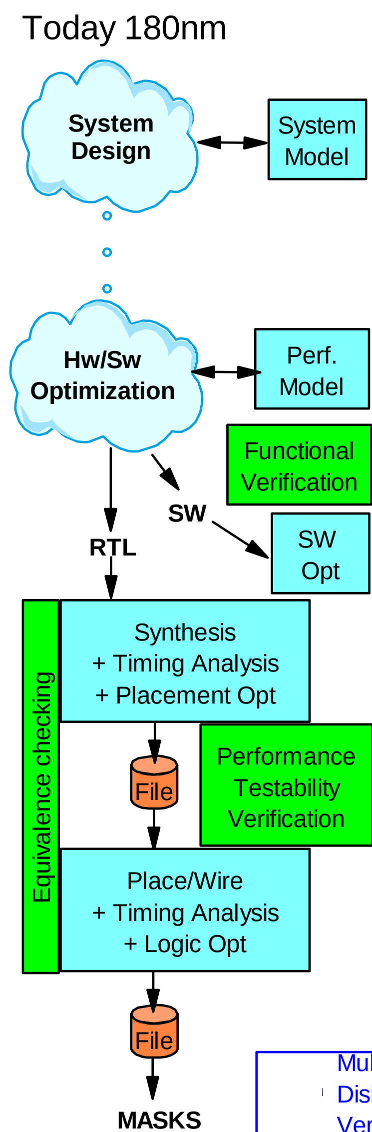
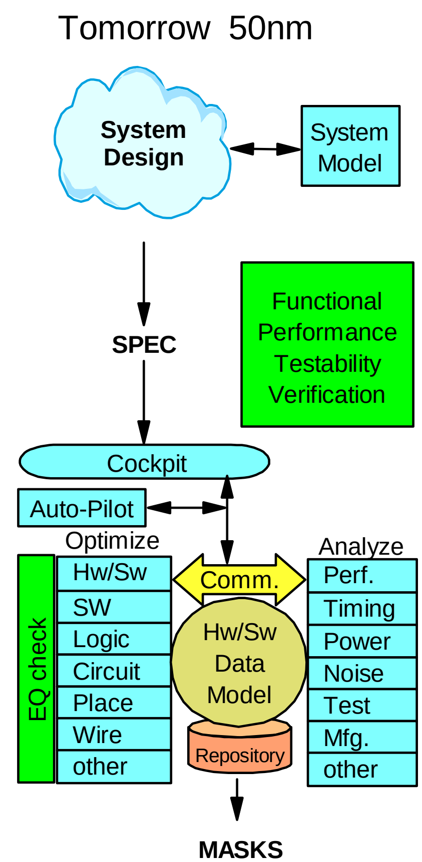
Required Advance in Design System Architecture







- Multiple design files are converged into one efficient Data Model
- Disk accesses are eliminated in critical methodology loops
- Verification of Function, Performance, Testability and other design criteria all move to earlier, higher levels of abstraction followed by
  - equivalence checking and
  - assertion driven design optimizations
- Industry Standard interfaces for data access and control
- Incremental modular tools for optimization and analysis

New Table 8

ITRS Working Group on System-on-a-Chip

ITRS Roadmap Conference

July 8, 1999

Santa Clara, CA

Al Dunlop, Bill Joyner, Richard Newton, Steve Schulz, Werner Weber (Design), Chris Case (Interconnect), Steve Hillenius (PIDS), Paco Leon (Modeling and Simulation), Chi-Shi Chang (Assembly and Packaging), Mark Barber (Test)

ITWG System-on-a-Chip: Our Mission

- **Define system-on-a-chip in terms of technology, products, characteristics, capabilities**
  - **contrasted with "traditional" roadmap categories of processor, ASIC, and memory**
- **Determine what tables (or additions to tables) need to be inserted to the roadmap to reflect SOC as a driver**
- **Develop a plan for providing the content of these tables or entries**

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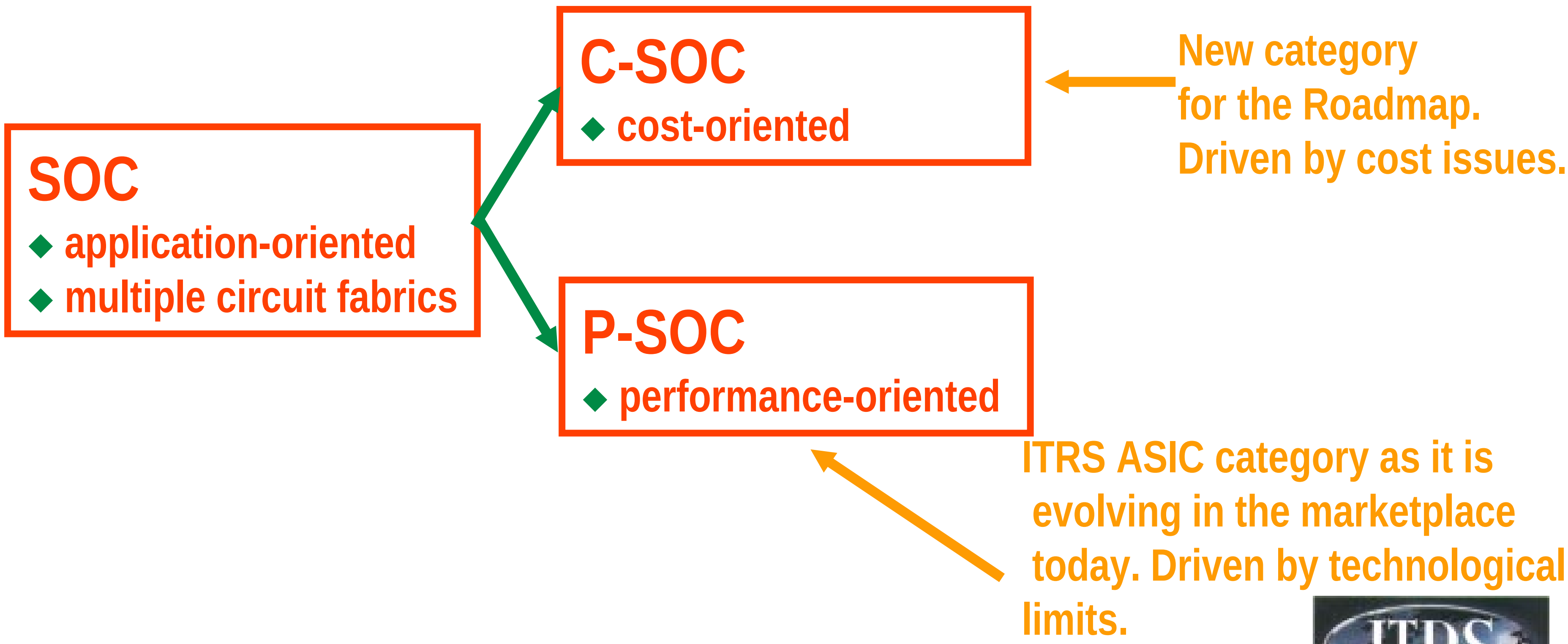
What is an SOC?

- A System-On-a-Chip (SOC, sometimes called System LSI) is an application-oriented design that has the following characteristics:



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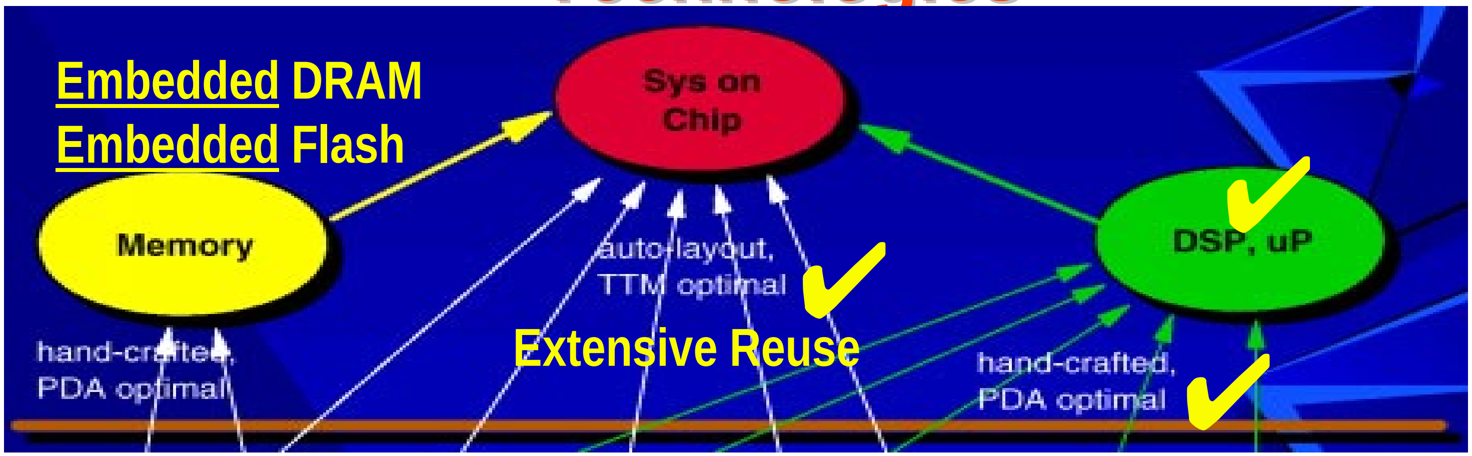
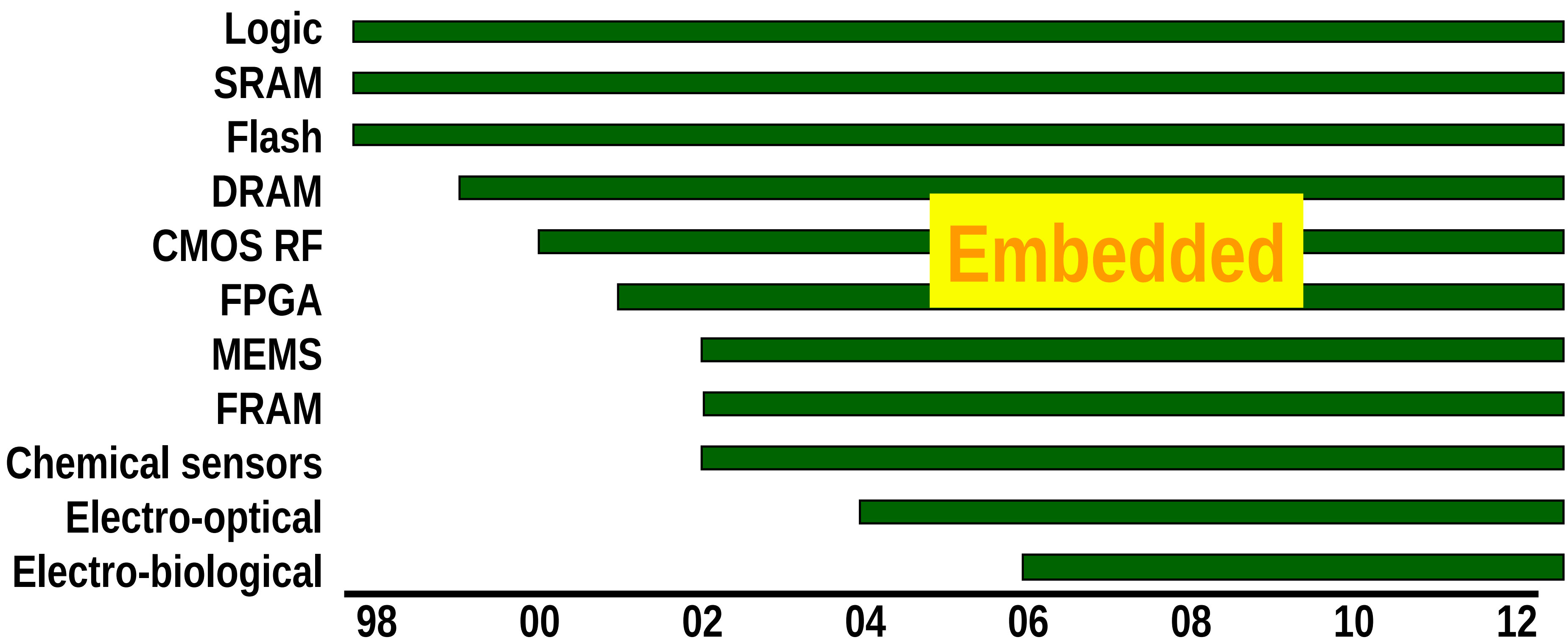
System-On-A-Chip Implies Mixed Technologies





Definition: Circuit Fabric

- Circuit Fabric: A particular classification of circuit and circuit design style, implemented in silicon, that share a set of process, functional and performance factors. Possible examples of different fabrics:
  - DRAM, E-DRAM, Flash, SRAM, FRAM, ...
  - Custom logic, Standard-cell logic, Array-based logic, FP logic, …
  - Analog, RF, Optical, Polysilicon MEMS
- Includes both process/manufacturing implications (e.g. special interconnect requirements, implants), as well as design-related implications (e.g. repairability, redundency, test methodology)
- All of these play a role in determining the overall cost and performance per unit of functionality (bit, gate, etc.)

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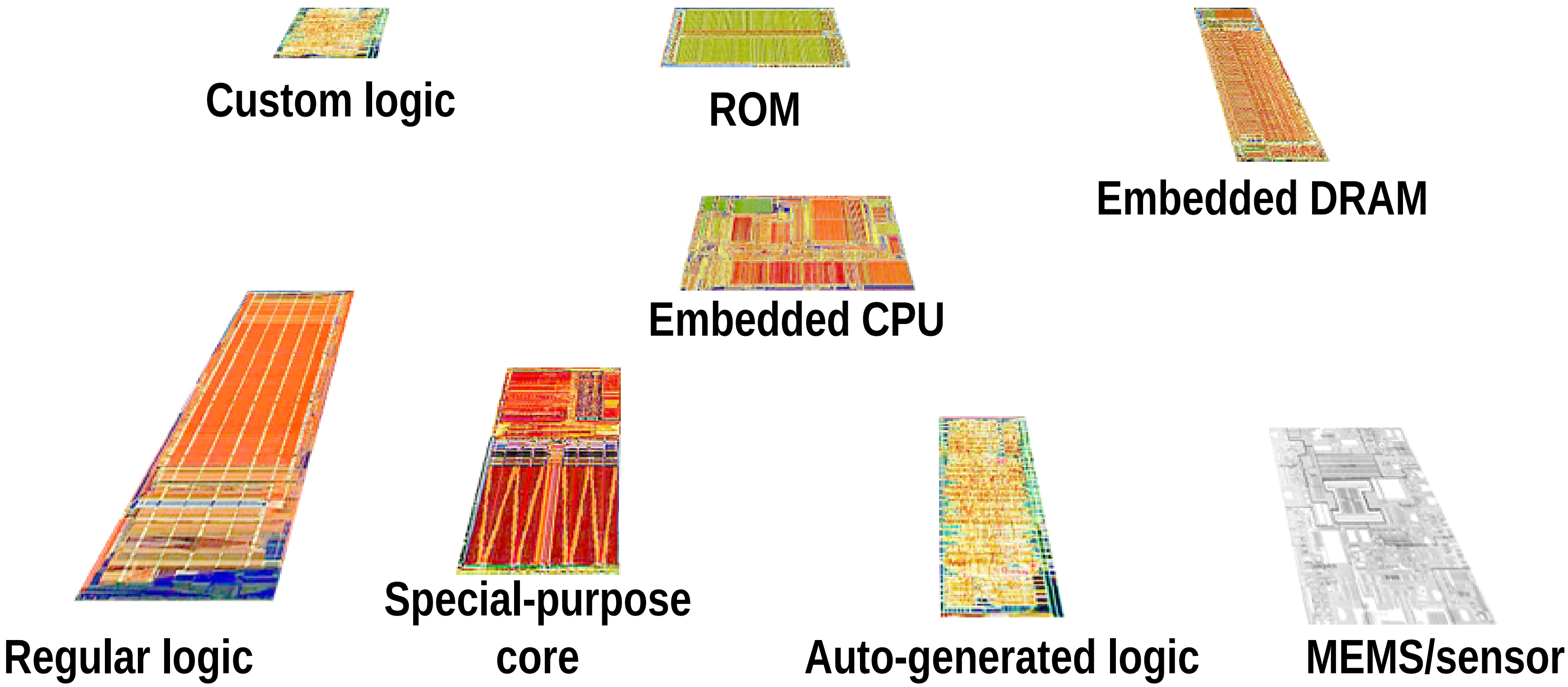
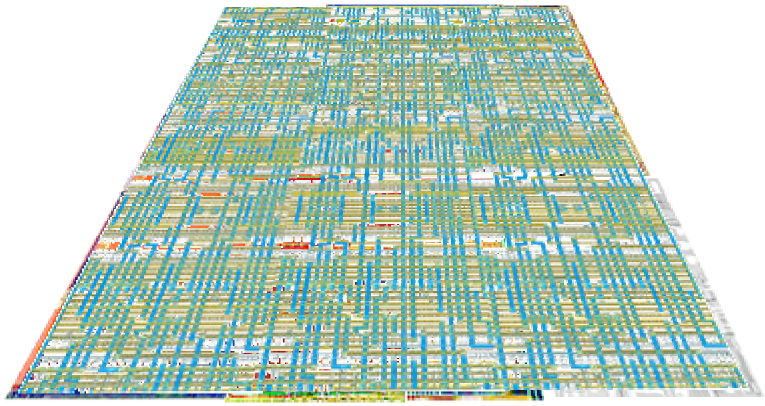
Component-Fabric-Based Approach to SOC

- Stage 1: Characterization of particular circuit fabrics
  - At a technology node
  - What is the yielded cost ($) per unit functionality (bit, gate, MPEG encode, etc.)?
  - What about other characteristics: performance, power, test, etc.



Component-Fabric-Based Approach to SOC

- **Stage 2: Characterization of assembled C-SOC and P-SOC**
  - **At a technology node**
  - **What is the *assembled* yielded cost ($) for a given mix of functionality?**
  - **What about other characteristics: performance, power, etc.**



- Assemble the components from characterized fabrics
- Wire them up and determine yielded cost and overall test and packaging costs

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Programmable versus Hard-Wired

- Ideally, to allow for inclusion if design issues related to embedded software (e.g. required improvements in code density, error rates, test issues), we should probably distinguish programmable versus non-programmable (hard-wired) designs in each category

	Programmable	Non-programmable
C-SOC	Low-cost PDA chip Digital camera chip FPGA Microcontroller-based SOC	Sensor interface Low-cost home RF front end
P-SOC	High-end game platform Set-top box High-end network router DSP	Read-channel for disc drive High-performance network chip

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One Approach to Analysis for SOC

Start Here → $$ Categories: (e.g. $1, $3, $10, $30, $100)

Packaging (40%?)

Test (30%?)

How many $$ left?

How complex a chip can I afford?

What can I build?

Mixed technologies

Semiconductor ITRS projections

Design reuse

Data We Would Like to See

- Tradeoff between functional capability in terms of area (total bits, gates, etc.) vs. approximate cost for each technology node
  - Feasible for MPU, DRAM, SRAM, and auto-generated logic
  - A real research problem for analog, RF, etc. (but needed!)
- Means of costing out the assembly of such fabric-specific components onto an overall die
- Implications to test and test methodology for both a fabric and an SOC (assembly of components)

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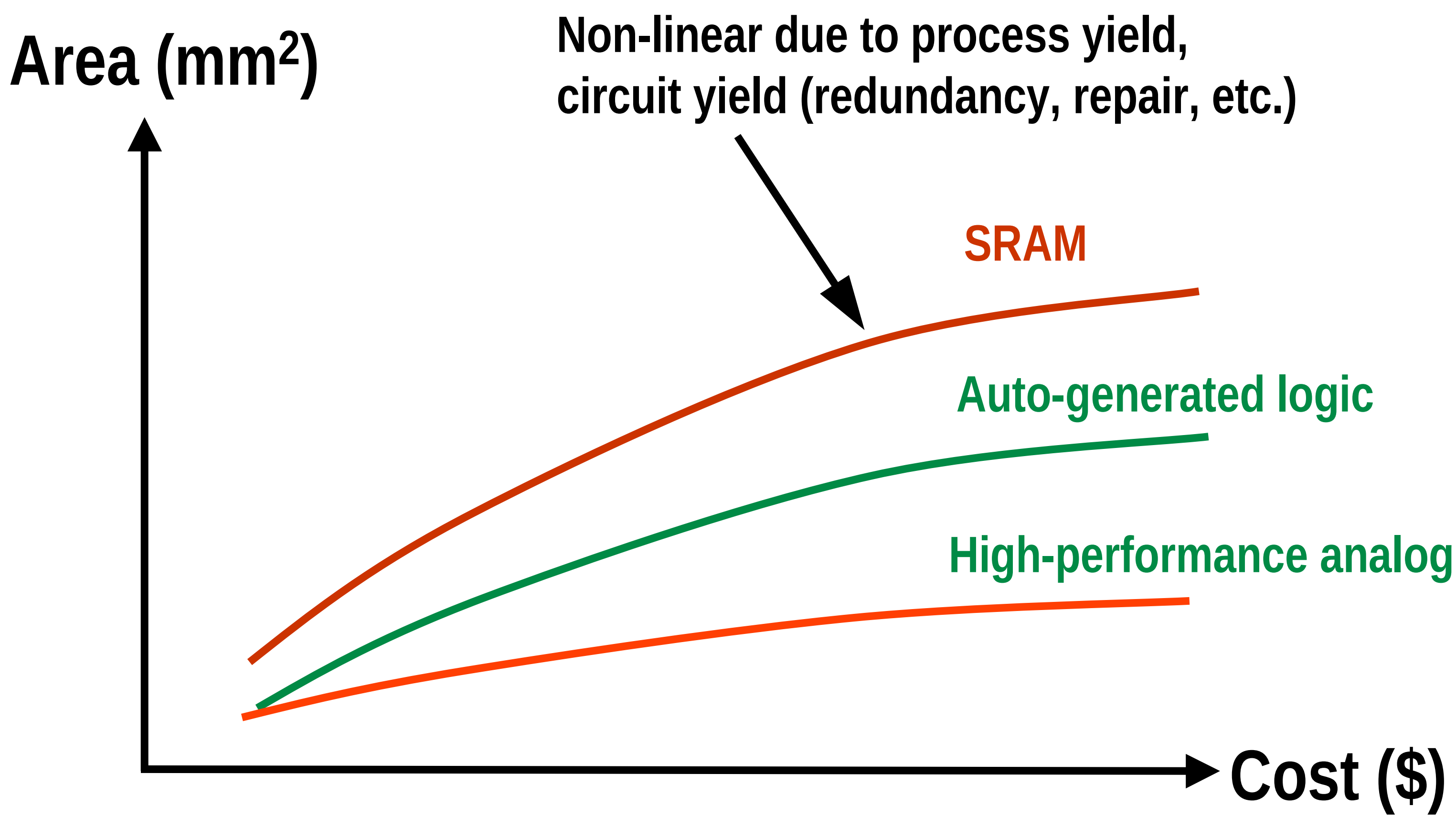
Data We Would Like to See

- Schematic Example:



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New Tables for ITRS

- Modify all places where "ASIC" is used to imply high-end (high-performance, high-power) to read "P-SOC"
- Add additional tables for selected circuit fabrics (where we can get the data!):
  - *For (component chip area) record: (est. yielded cost), (est. functional capacity--bits, gates, etc.), (est. test cost conventional and BIST) for the block*
- Add additional table for C-SOC assembly-related issues:
  - *For an assembled SOC record: (est. assembly overhead due to yield loss?), (est. package cost), (est. overall chip cost for particular fabric mix)*

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