Revised Table of Difficult Challenges

Old	New
Productization of new models	Gate stack modeling (e.g. alt.dielectrics, tunneling, breakdown, ..)
Defect-mediated profile evolution	Determine diffusion parameters (quantum calulations and experiment)
High-freq. interconnect modeling	High-frequency modeling add: substrate noise, NQS, gate RLC
Physical backend modeling	Materials modeling, interfaces, surfaces (Backend)
Package modeling	Package modeling
Predictive equipment simulation	Equipment modeling: (add CMP, Plasma, “effective chemistry”)
Predictive lithography simulation	Lithography simulation (add OPC, PSM, NGL)
Atomistic process modeling	Atomistic process modeling
Practical non-equilibrium transport	Nano-scale device model (quantum, alternatives)
Advanced quantum device modeling	Reliability simulation

3rd ITRS Roadmap meeting, Munich, 13/04/1999, M&S attendees

Paco Leon, US

Kenji Nishi, Japan

Andreas v. Schwerin, Europe

Shyh-Chyi Wong, Taiwan

Quantify the benefit of Modeling and Simulation

Design

No design possible without accurate compact models

Process development

To reduce costs and development time, TCAD models needs a certain accuracy

For longer-range analysis new model capabilities are needed

Two technology requirements tables:

1. Accuracy* necessary for
   - Cost reduction and time to market (TCAD)
   - Design (ECAD)
2. Capabilities (non-numerical)

*by new definition of accuracy, we reduce the red entries in the table

Technology Requirements Tables

Categories:

1. Equipment / Topography
2. Lithography
3. Process TCAD
4. Device (incl. Interconnect)
5. Compact models
6. Package
7. Numerical methods

Topics mentioned in the text:

1. Calibration
2. Statistical Modeling
3. Materials modeling
4. Reliability

Important modifications

Product specific technology requirements

- Mark specific technology requirements “Memory”, “MPU”, “SoC” (e.g. *stress* - memory, *etch/dep./growth uniformity* - SoC)
- Are we limited to MPU, Mem, and SoC, or shall we add analog, RF, ... ??

Industry standard circuit models

- Promote the standardization of compact models (CMC)
- Development of specialized models (e.g. SOI, flash, DRAM, FRAM, ...)

Procedure for decision on final contents of the 1999 roadmap

- Establish a web site at Sematech and post a draft version on it
- Suggestion for change is first approved in one region

  Changes are voted on by all regions
- Response is expected in less than 2 weeks (otherwise approved)