ITRS
Interconnect ITWG

13 April 1999
Munich

Process

- **Presentation of prepared materials**
  - **Japan**
  - **US**
- **Critique by all regions**
- **Completion of DRAM Technology Requirements Table**
- **Review of Potential Solutions Tables**
  - **need more work on Conductors, Planarization and Etch**
- **Generate XCUT discussion topics and visit other TWGS**
- **Convert ASIC table to SOC table**
  - **still need further input from PIDS and Design**
- **Plan activities for exchange for next 6 weeks (IITC)**

ITWG Participation

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Chapter Outline

- **Overview - 5P**
- **Dielectrics - 2P**
- **Conductors - 2P**
- **Planarization - 2P**
- **Etch - 2P**
- **Reliability - 2P**
- **System/Performance/Package Issues - 2P**
- **Metrology - 2P**
- **ESH - 2P**
- **Conclusion - 3P**

Overview Outline

- CMOS fabrication
  - Architecture
  - Process integration
    - sample cross-sections
    - Materials and Process issues
      - Dielectrics
      - Conductors
      - Planarization
      - Etch
  - Interconnect
    - local
      - cross-talk, capacitance
    - global
      - skew, power and ground, repeaters, lengths, wafer scale interconnect
  - Active elements
    - Rf wireless
      - antenna, noise margin
  - Passive elements
    - mixed signal
    - sample structures

XCUT Discussions in Munich

- **Defect**
  - **Discussed defect size distribution and effect on DRAM**
- **PIDS**
  - **Contact area requirement for DRAM**
- **before leavingDesign**
  - **SOC and how to address**
  - **New materials and first year of need**
- **Packaging**
  - **Agreed to cover all wafer level interconnect/passivation and bumping**
- **Modeling and Simulation**
  - **They will include CMP models and model for across die process variability**
- **IRC**
  - **What is MPU half pitch?**

Table 31 Difficult Challenges > 100 nm, rev. 1/99

Five Difficult Challenges ∨>100 nm / Before 2005	**Summary of Issues**
Chip Reliability	New materials and architecture (copper, low κ, damascene) create some chip reliability exposure. Detecting, testing, modeling and control of new failure mechanisms will be key.
Process Integration	Integrating new materials such as copper, low k, high k, ferroelectrics, etc., into process flows with low cost, high yield, acceptable reliability and contamination control,will be challenging.
Barriers/seed/low κ dielectric materials	Barrier and seedmaterials that address the electrical, mechanical and thermal issues with copper/ low κ.
Dimensional control	Three dimensional control of critical feature size and multi-layer film thicknesses is an increasingly important predictor for circuit performance and reliability. Improved metrology, *in situ* process control, CAD techniques and modeling are needed.
BEOL process with low/no FEOL** impact	As feature sizes shrink, BEOL*** processes must be compatible with FEOL roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.

Table 31 Difficult Challenges . 100 nm, rev. 1/99

Five Difficult Challenges < 100 nm / Beyond 2005	**Summary of Issues**
Dimensional control and size effects	Improved metrology, *in situ* process control and CAD techniques are needed. Microstructural and electron transport effects become important for 3D control.
Aspect ratios for fill and etch	As features shrink, etching and filling high aspect ratio structures will be challenging, especially for DRAM. Dual damascene metal structures are also expected to be difficult.
New materials	In order to take advantage of the low resistivity and dielectric constant targets, new materials or processes must be developed. New materials are also required for system-on-a-chip needs.
Solutions after copper and low κ	Copper and low k materials will be used for many generations. Innovations which include design and packaging enhancements or the use of rf/optical interconnect are necessary to meet future performance requirements.
BEOL process with low/no FEOL** impact	As feature sizes shrink, BEOL*** processes must be compatible with FEOL roadmaps. Low plasma damage, contamination and thermal budgets are key concerns.

Technology Requirements 1998

	1997 *250 nm*	*1999* *180 nm*	*2002* *130 nm*	*2005* *100 nm*	*2008* *70 nm*	*2011* *50 nm*	*2013* *35 nm*
Number of metal levels - DRAM	**2 - 3**	**3**	**3**	**3 - 4**	**3 - 4**	**4**	**4**
Number of metal levels - Logic	**6**	**6 - 7**	**7**	**7 - 8**	**8 - 9**	**9**	**9**
Maximum interconnect length - Logic (meters/chip)	**800**	**1,700**	**3300**	**5000**	**9200**	**17,000**	**24,000**
Reliability - Logic (FITS/meter) X10^{-3}	**4.9**	**1.5**	**0.8**	**0.5**	**0.3**	**0.1**	**0.1**
Planarity requirements within litho field for minimum interconnect CD (nm)	**300**	**250**	**200**	**175**	**175**	**175**	**175**
Minimum contacted/non-contacted interconnect pitch - DRAM (nm)	**550/500**	**400/360**	**280/260**	**220/200**	**160/140**	**110/100**	**110/100**
Minimum contacted/non-contacted interconnect pitch - LOGIC (nm)	**640/590**	**460/420**	**340/360**	**260/240**	**190/170**	**140/130**	**140/130**
Minimum metal CD (nm)**	**250**	**180**	**130**	**100**	**70**	**50**	**35**
Minimum contact/via CD (nm)	**280/360**	**200/260**	**170/210**	**140/180**	**110/140**	**80/100**	**60/70**
Metal height/width aspect ratio - LOGIC (µP)	**1.8**	**1.8****	**2.1****	**2.4****	**2.7****	**3.0****	**3.0****
Via aspect ratio - LOGIC	**2.2**	**2.2****	**2.4****	**2.5****	**2.7****	**2.9****	**3.2****
Contact aspect ratio - DRAM using tungsten	**5.5**	**6.3**	**7.5**	**9**	**10.5**	**12**	**’12**
Minimum metal effective resistivity (µΩ–cm)	**3.3**	**2.2**	**2.2**	**2.2**	**2.2**	**< 1.8**	**< 1.8**
Barrier/cladding thickness (nm)	**100**	**23**	**16**	**11**	**3**	**1**	**0**
Minimum Interlevel metal insulator; effective dielectric constant (k)	**3.0 - 4.1**	**2.5 - 4.1**	**2.0 - 2.5**	**1.5 - 2.0**	**< 1.5**	**< 1.5**	**< 1.5**

**Minimum CD for isolated lines (no contacts or vias)

Work in Progress DRAFT ONLY: Not for Publication

Table 32 MPU Interconnect Technology Requirements Rev 4/13/99								
Year of First Product Shipment Technology Generation	1999	2001	2003	2005	2007	2009	2011	2013
MPU 1/2 Pitch	210	160	140	115	90	55	45	
MPU Gate	140	100	70	50	35	25	18	
Number of metal levels	6–7	7–8	7–8	8–9	9-10	10-11	11-12	12-13
Number of optional levels - groundplanes	2	2	2	2	2	2	2	2
Jmax (A)/cm2 - wire	6E5							
Jmax (mA) - via	0.36							
Local pitch (nm)	500	400	320	255	205	165	130	105
Local A/R (for Al)	2	2.1	2.2					
Local A/R (for Cu)	1.4	1.5	1.6	1.7	1.8	2	2.1	2.2

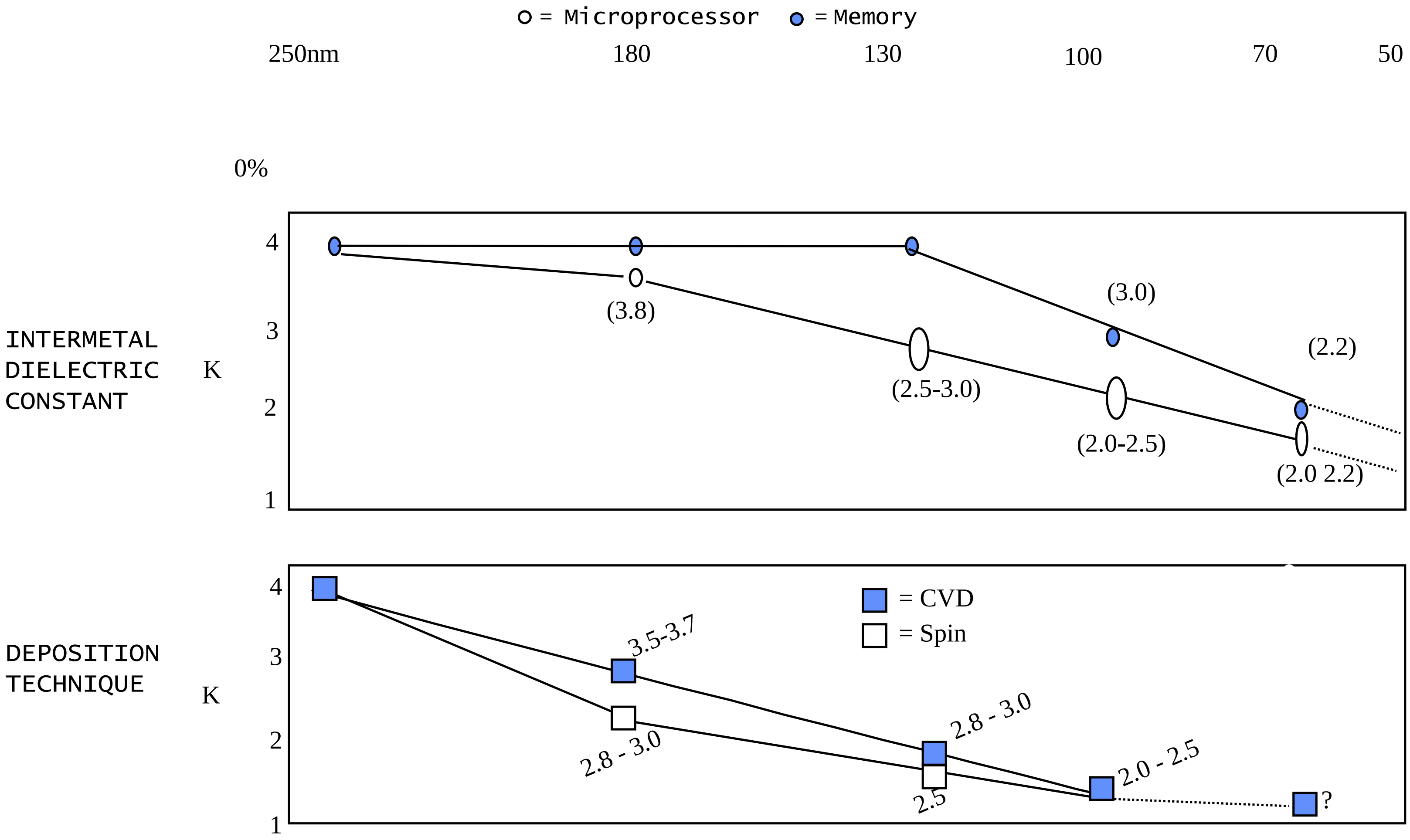
Year of First Product Shipment Technology Generation	1999	2001	2003	2005	2007	2009	2011	2013
Intermediate level(s) pitch (nm)	640	510	410	330	260	210	170	135
Intermediate level(s) A/R (Al)	2.2	2.4	2.6					
Intermediate level(s) dual damascene A/R (Cu)	3.3	3.5	3.6	3.8	4,0	4.3	4.5	4.7
Minimum pitch global level(s) (nm)	1050	840	670	540	430	345	275	220
Global level(s) A/R (Al)	2	2.2	2.4					
Global level(s) A/R (Cu)	1.5	1.7	1.8	2	2.2	2.5	2.7	2.9
Minimum metal effective resistivity (μΩ-cm) Al wiring *	3.3	3.3	3.3					
Minimum metal effective resistivity (μΩ-cm) Cu wiring *	2.2	2.2	2.2	2.2	1.8	≤ 1.8	≤ 1.8	≤ 1.8
Barrier/cladding thickness conformal (nm)	23	16	11	3	0	0	0	0
Minimum interlevel metal insulator—effective dielectric constant (k)	3.5-4.1	2.7-3.5	2.2-2.7	1.6-2.2	1.5	≤ 1.5	≤ 1.5	

Table 32 DRAM Interconnect Technology Requirements Rev 4/13/99

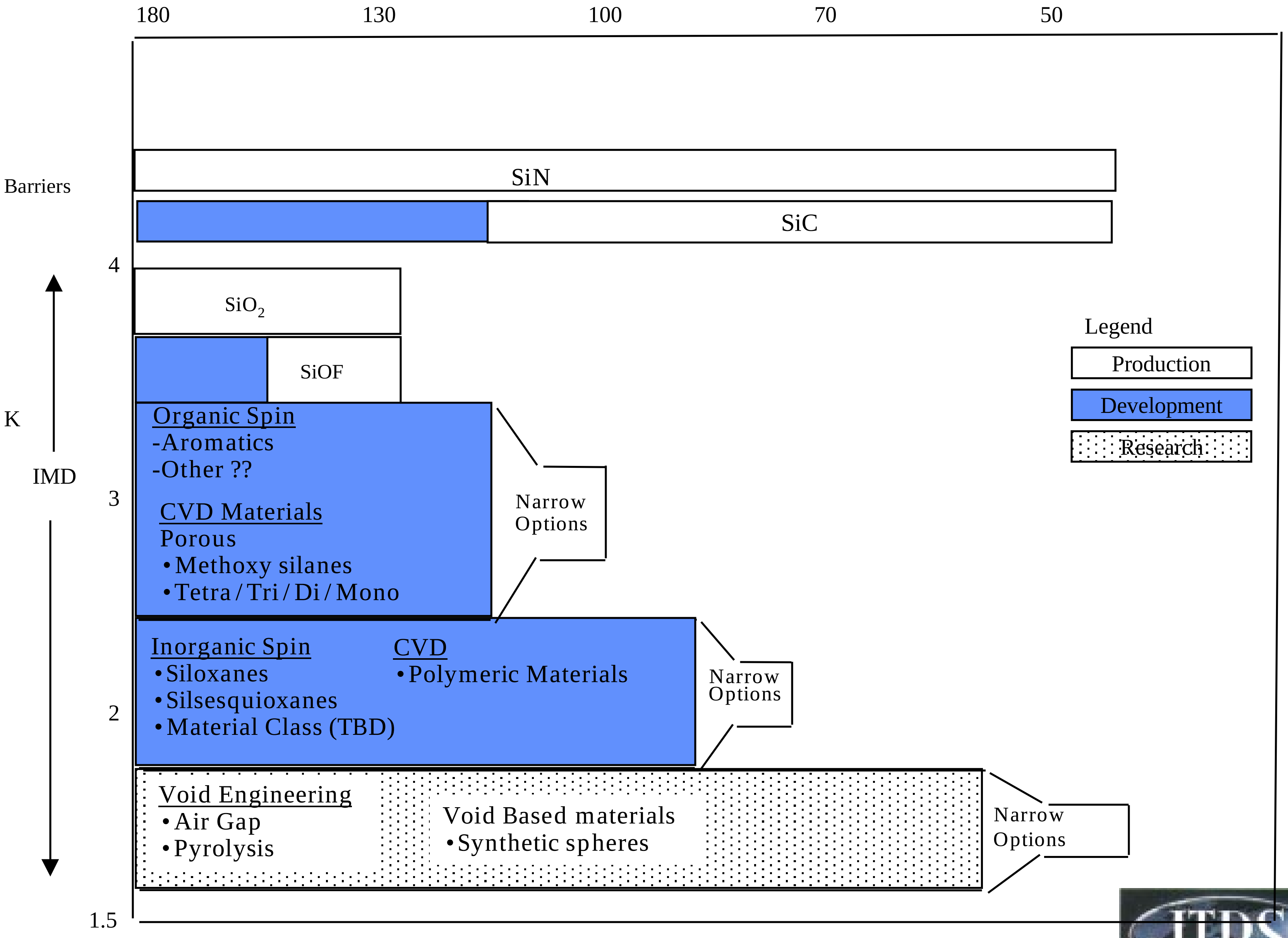
Year of First Product Shipment Technology Generation	1999	2002	2005	2008	2011	2014
DRAM 1/2 Pitch	180	130	100	70	50	35
Number of metal levels	3	3-4	3-4	4	4	4
Contact A/R - stacked capacitor	6.3	7.5	9	10.5	12	13.5
Local pitch (nm) - non contacted	360	260	200	140	100	70
M1 A/R						
Specific contact resistance						
Specific via resistance						
Metal effective resistivity	3.3	3.3	2.2	2.2	<1.8	<1.8
Minimum interlevel metal insulator—effective dielectric constant (k)	4.1	3.0 - 4.1	2.5 - 3.0	2.0 – 2.5	1.5 – 2.0	<1.5

Table 32 SOC Interconnect Technology Requirements Rev 4/13/99								
Year of First Product Shipment Technology Generation	1999	2001	2003	2005	2007	2009	2011	2013
MPU 1/2 Pitch	210	160	140	115	90	70	55	45
MPU Gate	140	100	70	50	35	25	18	
Number of metal levels	6	7	7–8	8	8	9-10	10	11
Number of optional levels - passive elements	0	2	4	4	6	6	6	6
Jmax (A)/cm2 - wire	3E5							
Jmax (mA) - via	0.36							
M1 pitch (nm)	450	360	290	230	185	150	120	95
M1 A/R (for Al)	2	2.1	2.2					
M1 A/R (for Cu)	1.4	1.5	1.6	1.7	1.8	2	2.1	2.2
M2-[M(n)-1] pitch (nm)	560	450	360	285	230	185	145	120
M2-[M(n)-1] A/R (Al)	2.2	2.4	2.6					
M2-[M(n)-1] A/R (Cu)	1.6	1.7	1.8					
Via A/R (Al)	2.8	2.9	3					
Dual damascene A/R (Cu)	3.3	3.5	3.6	3.8	4	4.3	4.5	4.7
Minimum pitch global level(s) (nm)	900	720	580	460	370	300	340	190
Global level(s) A/R (Al)	2.2	2.4	2.6					
Global level(s) A/R (Cu)	1.6	1.7	1.8					
Global level(s) dual damascene A/R (Cu)	3.3	3.5	3.6	3.8	4	4.3	4.5	4.7
Process control metric								
Xtalk metric								
Minimum interlevel metal insulator—effective dielectric constant (k)	3.5-4.1	2.7-3.5	2.2-2.7	1.6-2.2	1.5	≤ 1.5	≤ 1.5	

DRAFT -- DIELECTRIC ROADMAP



Dielectric Materials



180 130 100 70 50

Barriers

SiN

SiC

K

IMD

4

3

2

1.5

SiO_2

SiOF

Organic Spin
-Aromatics
-Other ??

CVD Materials
Porous
- Methoxy silanes
- Tetra / Tri / Di / Mono

Narrow Options

Inorganic Spin
- Siloxanes
- Silsesquioxanes
- Material Class (TBD)

CVD
- Polymeric Materials

Narrow Options

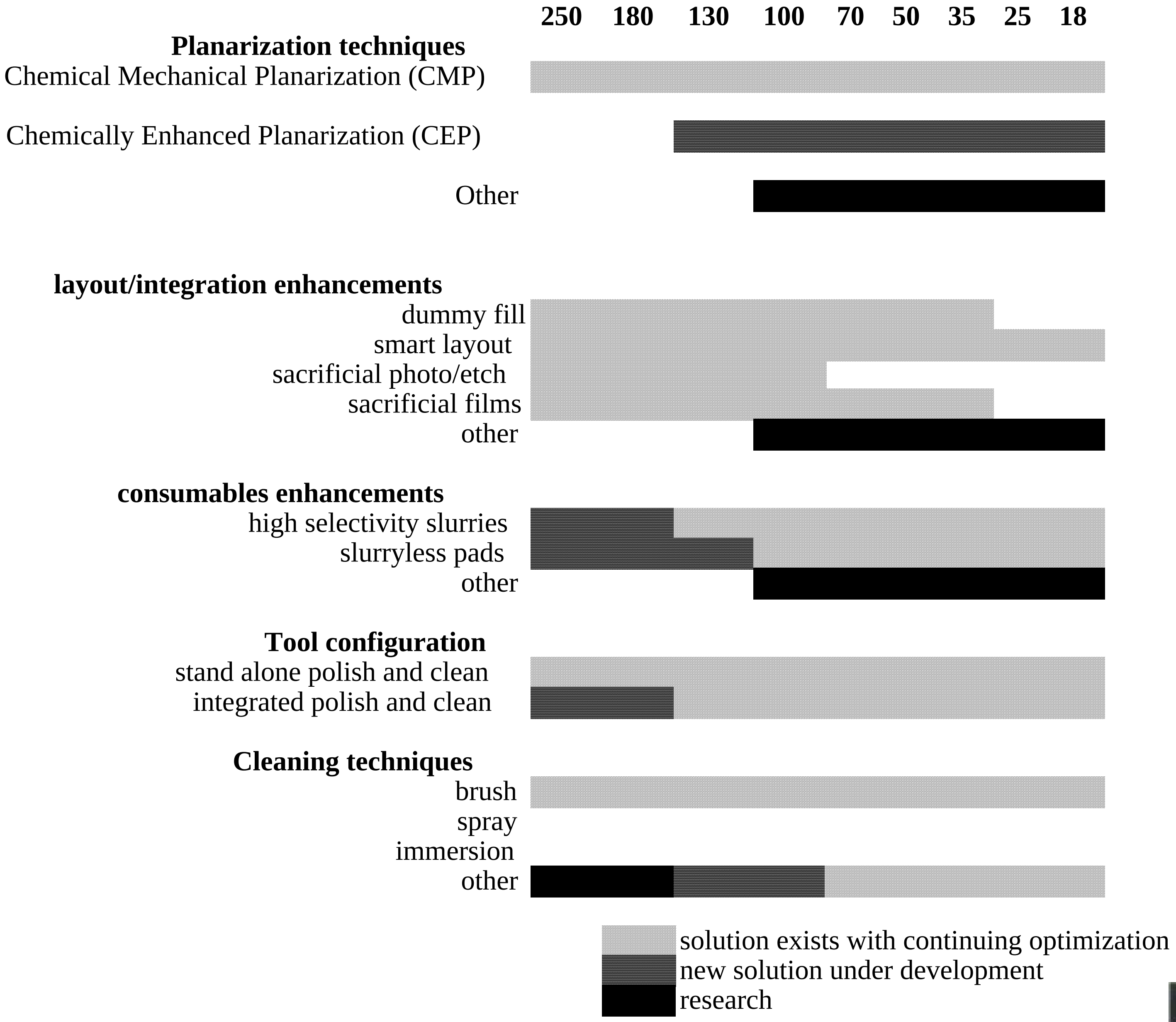
Void Engineering
- Air Gap
- Pyrolysis

Void Based materials
- Synthetic spheres

Narrow Options

Legend

☐	Production
■	Development
▨	Research



250 180 130 100 70 50 35 25 18

Planarization techniques

Chemical Mechanical Planarization (CMP)

Chemically Enhanced Planarization (CEP)

Other

layout/integration enhancements

dummy fill
smart layout
sacrificial photo/etch
sacrificial films
other

consumables enhancements

high selectivity slurries
slurryless pads
other

Tool configuration

stand alone polish and clean
integrated polish and clean

Cleaning techniques

brush
spray
immersion
other

░ solution exists with continuing optimization
▒ new solution under development
■ research

Short Term Plan

- Tables with changes distributed by 23 April 1999 to all regions
- Europe to provide white paper input on EM
- Prepare packaging text with A&P
- Identify gap-fill versus low k trade-offs for DRAM
- Japan - require calculate current limits for “latest” tables and design rules and specific contact and via resistance
- 12 May 1999 - 4 site video/multi telecon all regions
- Text drafts at IITC 27 May 1999 San Francisco - face to face plus telecon