

International Technology Roadmap for Semiconductors

FEP ITWG Update

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>70 nm

- 1) Gate Stack (Nitride)**
- 2) DRAM Storage Cell**
- 3) USJ with Std Processing**
- 4) L_{eff} CD Control**
- 5) Metrology**

≤ 70 nm

- 1) Gate Stack (High-K, Metal Electrode)**
- 2) Memory Storage Cell**
- 3) Transistor Structure**
- 4) Si Compatible Materials**
- 5) Metrology**

ITWG Crosscut Interface

Metrology: Thickness, CV, Dopants, Contaminates

ESH: New Materials, Pb Issue, Table Inputs

Factory Integration: No show.

PIDS: Gate Stack @70nm, Memory Strategy

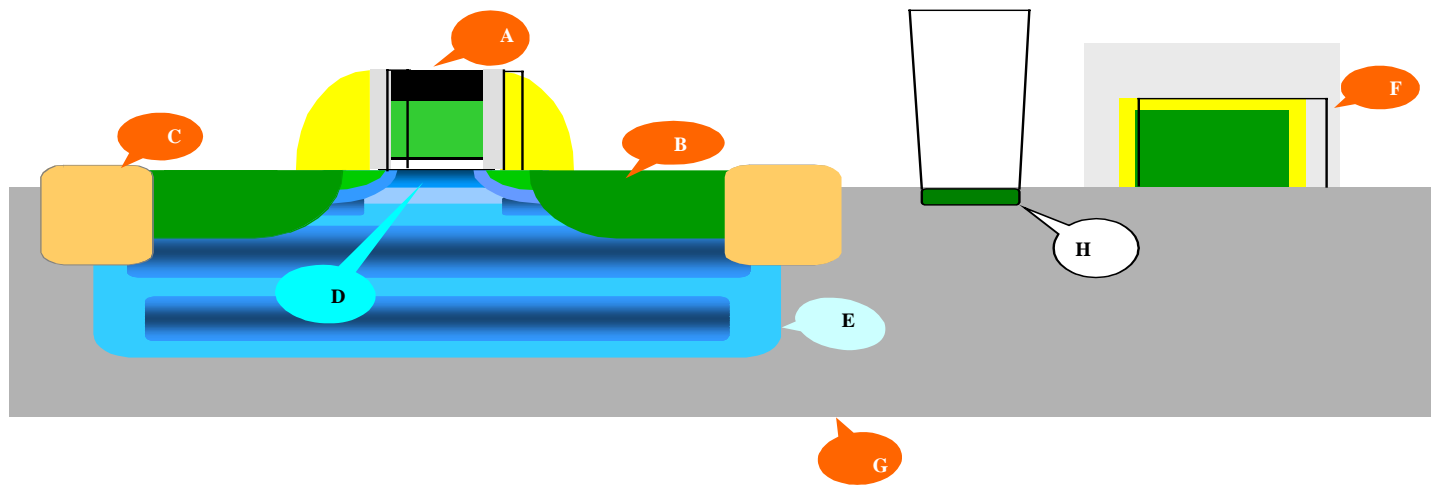
FRONT END PROCESSES

SCOPE

The Front End Processes (FEP) Roadmap was developed with a focus on high performance transistor structures appropriate for both memory and logic product types. The intent of this Roadmap is to define comprehensive, integrated solutions for the key technology areas in the front-end-of-line (FEOL) wafer fabrication processing of integrated circuits. Hence, the Roadmap includes the tools and processes utilized from the starting silicon wafer through the silicidation process. These specific technology areas are covered: *Starting Materials, Surface Preparation, Thermal/Thin Films and Doping, and Front End Plasma Etch.*

A presentation of the requirements and potential solutions is provided for each technology area. The targets and trends shown in the requirements tables are model-based unless otherwise noted. Potential solutions are known examples of possible solutions, however, they are not to be considered the only approaches; innovative, novel solutions are sought.

Related topics for front end processes are presented in other sections of this Roadmap. The tool-related issues for plasma etch and chemical mechanical polish (CMP) for trench isolation are delineated in the *Interconnect* section rather than in this FEP section because of their overlap with back-end-of-line (BEOL) tool issues. The FEP roadmap includes the processing issues as well as future requirements for plasma etch and CMP processing related to FEOL device fabrication. The crosscut needs of FEP are covered in the following sections: *Defect Reduction; Metrology; Environment, Safety, & Health; and Modeling & Simulation.*



A : Gate Stack	B : Source/Drain - Extension	C : Isolation	D : Channel
E : Wells	F : Capacitor Stack/Trench	G : Starting Material	H : Contacts

Table 22a Thermal/Thin Films, Gate Etch, and Doping Technology Requirements for Logic

Year of First Product Shipment Technology Generation (λ)	1999 180 nm	2001 130 nm	2003 100 nm	2005 70 nm	2007 50 nm	2009 35 nm	2011 25 nm	2013 18 nm
Equivalent physical oxide thickness T_{ox} (nm) (A)	1.9-2.5	1.5-1.9	1.2-1.5	0.8-1.2	0.6-0.8	0.5-0.6	< 0.5	< 0.5
Gate Dielectric Leakage (A/cm ²) (B) Logic	0.7	3	4	20	28	40	55	77
Thickness control equiv phys ox thk(% 3 σ) (C)	<± 4	<± 4	<± 4	<± 4	<± 4	<± 4	<± 4	<± 4
Maximum gate dielectric loss from etch (oxide equiv nm)	0.5	0.4	0.3	0.3	0.3	0.2	0.2	0.2
Leffective Control	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
Sidewall spacer thickness (nm) Extension Structure (D)	72-144	52-104	40-60	28-56	20-40	14-28	10-20	7-14
Sidewall spacer thickness (nm) Elevated Junction (E)			20-40	14-28	10-20	7-14	5-10	3.5-7
Sidewall spacer thickness (nm) Single Drain (F)				7.5-15	5-10	3.7-7.5	2.5-5	1.8-4
Sidewall spacer thickness control (nm, 3 σ)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
Gate electrode sheet Rs (Ω/sq) (G)	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6
Gate electrode thickness (H)	144	104	80	56	40	28	20	14
Gate electrode Resistivity (μ Ohm-cm) (I)	72	54	40	28	20	14	10	7
Gate Depletion Effect on Tox (nm)	≤ 10% EOT	≤ 10% EOT	≤ 10% EOT	≤ 10% EOT	≤ 10% EOT	≤ 10% EOT	≤ 10% EOT	≤ 10% EOT
Drain extension Xj (nm) (K)	36-72	26-52	20-40	15-30	10-20	7.5-15	5-10	3.7-7.5
Silicide thickness (nm) (L)	55	35	45-70		New Structure.....			
Contact silicide sheet Rs (W/sq) (M)	2.7	4.3	2	2.7	3.8	5.4	7.5	10.7
Si/Silicide max resistivity (W-cm ²) (N)	< 6.0 x 10 ⁻⁷	< 3.0 x 10 ⁻⁷	< 2.0 x 10 ⁻⁷	< 8.0 x 10 ⁻⁸	< 3.0 x 10 ⁻⁸			
Maximum Silicon consumption (nm) (O)	50-56	34-39	63-72	56	40	28	20	14
Doping (active) @ oxide interface	1.00E+20	1.40E+20	2.3E+20	2.40E+20	3.60E+20	3.70E+20	5.00E+20	4.80E+20
Contact Xj (nm) (E)	70-140	50-100	40-80	30-55	20-40	15-35	10-19	7.5-13
Drain Extension Sheet Resistance (Ohms/square)	350-800	250-700	200-625	150-525	120-450	100-400	75-350	60-300
Drain Extension Resistivity (Ohm-cm)	1.3-6X10 ⁻³	0.6-3.5X10 ⁻³	0.4-2.5X10 ⁻³	0.2-1.6X10 ⁻³	1.2-9X10 ⁻⁴	0.8-6X10 ⁻⁴	0.4-3.5X10 ⁻⁴	0.2-2.3X10 ⁻⁴
Drain extension conc. (cm ⁻³)	1-8 x 10 ¹⁹	2-2 X 10 ²⁰	3-3.5 x 10 ²⁰	4-2.5 x 10 ²⁰	1-8 x 10 ²⁰	2-1.5 x 10 ²⁰	"silicide"	"silicide"
Extension Specific Resistance (Ohm-microns)	115-25	72-13	50-8	29-4	18-2	10.8-1.3	7-0.7	4.5-0.4
Lateral Abruptness for Source Extension (Decade/nm)	0.2	0.35	0.5	0.8	1.2	???	???	???
Extension Lateral Abruptness (nm/decade) (R)	18	13	10	7	5	3.5	2.5	1.8
Potential: Dopant Variation- Position	15 nm	2-10nm	1-7nm	1-5nm	<4nm	<3nm	<2nm	<1nm
Potential: Dopant Variation - Dose	?	?	?	?	?	?	?	?
Maximum Parasitic Resitivity (Ohm-cm ²)	6.0 x 10 ⁻⁷	3.0 x 10 ⁻⁷	2.0 x 10 ⁻⁷	8.0 x 10 ⁻⁸	3.0 x 10 ⁻⁸			
Channel conc. for Wdepletion <1/4L_{eff} (cm⁻³) (K)	2.0 x 10 ¹⁸	3.0 x 10 ¹⁸	4.0 x 10 ¹⁸	8.0 x 10 ¹⁸	1.4 x 10 ¹⁹	3 x 10 ¹⁹	> 5 x 10 ¹⁹	> 1 x 10 ²⁰
Unif. channel conc. (cm ⁻³), for V _t =0.4 (L)	6-10 x 10 ¹⁷	1-2 x 10 ¹⁸	2-3 x 10 ¹⁸	> 3.5 x 10 ¹⁸	> 7 x 10 ¹⁸	> 9 x 10 ¹⁸	> 1 x 10 ¹⁹	> 2 x 10 ¹⁹
Retrograde Channel Depth								
Channel Engineering	Halo	Pocket?						
Minimum measurable gate dielectric remaining (post gate etch clean) move to text only?	>0	>0	>0	>0	>0	>0	>0	
L _{gate} 3 σ Variation (nm) (Dense and Isolated lines) (S)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	
(A) Logic	14	10	7	5	3.5	2.5	1.8	
(B) DRAM	18	13	10	7	5	3.5	2.5	
CD bias between dense and isolated lines (T)	≤ 15%	≤ 15%	≤ 15%	≤ 10% (?)	≤ 10% (?)	≤ 7% (?)	≤ 5% (?)	
Line edge roughness	1.5-2.0 (?)	1.0-1.5 (?)	0.6-1.0 (?)	0.45-0.60 (?)	0.35-0.42 (?)	0.25-0.3 (?)	0.2-0.25 (?)	