AP TWG ATTENDEES

EUROPE

- Jean-Pierre Moscicki, ST Microelectronics
- Richard Scheuenpflug, Infineon

JAPAN

- Hisao Kasuga, NEC
- Henry Utsunomiya, MITI Consultant

US

- Chi Shih Chang, SEMATECH
- Bob Werner, SEMATECH

HIGHLIGHTS

- Region updates
- Reviewed preliminary draft
  - changes identified
  - assigned responsibilities
- Chip size
  - agreement with approach
  - will use product start and volume ramp numbers
- Flip chip pitch scaling unchanged
  - tech timing needs to be finalized (i.e., 2 years vs. 3 years)
- Wafer bumping process is a shared responsibility with Interconnect
- Very good open communications

1999 vs. 1998

- Additions
  - high performance memory packaging
  - high function hand held
  - wafer level packaging process
- Changes
  - lower cost
  - expanded mixed signal, reliability, and thermal sections