

Process Integration, Devices & Structures (PID&S)

Working Group Report Summary

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1/7/99

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General Comments:

- Node name input.

Either:

- Lithography $\frac{1}{2}$ pitch at L/S =1 or:
- No node name

- New cycle for 1999 needs to focus more on embedded and SOC Needs

1999:

- Focus on three subgroups rather than four (no short loop methodology)**

Table #15 Analog , Mixed signal, and RF Technology

This was the first year of Analog in the roadmap.

- Should emphasize embedded analog as opposed to RF.
- Inductor Q's 50 and greater red
- Should revisit noise figures.

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- Changes recommended include:

Difficult Challenges: Took out function integration at low V_{DD}
Added interconnect performance to integrated
management of power, ground, ...

Table 14 Memory and logic requirements:

- Max I_{off} was modified to be max I_{off} at nom V_{DD}
- 1999 column was made white instead of yellow
- DRAM cell size was modified to be consistent with trends

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Table 15:

- Transmit/receive frequency was modified to reflect the move to 5GHz happening sooner than expected
- Improvements to capacitor linearity were made more aggressive
- Inductor Q targets were made more aggressive
- Noise figure target was kept at 1 dB for the higher frequencies

Table 16:

- Not a requirements table; reevaluate this for the next roadmap

Should remove as a table and capture short flow needs as part of table

38 Factory Investment Risk Management, and in Defect reduction, and Modeling and simulation. TWG's

Table #17 Reliability Technology Requirement

This table need to have better Tie in with the device needs table. More work on the organization and specific device failure aspects need to be emphasized. Hot carrier effects, TDDB etc.