

**Roadmap Coordinating Group/TWG Chair Meeting
January 8, 1999**

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SEMATECH/Roadmap Information manager	Linda Wilson	linda.wilson@sematech.org
SEMATECH/Web design and development	Sarah Mangum	sarah.mangum@sematech.org

Agenda

8:00 am	Process Overview	11:30	Interconnect
8:30	ORTC Table Discussion	11:45	Factory Integration
9:00	Process Discussion	1:00 pm	Assembly and Packaging
9:30	Logistics	1:15	Environment, Safety, and Health
10:00	Break	1:30	Defect Reduction
10:15	Design	1:45	Metrology
10:30	Test	2:00	Modeling and Simulation
10:45	Process Int., Devices, Structures	2:15	Break
11:00	Front End Processes	2:30	Overall Discussion
11:15	Lithography	3:30	Adjourn

Key Points

Summary – Paolo Gargini

- We have a tentative schedule – see attached Calendar
- Goal is to be prepared by April ITRS
- Page allocation + suppliments (20 pages ITRS + 20 pages)
- Outcome of April meeting will give direction to make July success
- Teleconferences to keep focus on status
- Domestic May Workshop is face-to-face meeting
- Issue is still timing, try to make self consistent columns
- 1998 versus 1999 cycles - stay within these cycles
- Die size model needs to be corrected
- DRAM is at greater focus
- Volume production is lower die size than 3 years ago
- 60% yield targets need to be validated

Points/Comments

C. Case	Definitions and consistency checking are critical
K. Monahan	Economic considerations – we are ignoring cost implications from the acceleration of the Roadmap. Feasibility of Roadmap numbers with respect to factory cost. Economic workshop should include Roadmap TWG Chairs/ RCG members.
W. Class	Concurrent work makes information flow difficult. Dependent technologies and ccTWGs could then supply other TWGs in other years with information.
P. Percy	Need sanity check on 15-year number extrapolation
J. Canning	Chip size owners need to be identified. Lithography will participate, (ad hoc team is W. Class, B. Werner, C. Skinner, J. Canning) Also timing issue needs to be resolved before April ORTC line items and process?
A. Oscilowski	Different TWGs and timing issues must be resolved between April and July
A. Diebold	Will the Roadmap incorporate long term technology. (NGL lithography, optical interconnects) out-year innovation areas to pull in university
B. Joyner	SOC needs to be reflected in ORTC. Steve Hillenius needs to get involved
B. Doering	2000 Roadmap interpretation and analysis. What the roadmap represents.
A. Allan	2-year cycles product requirements will be accelerated (status of technology solution will change)
J. Jewitt	Shift from political and government to technology drivers will be challenge for ESH. Will need support
L. Novak	Need pressure on people to commit to participate. Need pressure from RCG.
D. Mehta	Needs Roadmap must be emphasized rather than fixed technology set. Emphasis on opportunity where red is.
J. Hutchby	Need business inputs to define mechanism to identify business factors
J. Harlow	Increasing functionality versus lower power becomes dominant. Certain factors must be recognized. Assumptions of numbers annotations in data is useful
C. Skinner	Reimbursement for professorship needs to be addressed. Will send estimate of Factory Integration TWG needs
W. Class	RCG might benefit by priority of readership (suppliers, university, industry and government is readership priority)
L. Wilson	Need presentations. Needs feedback on electronic media. TWG web sites.

Action Items

All

- All to review calendar and communicate conflicts
- Review ORTC numbers carefully

TWGs/RCG

- Items to be sent to Linda Wilson
 1. 01/08 electronic copies of presentations
 2. Memberships
 3. Designated TWG writers
 4. Designated contact person for edits
- Finalize tables and send by January 11 ** (this has been extended)
- Communicate with their ITWG counterparts
- Select liaisons for other TWGs
- Need new Modeling and Simulation co-chair
- Factory Int. TWG to send estimate on FI TWG needs for reimbursement
- TWGs who want a website to contact Sarah Mangum

RCG

- RCG advocates need to be selected
- Policy on memberships/duties needs to be sent by RCG to TWGs
- Introductory section writers need to be identified

Paolo Gargini

- Contact Siemens regarding meeting in Munich, Alex O. to follow-up
- Present 1998 Roadmap to SIA with cover statement to approve

Alan Allan

- ORTC tables need to be color coded
- Send ORTC tables to Linda Wilson
- Alan Allan to initiate die size task force

Linda Wilson

- Send format to TWG chairs by January 22, along with instructions and standards for publication
- Send publication schedule details for edit sessions/web postings of drafts/prereading
- 1998 Roadmap tables / figures posted to web by January 22 ** (this has been extended)
- Detail supplementary material and send to RCG/TWG
- Add web sites for Interconnect, Front End Processes, Lithography, maybe Defect Reduction (Sarah)
- Address frameset issue with display (Sarah)

Open Issues

- Timing / Technology nodes for 1999 needs to be discussed/debated/decided before April
- Non-extrapolated items need to be resolved - chip size, wafer diameter years, etc.
- Need note on Technology Requirements for manufacturing tool timing
- Introduction of DRAM, ASIC, MPU needs to be resolved
- Domestic Roadmap Workshop dates need to be set, location, invitees, logistics
- ASIC versus SOC needs to be resolved
- Need details for Technology Requirements and Potential Solutions

Calendar

January 15	All 1998 tables posted to web sites**
January 22	1999 ITRS format sent to TWG chairs and posted for downloading on web
Feb - Apr	Rewrite of 1999 ITRS sections by TWGs
April	SIA Approved 1998 tables posted publicly to world
April 12 - 15	ITRS meeting to review draft of sections with ITWG members (location/dates TBD, Munich is proposed) Manuscript draft 1 is then compiled
May - June	Update of all TWG sections compiled / presented at Int'l Roadmap Workshop
July 8 - 9	International Roadmap Workshop (location TBD, San Francisco proposed) Manuscript draft 2 is then compiled, includes Introduction sections by RCG/IRC
September	Content is approved and frozen
October	Document/CD is produced
November	ITRS is distributed
December	Roadmap presentations begin (SEMICON Japan, IEDM, other)

Schedule for RCG/TWG teleconferences for 1999

- March 26 before NTRS SRC and ITRS meeting in April
- June 21-25 before ITRS meeting in July (date to be decided based on feedback)
- August 16-20 before final approval (date to be decided based on feedback)
- Sept 7-10 before freezing document (date to be decided based on feedback)

*** this has been extended*

Meeting Notes - Detailed

Process Overview, Process Discussion - Paolo Gargini

The ITRS meeting was summarized, highlighting the following

1. Timing / technology nodes for the 1998 and 1999 roadmaps
 - The ITRS is a 15-year Roadmap, so continue table trendout that duration
 - 1998 Cycle
 - Summary of Technology Cycle from 3 years to 2 years
 - 1998 timing moved up by one year
 - DRAM 1/2 pitch 1999 - 180, 2002 - 130, 2005 - 100, 2008 - 70
 - Logic Isol Line** 1999 - 140, 2002 - 100, 2005 - 70, 2008 - 50
 - **note: same as gate length*
 - 1999 Cycle
 - DRAM 1/2 pitch 1999 - 180, 2001 - 130, 2003 - 100, 2005 - 70, 2007 - 50, 2009 - 35, 2011 - , 2013 - , 2015 - ,
 - Logic 1/2 Pitch 1999 - 180, 2001 - 150, 2003 - 115, 2005 - 80, 2007 - 55, 2009 - 40, 2011 - , 2013 - , 2015 -
 - L Isol Line** 1999 - 140, 2001 - 100, 2003 - 70, 2005 - 50, 2007 - 35, 2009 - 25, 2011 - , 2013 - , 2015 -
 - **note: same as gate length*
 - Feedback:
 - Introduction of DRAM, ASIC, MPU needs to be resolved
 - Logic should be called MPU
2. 1998 Roadmap release to the public in 2Q99
 - The electronic document will state the International Technology Roadmap for Semiconductors is "1998 Revision Sponsored by SIA with Support from the EIAJ, EECA, TSAI, KSIA"
 - Will contain all tables, figures, and executive summary introduction**
 - Contributors from each region will be included
 - It will exist as paperback to send to constituency to approve
 - Actual copy will be electronic on the web only
 - Posted to web by April
3. 1999 Calendar
 - ITRS ITWG meeting in April 12-16
 - held in Munich
 - actual days will be announced soon
 - International Roadmap workshop on July 8-9
 - the schedule of TWG tasks for 1999
 - set to meet the distribution deadline in November 1999
 - April ITRS meeting must have TWG sections ready for review by ITWGs
 - international commitment and response must be encouraged
 - approval of reviews must be followed up by DTWGs to achieve best consensus
 - a proposed USA-only domestic Roadmap Workshop in May
 - feedback was positive
 - Proposed date is the week before Memorial Day 1999
 - Proposed location was San Francisco during the International Interconnect Conference
 - Schedule for RCG/TWG teleconferences for 1999
 - March 26 before NTRS SRC and ITRS meeting in April
 - June 21-25 before ITRS meeting in July
 - August 16-20 before final approval
 - Sept 7-10 before freezing document
4. Policy and Organizations
 - Overall policy for memberships needs to be updated and resent to RCG and TWGs
 - TWG groups (both Focus and Cross Cut) were approved

- 1999 TWGs are the same as 1998
 - TWG need to identify delegate (s) as primary writer (s) of materials for sections
 - Several TWGs requested liaisons from other TWGs, mainly Cross Cut contacts
 - TWGs need to communicate problems with memberships for both DTWGs and ITWGs
 - Additional TWG memberships is beneficial; memberships can be extended to add value
 - Policy for reimbursement for professors needs to be addressed
 - A public discussion group on the web was requested for feedback on 1998 tables
5. RCG Organization
- Bob Doering was ratified as new RCG co-chair to share duties with Paolo Gargini
 - RCG advocates need to be identified
 - Budget for Roadmap process needs to be understood

ORTC Discussion - Alan Allan

1. Annualized Tables

- 1998 and 1999 annualized tables were reviewed and explained with these notes:
 - self-consistent numbers are modeled annually
 - some numbers as extrapolated are aggressive: etch, lithography, gate length
 - when reviewing, focus on columns for the major nodes, not the annualized years
 - data numbers remain essentially the same, but years may change to pull in by 1 year at least through 2003 to a 2-year cycle. For symmetry and to stay on trend, the table stays as 2-year cycle.
 - Proposed 1999 2-years needs to be studied
 - there will be non-extrapolated numbers, e.g., wafer diameter at 450/2009
 - ASIC is still ASIC, not System on Chip (SOC)
 - Year of 1st Production Shipment is based on volume production (hard tool set) – full flow.
 - Logic ½ pitch is not included on tables
 - Consensus extends only to 2007 because that is where 2012 numbers were pulled into
- DRAM ½ Pitch chart is an example of line item to show validation and trend chart
- If TWGs have models and algorithms to build extrapolations for ORTC line items, please send to Alan Allan
- Moore's law is still being assumed (bits on a chip doubles every 3 years)

2. Feedback and suggestions

- Roadmap purpose is to show where showstoppers occur that could depart from Moore's law.
- Issues with Moore's law are more economic. Meindl's extrapolation of today's technology, "Meindl's law," the physical limitations level off/depart from the trend.
- Lithography presented a graphic of Average Minimum Feature Size Past/Future shows device limits, material limits, SIA 1999 proposal, fundamental limits as trended
- Supplier sensitivity demands issues of significance: 300 mm (wafer diameter), die size, etc.
- The previous Roadmaps did not have space for data generation discussion.
- Best guess/experience may not be valid and is risky.
- Suggestions were to
 - review / compare Meindl's extrapolation with ORTC extrapolation model
 - identify a group (i.e., Design, PIDS, Factory Integ., Lithography, and /or Assembly and Packaging, Alan Allan) to review density and feature size with respect to fundamental limits to compare the Roadmap timeframe and numbers.
 - add a discussion of Moore's law and fundamental limits and how this compares with the identified needs in the Roadmap in the Introduction
 - color code the ORTC tables
 - supplementary material / appendix for TWGs to describe/support data generation

Logistics - Linda Wilson

1. Publication will be electronic media (online on web and as a CD-ROM), accompanied by an Introductory section

- Electronic media allows links to supplementary supporting material
 - Supplements not to exceed 20 items (tables, figures, or total pages)
 - Will be described / discussed thoroughly
2. 1997 format for publication will be used
 3. Sections for TWG sections are as 1997 document
 - Introductory sections are
 - Introduction
 - International Considerations
 - Purpose/Objective of Semiconductor Technology Forecasting
 - Grand Challenges Update
 - Overall Technology Characteristics
 - Summary of Technology Sections
 - TWG sections are
 - Scope
 - Difficult Challenges
 - Use Standard Table like 1997
 - *Near and Out-Year nodes / years need to be determined*
 - 5 Challenges ³ 70nm/ Before 2005 / < 70 nm/ Beyond 2005
 - Technology Requirements
 - Use Standard Table like 1997
 - *Year of First Chip/Product Shipment/Technology Generation*
 - Allowance for figures
 - Potential Solutions
 - Use Standard Figures like 1997
 - Allowance for other figures
 - Appendix
 - Contributors
 - Overall Technology Characteristic Tables
 - Definitions of ORTC drivers
 - Glossary of Acronyms and Terms
 4. Page allocation for each TWG section of the Roadmap (not counting supplementary material) is 20 pages for Focus TWGs, 15 pages for CrossCut TWGs
 - Cross Cuts may submit a paragraph to a Focus TWG section, summarizing needs particular to that FTWG, and then link back to the main CCTWG section
 5. Electronic format will be sent January 22 to all TWGs and be downloadable from the web
 - Versions will be in Word 6.0
 - Figures will be in Powerpoint and copied into Word document
 - If tables are constructed in Excel, TWGs to copy into Word as Word tables
 6. Publication schedule is aggressive, but allows several draft versions with reviews
 - TWG sections writing scheduled for 1Q99
 - Draft manuscript scheduled to be assembled after ITRS meeting in April.
 - Drafts and edits scheduled for 2Q-3Q
 - Publishing and distribution scheduled for 4Q

Suggestions/Feedback

- writers need to be identified now
- quantify mbytes for CD-ROM as a budget for supplemental materials
- potential solutions should extend a minimum of 1 year

TWG Key Messages (*presentations are needed so they can be posted...*)

Design – Bill Joyner

Membership – Writers are identified

Focus Topics are the same as 1997

ITWG Newton and Schultz

Status discussed

ISSCC Feb 17

TWG meeting ITWG involved

DTWG will write sections

Changes from the 1997 NTRS

economics and end results change drivers and line items (ASIC to SOC)

liaisons have been appointed to communicate with other TWGs

PIDS – Steve Hillenius

Contributors have been identified

most Value from 1997 Memory and Logic, and Analog, Mixed Signal & RF

Analog needs to be integrated more fully in the Roadmap (SOC)

Short flow should be eliminated

do not want to be too inclusive, needs to be focused on specific priorities

Reliability

Memory and Logic

Analog, Mixed Signal & RF

Front End Processes – Walter Class

Memberships with writers and sub-TWG chairs

Etch

Surface Prep

Doping

Thermal/Thin Films

Starting Mater

Device, Integration Modeling

Issue of importance to come to closure as to what will appear in Tech, Req's and Potential Sols.

sub-TWGs will meet on definitions of new line items along with ITWG input

by April 16 will have tables set, by July will have section draft

Overview of ITRS Meeting Accomplishments

1998/1999 Action Items for Tables 19-22

Other TWG coordination is needed, especially PIDS

T20 Litho, PIDS, Metrology, T21 - ORTC, T22 - PIDS, Litho

Issues requiring coordination

ORTC revisit chip size (1.3x multiplier versus 1.4x)

logic isolated length is equal to physical gate length

die size and manufactured product needs definitions

Litho

gate length printed versus physical gate length – physical gate length is actual driver for FEP

Litho does printed versus etched gate

final physical gate length and budget analysis

number for Roadmap is printed gate length

issues requiring actions are Metrology and PIDS

Lithography - John Canning

Overall Characteristic table

Chip size is too large and drives ;suppliers in the wrong directions and sends R&D down wrong solution set

Suppliers for mask (reticle) and steppers in the wrong direction

Timing cycle of Roadmap

Cost of Ownership Analysis

What is mainstream production - this group needs to decide. Lithography is willing to work on die size.

Timing

do we maintain or accelerate Moore's law
 is the process a consensus building process or directive from RCG?
 Litho overwhelming supports 3-year cycle
 See no path/way to accelerate long term goals
 Need resolution before April
 No numbers and no dates is non-relevant
 FEP seconds this- Suppliers cannot respond to pull – in of years

Interconnect – Chris Case

Members

Issue: how to incorporate DRAM specific challenges
 New materials incorporation is not easily integrated
 Issues – see slides
 Table 32 clarify all computations behind numbers
 Section addressing this will be entirely rewritten ...
 1999 issues not addressed in 1998 were presented

Factory Integration – Court Skinner

FITWG transition

Membership

Web site

Mission statement

Meetings are once a month through September

Difficult Challenges need to be more specific

see slide...

Assembly and Packaging – Bob Werner

RAMBUS and SLDRAM is going to be addressed in 1999

high function handheld – Japan will give metrics

technology strength and emphasis

Issues

memory chip size too large in 1997

chip signal pads not accessible (pad pitch and probe pitch)

SOC – who owns definition of SOC?

technology acceleration on pad/pin count, pad pitch,

curve on lifecycle of chip sizes – need to take close look/ describe chip size (where in life cycle for what chip size)

see slide....

need owners for chip size and SOC

ESH – Larry Novak

Calendar and membership is set

reached consensus quickly in 1998

particular issues are agreed upon

US and Japan

ESH needs representatives/liasons to coordinate with FTWGs, attend meetings

ESH will send by 1/19 the ESH contacts to the FTWGs

Table 53 to tie ESH issues to tech node

Defect Reduction – David Jensen

Focus Topics will be the same based on yield learning

supplemental material is available on web
 Calendar is aggressive but will try to meet
 ITWG representatives are still be assembled
 Need 1st and 3rd year yield targets (probe yields of 60% and 80%, 1997, e.g.) by FTWGs
 Japan requested more DRAM information
 Table 56 - add table or conversion for DRAM with consideration for repairs

Metrology – Alain Diebold

Meetings start in March

Adding members,

ITWG meeting 1998 update to Tech Requi and Diff. Challenges

Statistical limits of sub-100nm process control in difficult challenges and textually

Correlation between electrical and physical

Evolution towards sensor-based process control in 1999 is slowed down, emphasis has diminished since 1997, so focus will be lessened

Cost and productivity is the reason (W. Class)

Perception of reality versus perception of need (D. Jensen)

Automation complexity versus operation compatability

P/T ratios on smaller architectures

Needs crossfunctional participation – send tables and send meeting announcements

Modeling and Simulation – Paco Leon

ITRS meeting went well

need new co-chair to replace Ron Goossens

Issues

Origin of technology Requirements numbers should be document (suggested as annotation on each line item)

Coverage of non-logic devices

More coverage of compact circuit

Refinement of tables...see slide

Modeling of future technologies would be provided by SRC/SEMATECH to build consistency into roadmap tables