

December 10, 1998 FEP ITWG  
Meeting Summary

# **FEP ITWG Meeting Participants**

- Seiichiro Kawamura- Fujitsu
- Bernd Vollmer -Siemens
- Hong-Hsiang Tsai- Winbond
- Rinn Cleavelin- TI/Sematech
- Walter Class- Eaton Corp.

# Fulfillment of Meeting Expectations

- Review and Understand Charts or your ITWG-OK
  - Highly compressed roadmap format continues to create misunderstanding/confusion, needs to be addressed in 1999
- Identify agreements & Issues- OK
  - eight issues addressed for action on 1998 update
  - Twenty-five issues identified for action on 1999 ITRS
  - Identified coordination needs with Litho, PIDS, ORTC and Metrology

# Fulfillment of Meeting Expectations

- List issues and begin the discussion-OK
- Plan for future resolution of the Issues-OK
  - Draft 1999 Roadmap time table has been prepared which defines interaction points between DTWG and ITWG's
- Identify technology node components independent of timing- OK
- Begin to Address Timing- OK
  - One major issue associated with new proposed 2-year timing

# Overview of Meeting Accomplishments

Table Number	1998 Action Items	1999 Action Items	Other TWG Coordination
19	0	2	None
20	3	9	Litho, PIDS, Metrology
21	3	9	ORTC
22	2	5	PIDS, Litho

Suggestion: All TWGS should institute a system of revision numbering and control to assure that correct table updates are posted to the Web site.

# Highlights

- 1999 Timetable and interaction schedule underway
- Japan TWG will be preparing DRAM storage capacitor roadmap
- All ITWG's will prepare table line item suggestions and forward these to DTWG's by mid-March
- Major issue Identified associated with proposed 1999 technology node timing

## Major 1999 ITRS Timing Issue

- Technology node Compression places 100nm physical gate length devices in the year 2001
- This implies that 70nm physical gate length devices will be ready by the year 2003 having:
  - Dual metal gate structures
  - Hi-K dielectrics
  - Elevated contact structures
- Is this realistic?