

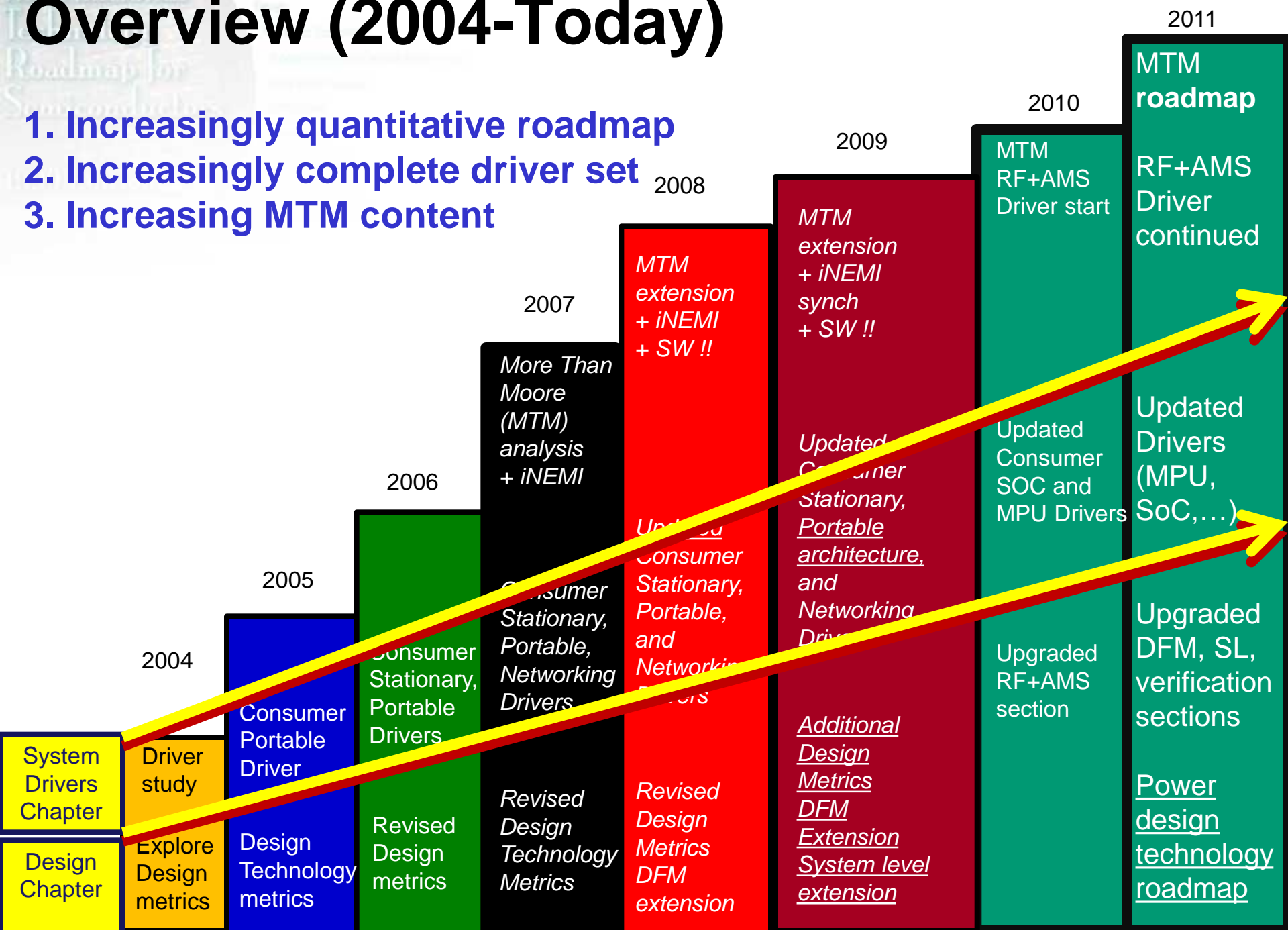
ITRS Winter Public Conference 2011

December 14, 2011
Songdo ConvensiA

ITRS Design ITWG

Overview (2004-Today)

1. Increasingly quantitative roadmap
2. Increasingly complete driver set
3. Increasing MTM content



Design / System Drivers 2011* -2012* Plans

1. Design chapter

- New power-aware design technology roadmap*
- Redefined grand challenges (long term, near term)*
- Updates to Design for Test, Verification, L/C/P sections*
- SRAM, resilience added to DFM section*
- MTM design technology roadmap*

2. System Drivers chapter

- MPU frequency roadmap revision*
- Update of AMS/RF and Embedded Memory drivers *
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3. Cross-TWG and public activity

- PIDS: reduced rate of CV/I improvement, power-aware roadmapping of main logic device families *
- Cross-ITRS : CSTN, MTM, 3D study groups *
- 2011 IEEE CANDE Workshop: Special panel on EDA Roadmap*

Updated Design Technology Grand Challenges

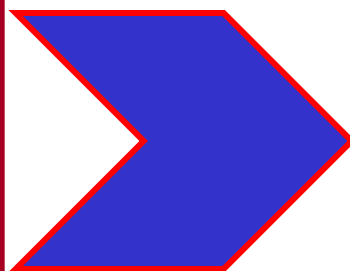
2005-2009

Near Term

- Power Management
- Design Productivity and Design for Manufacturing

Long Term

- Management of Leakage Power Consumption



2011

Near Term

- Power Management
- Design Productivity and Design for Manufacturability

Long Term

- Design of Concurrent Software
- Design for Reliability and Resilience

Power-Aware Design Technology Roadmap

<i>DT Improvement</i>	<i>Year</i>	<i>Dynamic Power Improvement (x)</i>	<i>Static Power Improvement (x)</i>	<i>Description of Improvements</i>
Software Virtual Prototype	2011	1.23	1.20	Virtualization tools to allow the programmer to develop software prior to silicon
Frequency Islands	2013	1.26	1.00	Designing blocks that operate at different frequencies
Near-Threshold Computing	2015	1.23	0.80	Lowering Vdd to 400 - 500 mV
Hardware/Software Co-Partitioning	2017	1.18	1.00	Hardware/software partitioning at the behavioral level based on power
Heterogeneous Parallel Processing (AMP)	2019	1.18	1.00	Using multiple types of processors in a parallel computing architecture
Many Core Software Development Tools	2021	1.20	1.00	Using multiple types of processors in a parallel computing architecture
Power-Aware Software	2023	1.21	1.00	Developing software using power consumption as a parameter
Asynchronous Design	2025	1.21	1.00	Non-clock driven design
Total		4.66	0.96	

Table DESN14. Power-Directed Design Technology Improvements and Their Projected Benefits

Power-Aware Design Technology Roadmap

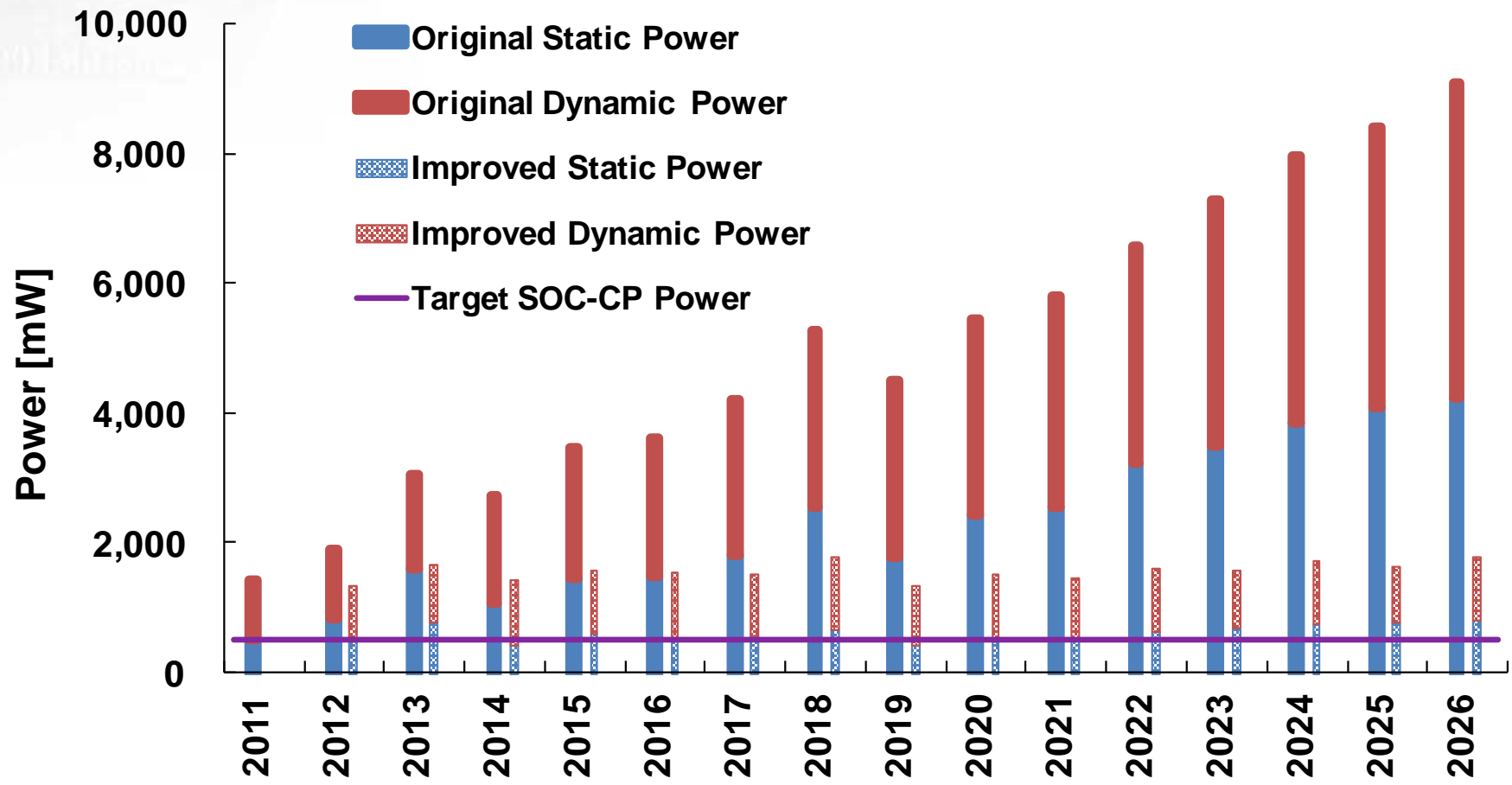


Figure DESN14. Impact of Low-Power Design Technology on SOC Consumer Portable Power Consumption

Key Challenges in Digital Verification

■ STRJ WG1 study in 2010

- Scope: HW functional verification (functional spec through RTL), high-level performance verification

■ 8 Key Problems identified

- Structure: Status, Problem, Challenges, Near-/Long-Term Solutions

Verification Strategy Planning	Optimized verification planning
	Develop expert human resource
Specification Design	Definite specification without misunderstanding
	Exhaustive extraction of to-be-verified items, and optimized verification process
	IP model preparation and quality verification
Verification Execution	High-speed simulation
	Efficient debugging
	Equivalence check for C to RTL

Example: Develop Expert Human Resource

■ Current Status (2010)

- Few engineers can develop UVM verification environment
- Many engineers can use assertions for dynamic simulation, but formal verification is too difficult for most engineers
- Training of verification engineers is local, not methodical

■ Problem Statement

- Need new skills for new methodologies such as formal verification
- Few engineers can handle many kinds of verification methodologies

■ Challenges

- Scarcity of skilled verification engineers \Rightarrow increasing TAT and declining design quality

■ Near-Term Solutions

- Implement human resources program for verification, e.g., promoting a guideline for IP verification

■ Long-Term Solutions

- System for developing verification engineers, understanding how different kinds of skills are learned, and how to measure skills

Example: Vendor IP Model Preparation and Quality Verification

■ Current Status (2010)

1. No IP guarantee quality
2. Must add testbench if not sufficiently provided by IP vendor
3. Both black-box and white-box IP distributed

■ Problem Statement

1. No system that can guarantee quality of IP
2. No standard for IP models; each IP vendor has different deliverables
3. Difficult to check quality of black-box IP

■ Challenges

1. Cannot measure quality of IP and deliverables without common quality criteria
2. Cost and time to develop additional functional models or testbenches
3. Product teams extremely nervous about quality

■ Near-Term Solutions

1. Internal IP design review
2. Internal IP quality checks
3. Make unused functions explicit

■ Long-Term Solutions

1. Institutionalize certification of standards-compliant IP quality
2. Guideline for IP deliverables (files/contents, must/should/could)

Example: Efficient Debugging

■ Current Status (2010)

- Assertions and formal verification are used
- “Schematic viewer” type debug tools are popular and widely applied. “Lint” type tools produce many pseudo-errors. \Rightarrow steady human effort is of fundamental importance

■ Problem Statement

- Assertion methods not widespread because designers are unfamiliar with methods
- Prioritizing extracted errors and how to resolve depends on skill of verification engineer

■ Challenges

- Efficiency in debugging is not improved
- Efficiency and quality of debugging varies widely depending on engineers' skills

■ Near-Term Solutions

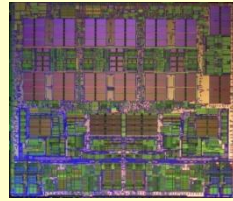
- Automated assertion tool and support by EDA vendors
- Compilation of know-how for debugging, and sharing to designers through training

■ Long-Term Solutions

- Reusable assertions as verification IP (\Rightarrow know-how can be applied by automated tools)
- Verification IP and Verification Bench must be reusable \Rightarrow faster setup of verification environment, greater debug efficiency

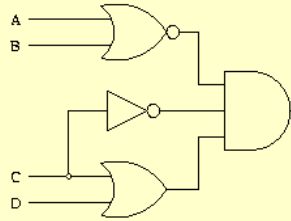
Abstractions, Methods Differ for Logic and Memory

LOGIC



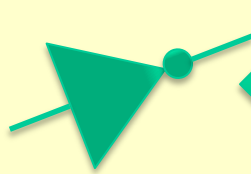
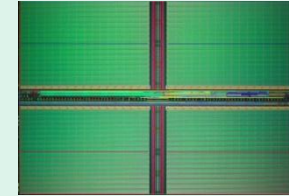
Chip

MEMORY



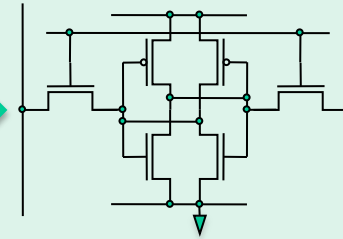
Circuit

Array



Gate

Bit Cell

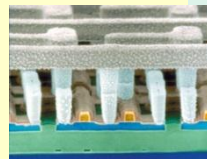


Device

- *Gate-level timing, power models*
- *Static “signoff”*



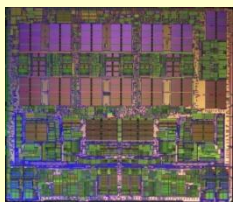
Physical



- *Models of inherent device variability*
- *Statistical, dynamic “signoff”*

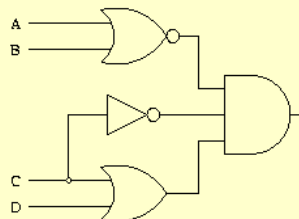
Design Roadmap Must Span *Both Logic and Memory*

LOGIC



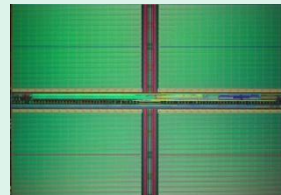
Chip

MEMORY

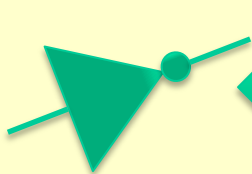


Circuit

Array

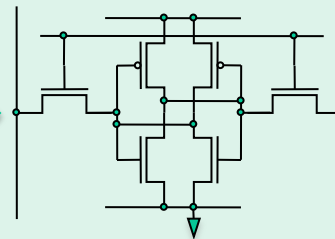


2011 DFM section: New reliability, SRAM cell models

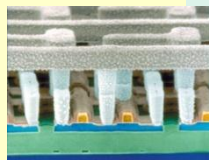


Gate

Bit Cell



Device



Physical

Design / System Drivers 2011* -2012* Plans

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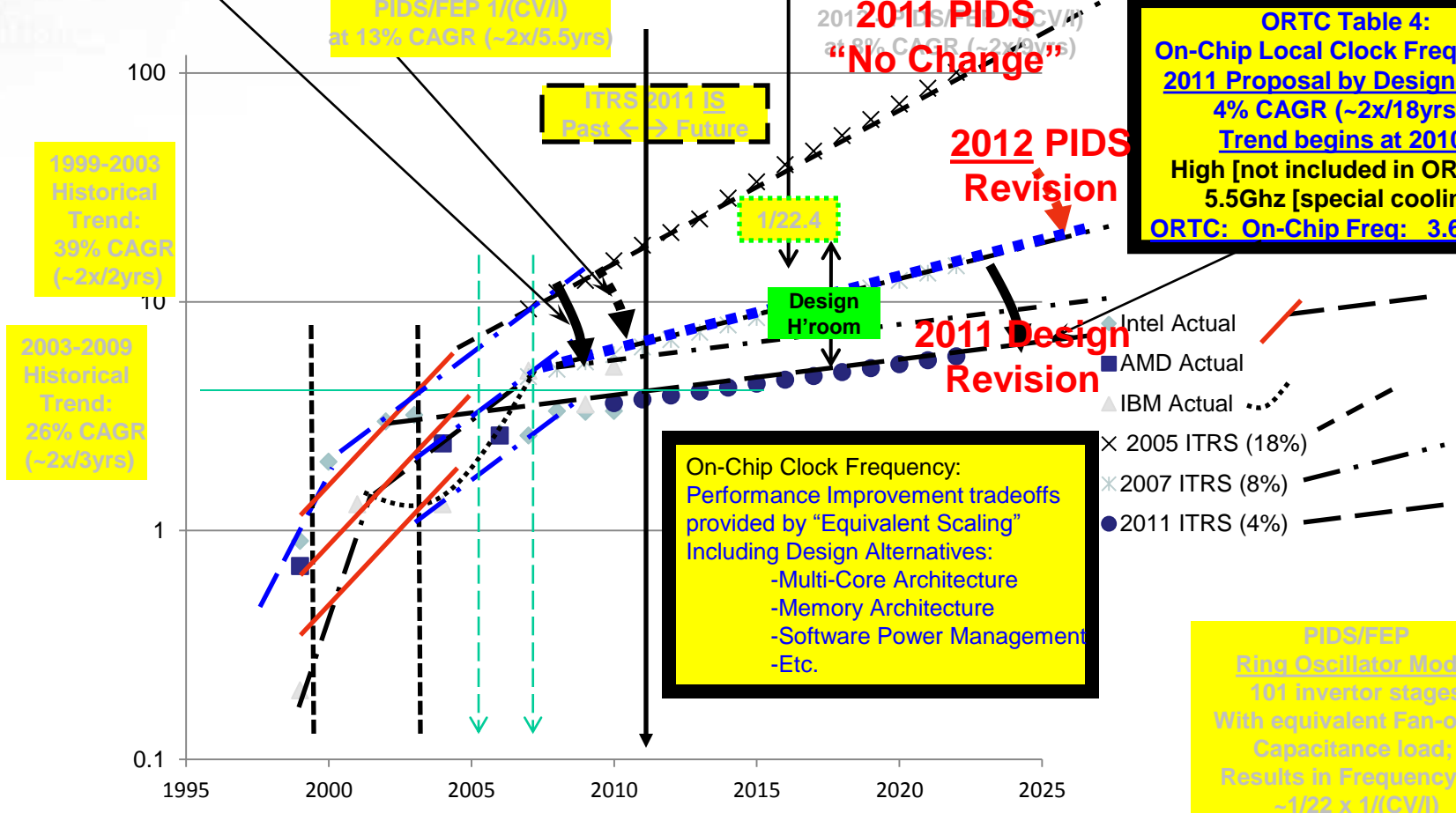
PIDS/FEP CV/I WAS 2007: $1/(CV/I) =$
 from 18% to 13% CAGR (~2x/5.5yrs)
 2007 Proposal by Design TWG:
 On-Chip Freq. = from 18% to 8% CAGR
 (~2x/9yrs)

PIDS/FEP 1/(CV/I) WAS: 13% CAGR (~2x/5.5yrs)
 2011 Proposal by Design TWG: $1/(CV/I) = 8%$ CAGR
 (~2x/9yrs)

**ORTC Table 4:
 On Chip Local Clock Frequency
 "GOLD" Trend**

PIDS/FEP
 2012 Update
 Proposal

**ORTC Table 4:
 On-Chip Local Clock Frequency:
 2011 Proposal by Design TWG:
 4% CAGR (~2x/18yrs),
 Trend begins at 2010:
 High [not included in ORTC]:
 5.5Ghz [special cooling]
 ORTC: On-Chip Freq: 3.6Ghz**



Source: ITRS Test TWG compilation, ca 4Q 2010

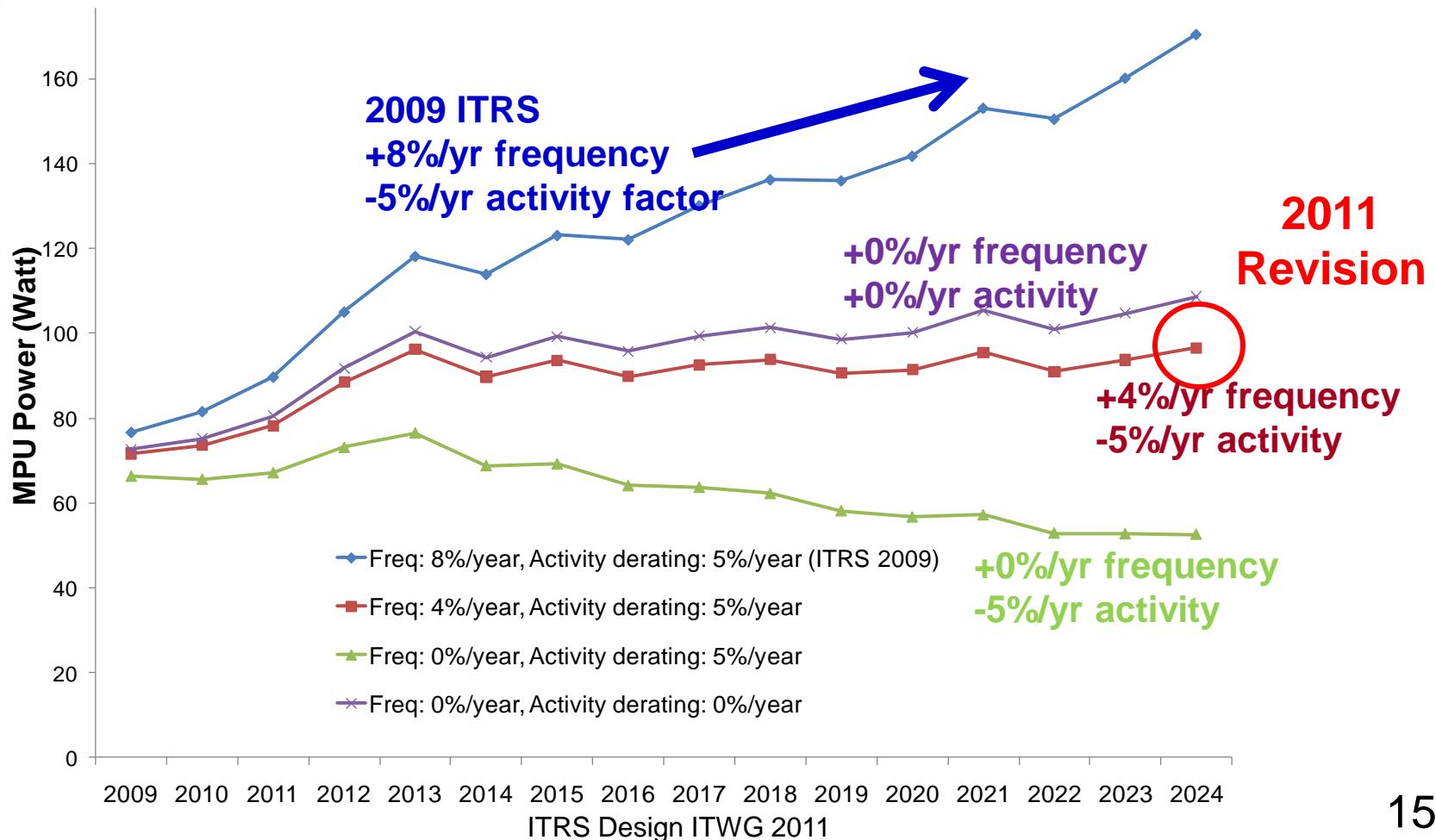
PIDS/FEP
 Ring Oscillator Model
 101 inverter stages
 With equivalent Fan-out 4
 Capacitance load;
 Results in Frequency of
 $\sim 1/22 \times 1/(CV/I)$
 at 13% CAGR (~2x/5.5yrs)

Work in Progress – Do Not Publish!



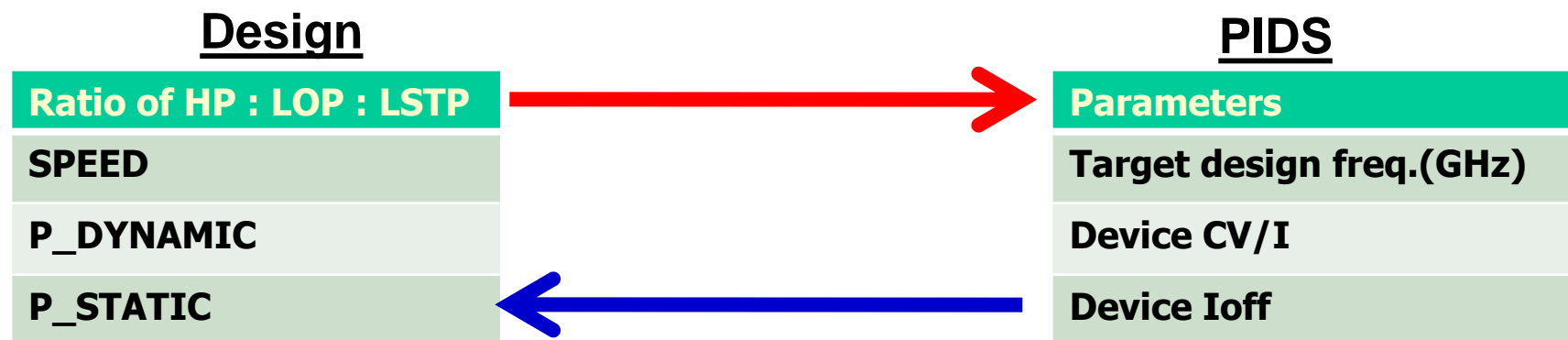
Power-Constrained MPU Frequency

- 2007: power limit led to 8%/year MPU frequency scaling, BELOW 13%/year intrinsic device CV/I scaling
- 2010: 8%/year too aggressive, given markets and devices



Example Impact: Design-PIDS Cross-TWGW

- Device speed “headroom” enables power savings in Design
- What selection of devices can PIDS provide together in a process?
 - High Performance (HP): Highest Ion and Ioff, lowest CV/I
 - Low Operating Power (LOP): Lowest VDD, medium Ion, Ioff and CV/I
 - Low Standby Power (LSTP): Lowest leakage, low Ion, high CV/I
- What ratio of device characteristics does Design want?
 - Preferred order of dynamic power: LOP < LSTP << HP
 - Preferred order of leakage power: LSTP < LOP << HP



Application- and Market-driven

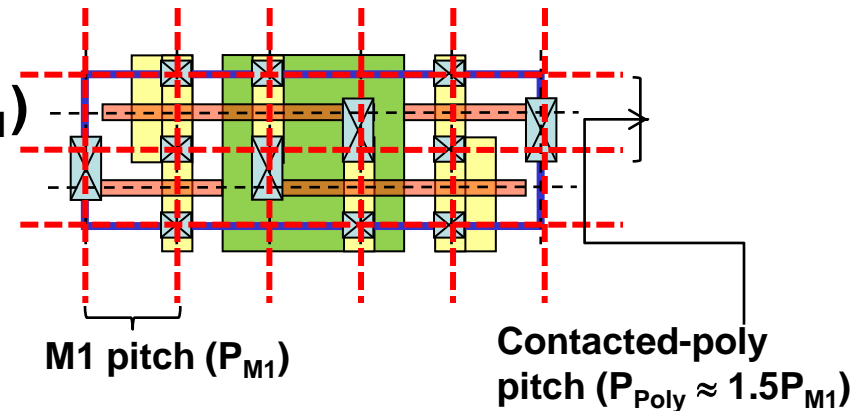
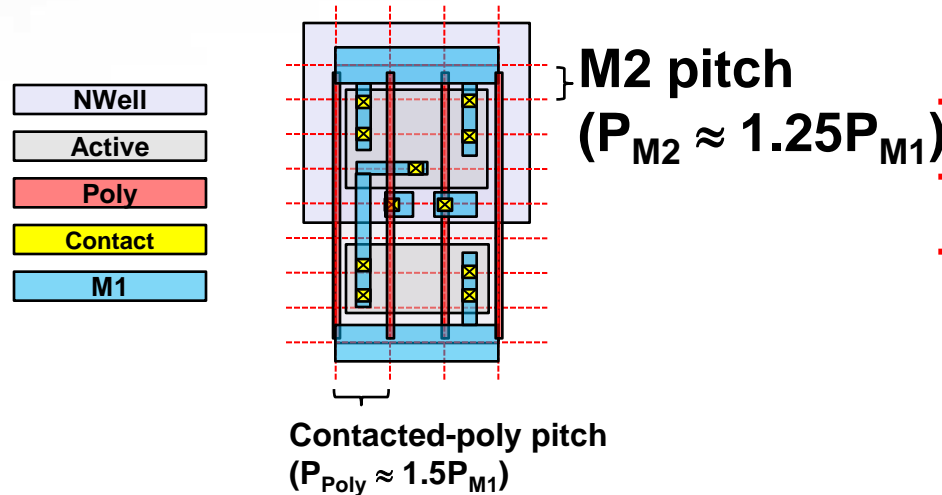
Technology-driven

2012 Plans: Update of Layout Density in MPU, SOC Products

(Area = "A-factor" $\times F^2$)

- Logic: A-factor = 175

- SRAM: A-factor = 60



NAND2 Area

$$\begin{aligned}
 &= 3 P_{Poly} \times 8 P_{M2} \\
 &\approx (3 \times 1.5 P_{M1}) \times (8 \times 1.25 P_{M1}) \\
 &= 45 (P_{M1})^2 \\
 &= 180 F^2 \rightarrow \mathbf{175 F^2}
 \end{aligned}$$

SRAM Bitcell Area

$$\begin{aligned}
 &= 2 P_{Poly} \times 5 P_{M1} \\
 &= 3 P_{M1} \times 5 P_{M1} = 15 (P_{M1})^2 \\
 &= 15 (2 F)^2 = \mathbf{60 F^2}
 \end{aligned}$$

Fitted to industry data

2012-2013: Update for 8T SRAM, MGFET, density scaling challenges

ITRS Consumer Portable Driver

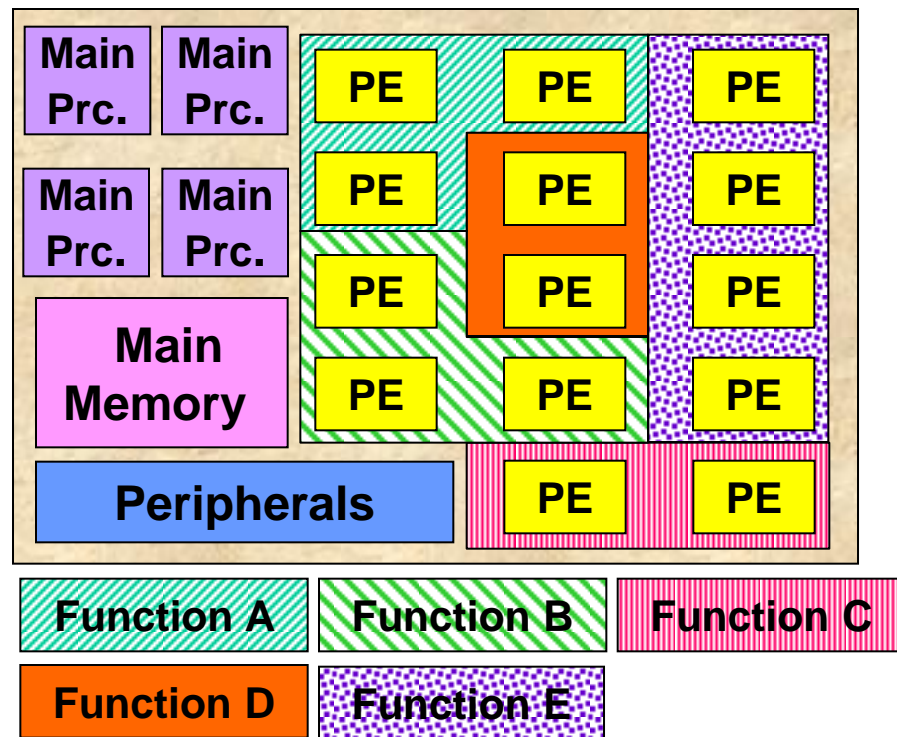
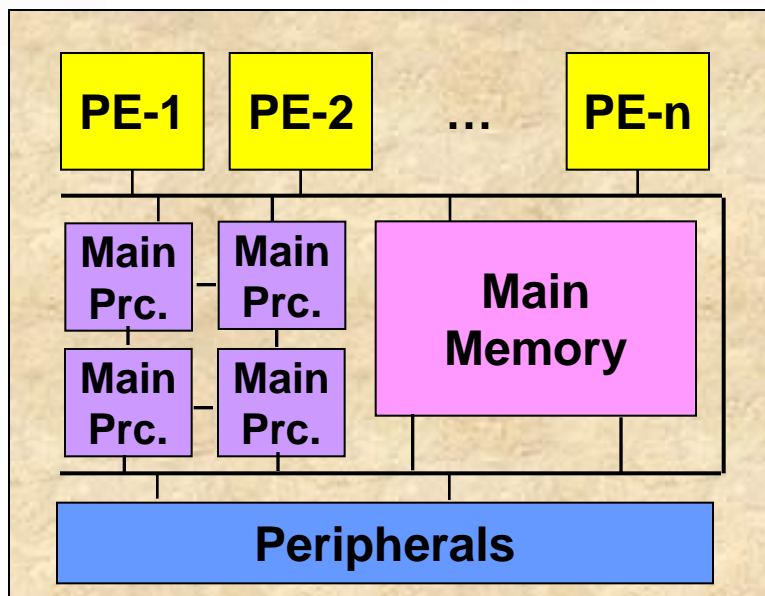


Figure SYSD4 SOC Consumer Portable Driver Architecture Template

Same model as ITRS2009

ITRS Consumer Portable Update (2011)

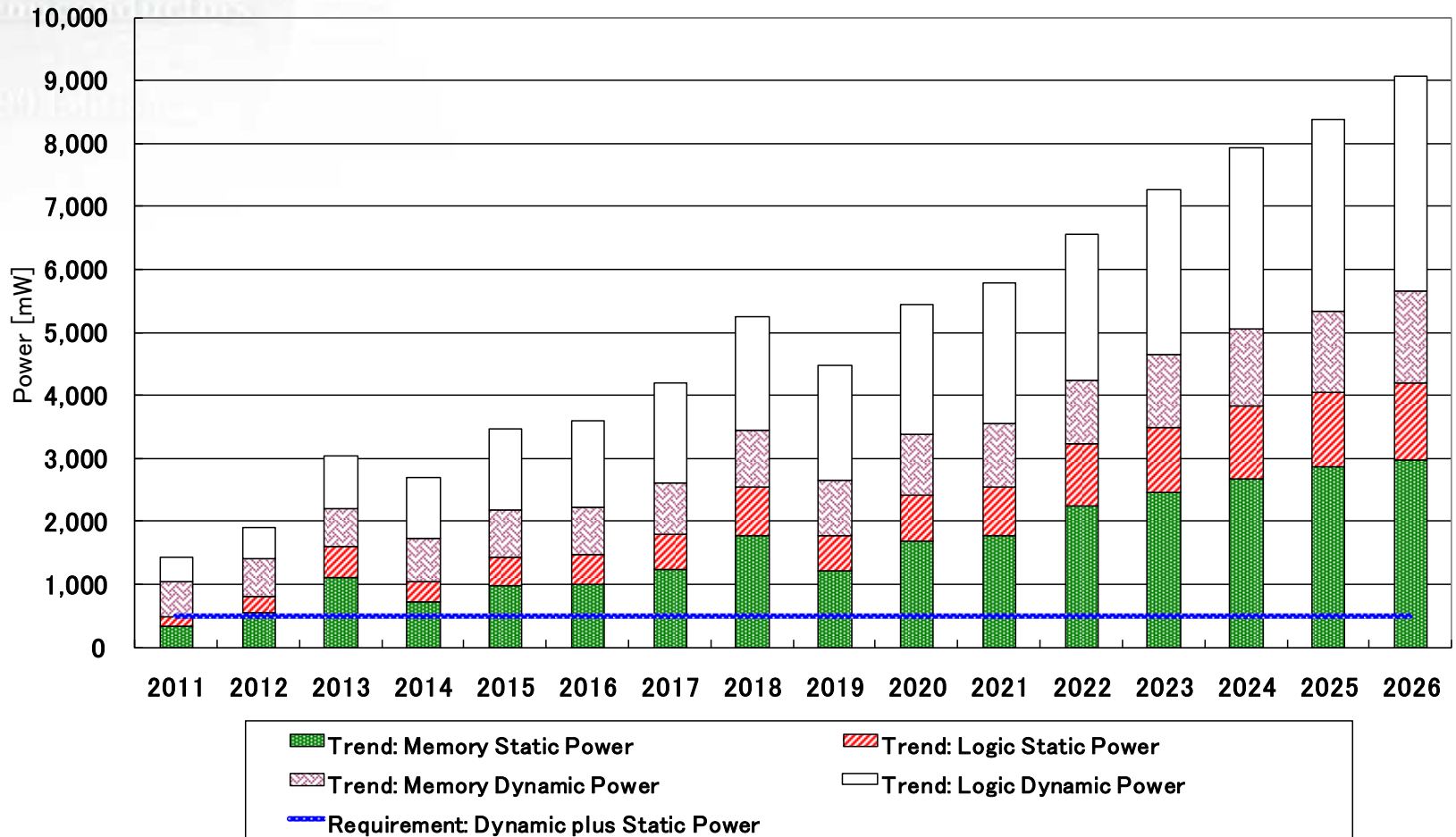


Figure SYSD6 SOC Consumer Portable Power Consumption Trends

ITRS Consumer Portable Update (2011)

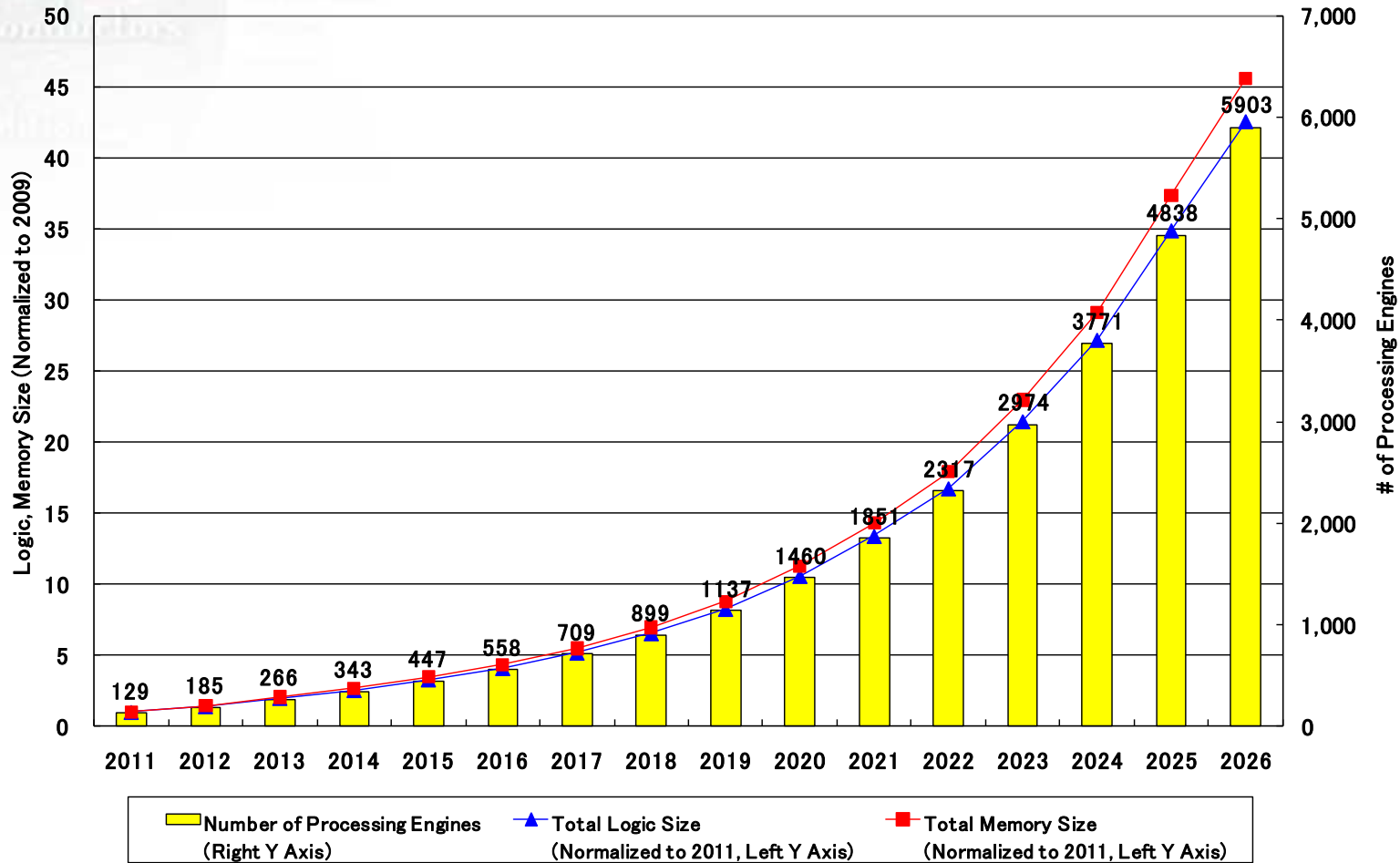


Figure SYSD5 SOC Consumer Portable Design Complexity Trends

ITRS Consumer Stationary Driver

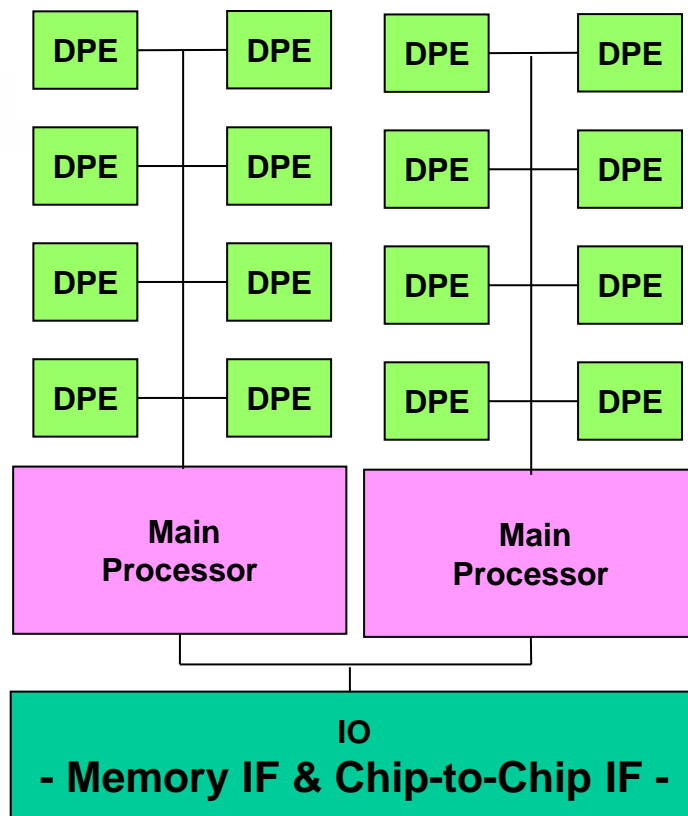


Figure SYSD8 SOC Consumer Stationary Driver Architecture Template

Same model as ITRS2009

ITRS Consumer Stationary Update (2011)

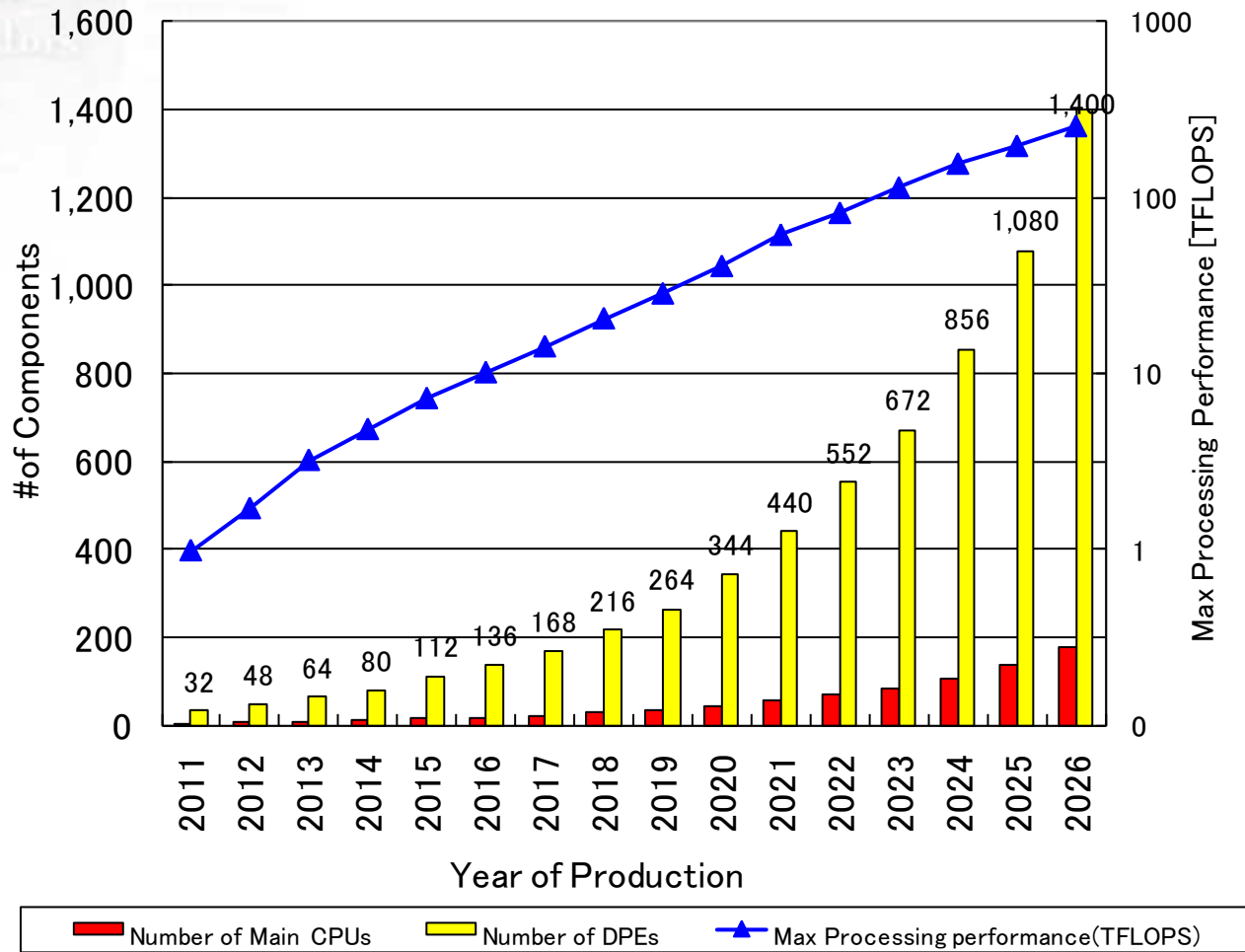


Figure SYSD9 SOC Consumer Stationary Trends

ITRS Consumer Stationary Update (2011)

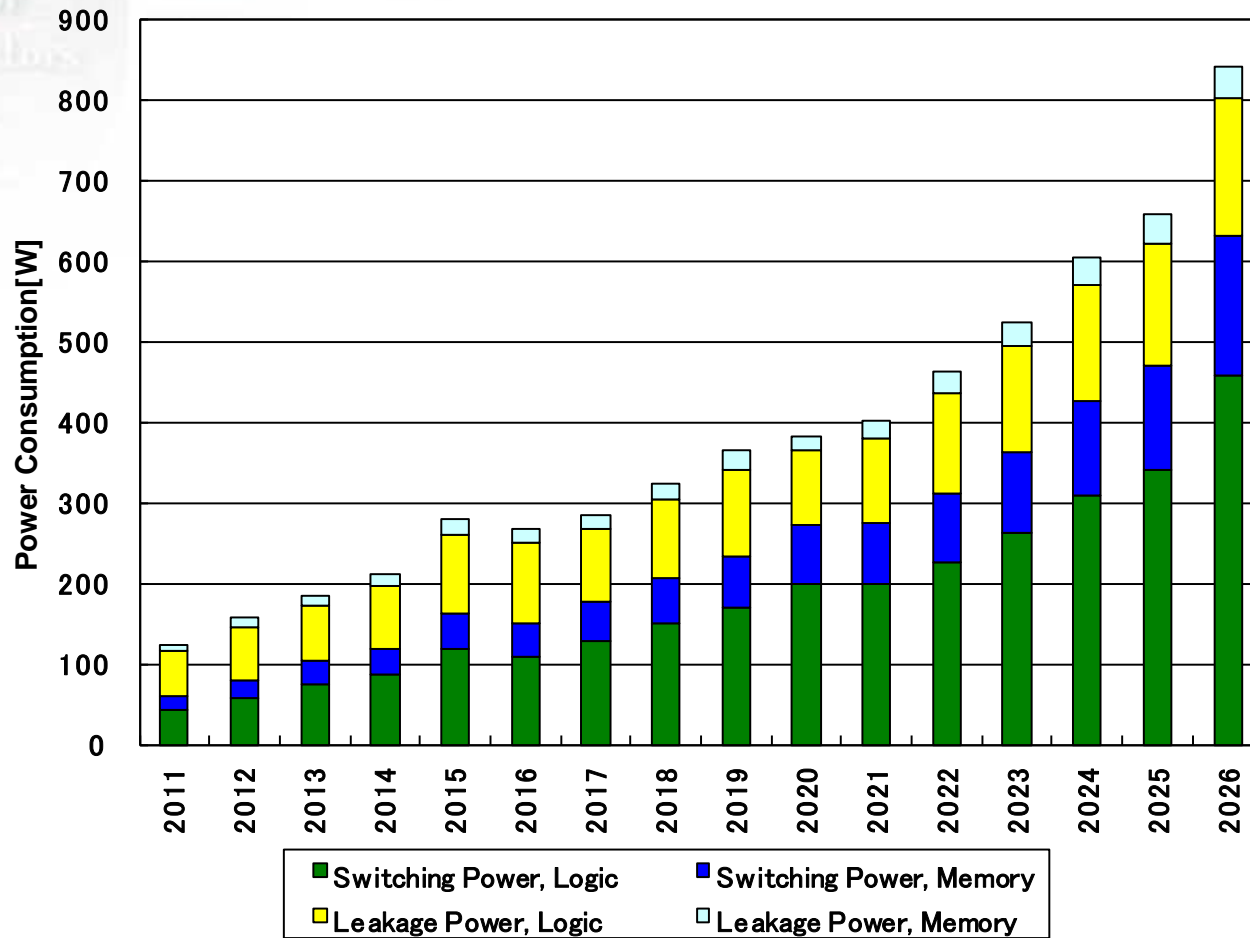


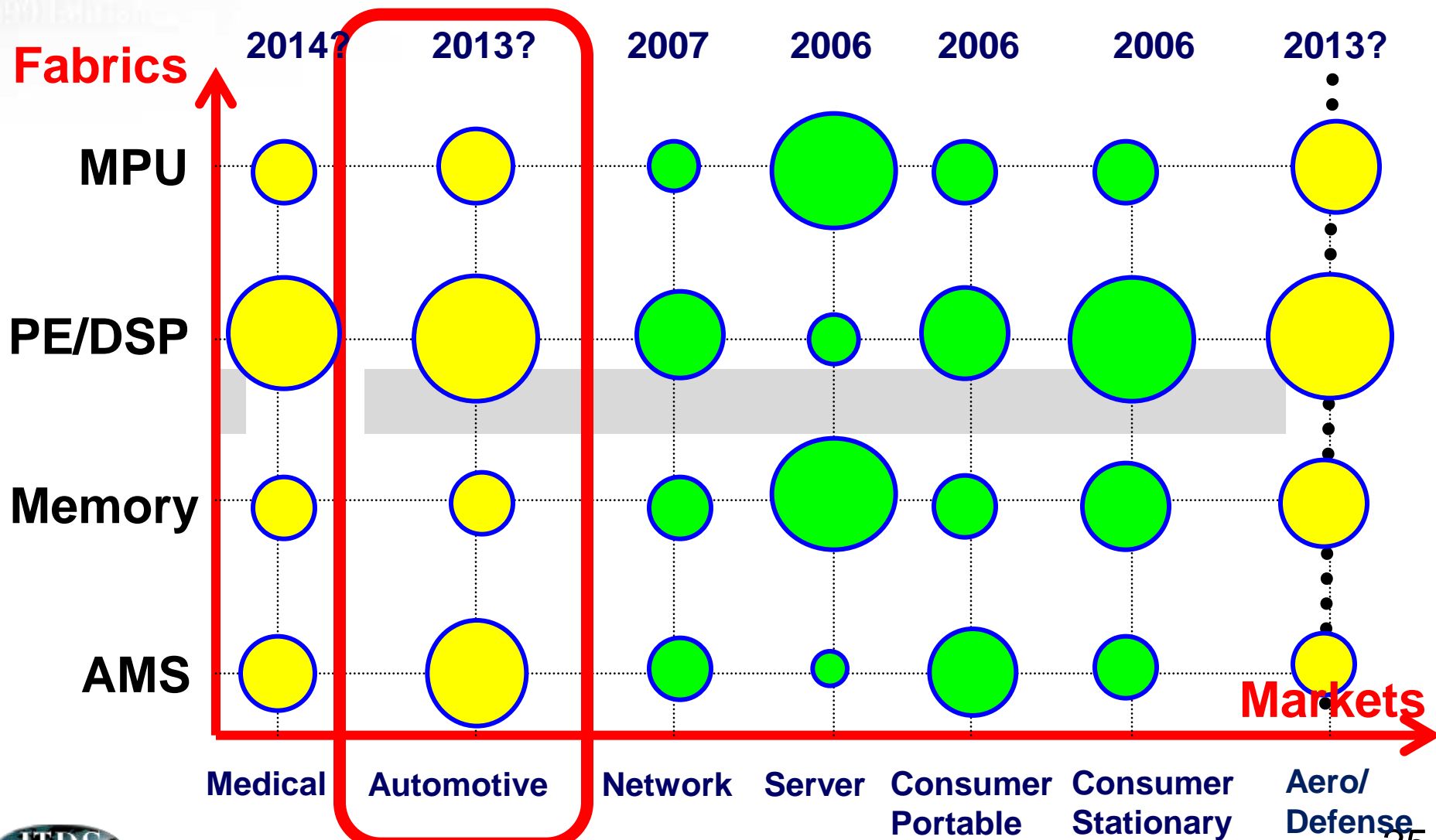
Figure SYSD11 SOC Consumer Stationary Power Consumption Trends

Core Effort: STRJ-WG1 SOC Modeling

- **Basis for quantifying ITRS Grand Challenges**
 - **Productivity → Power**
 - 2003: Low-Power SOC proposal
 - 2005: Consumer Portable SOC power analysis
 - 2006: Consumer Stationary SOC power analysis
 - 2007: Productivity impact of low-power design
 - 2008/9: Changes to devices, densities
- **2012+: Major renewal of SOC Consumer Drivers**
 - Updates of target applications
 - Heterogeneity (A/MS content, interfaces, application-specific accelerators)
 - Design productivity model including software

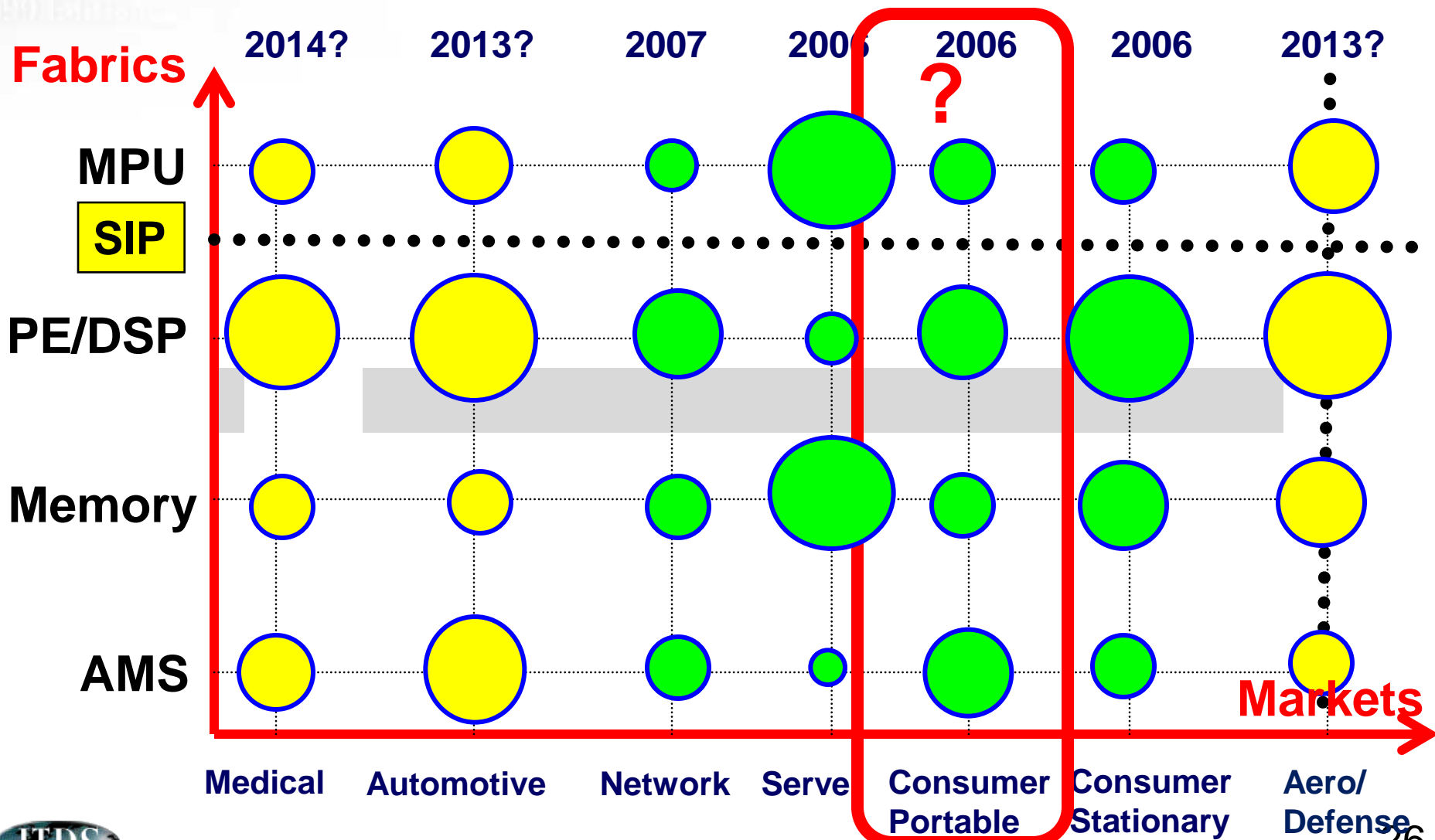
New System Drivers?

- What is the next priority driver per MTM, other trends?
 - Should an energy management driver be introduced ?

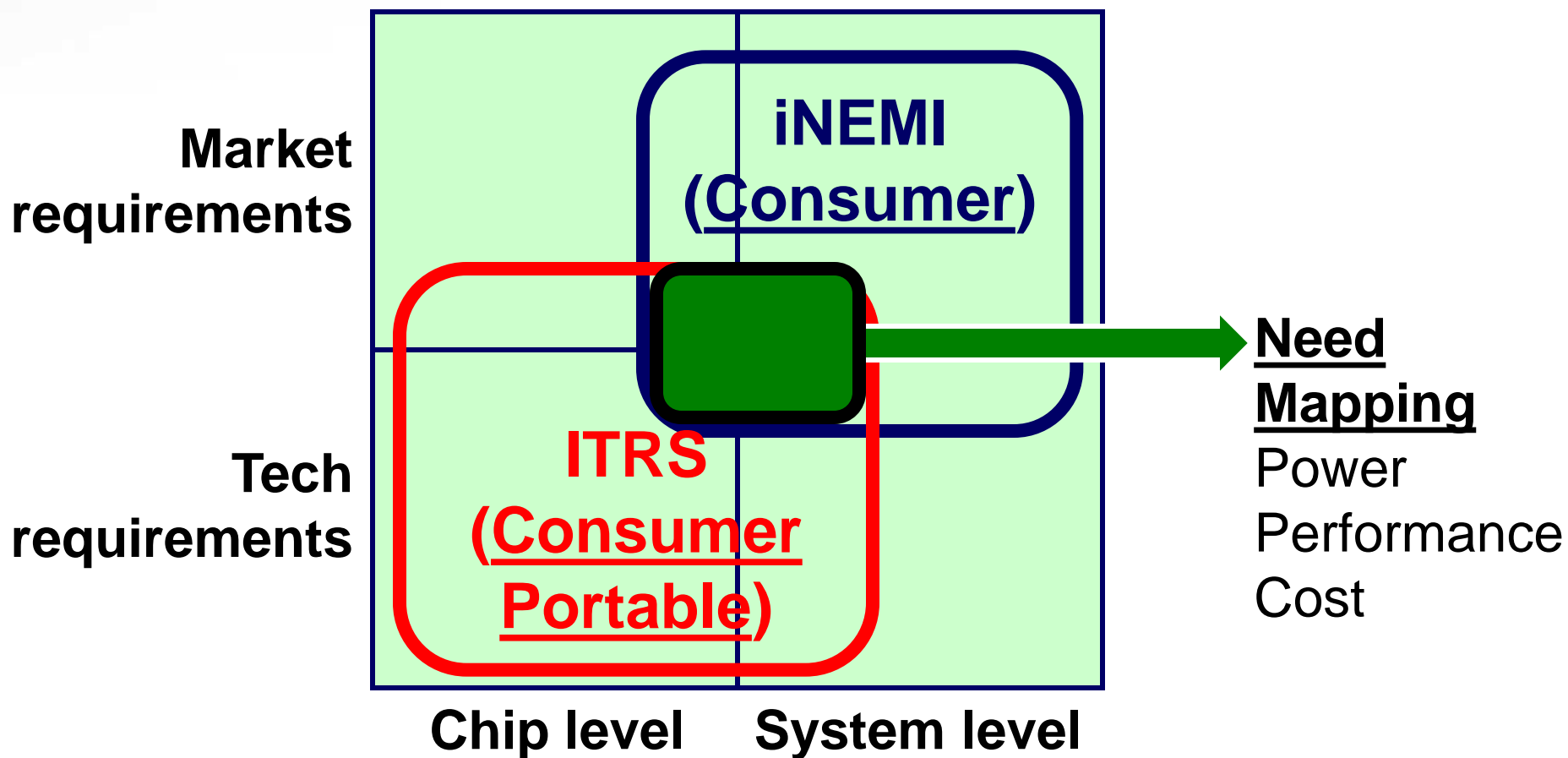


New Fabrics ?

- Is SIP a new fabric ?
- What application drives (leading edge) 3D/TSVs ?

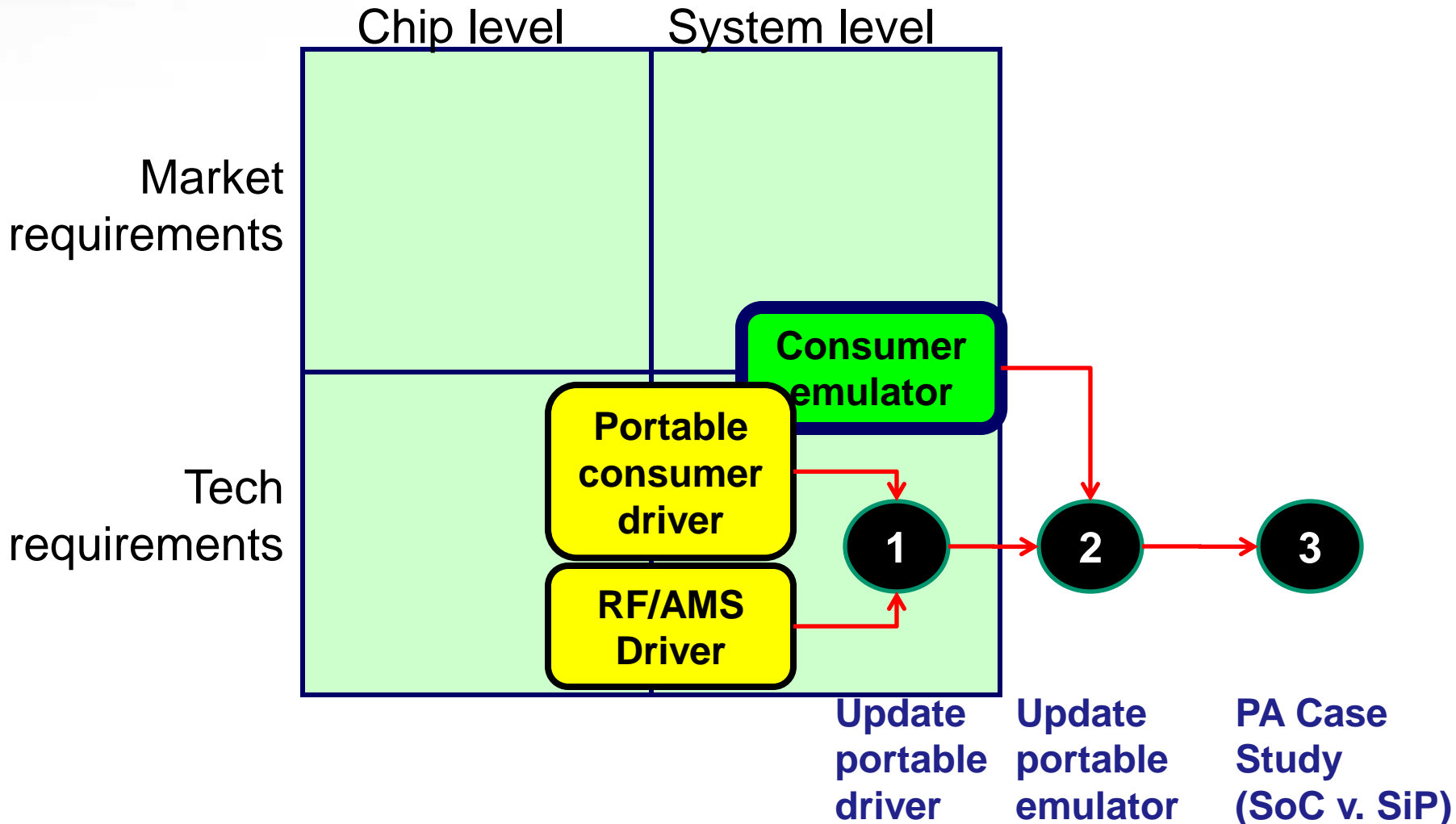


ITRS-iNEMI Domain Space



Impact of More Than Moore

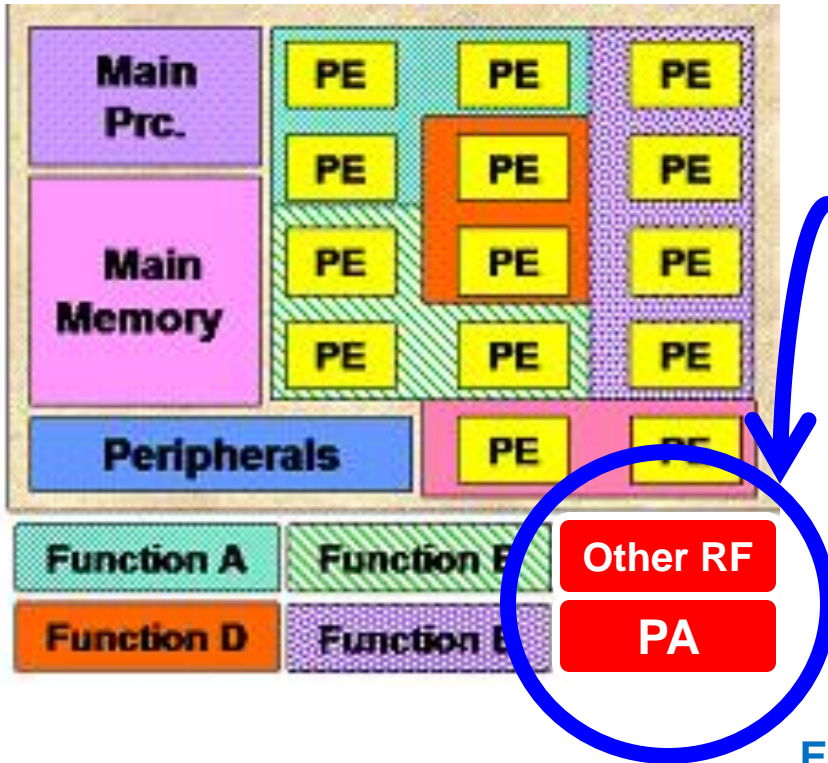
As System Components Integrate → Drivers Change



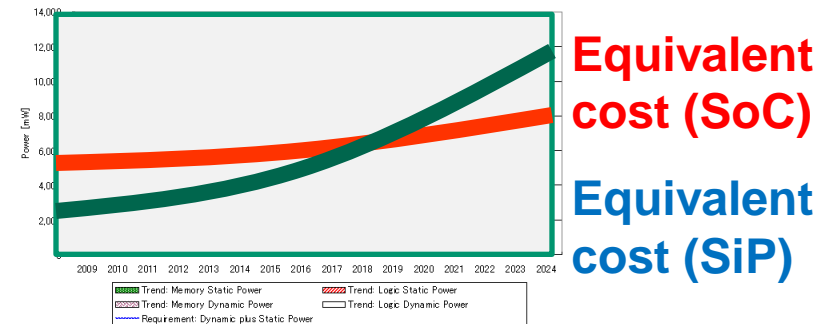
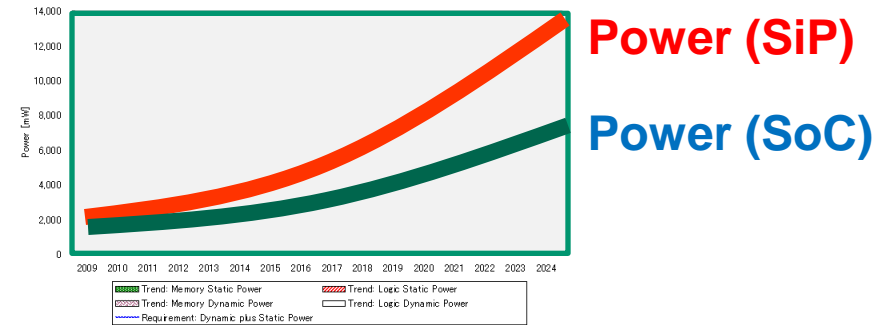
More Than Moore: SOC/SIP Design/Integration

Future Update of Consumer Portable System Driver

Inclusion of AMS/RF **sub-driver** from ITRS AMS driver



PA Case Study

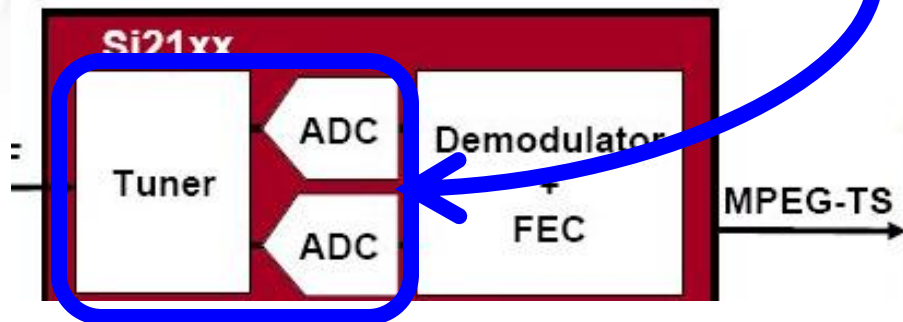


Equivalent cost = NRE + non-NRE per-board cost

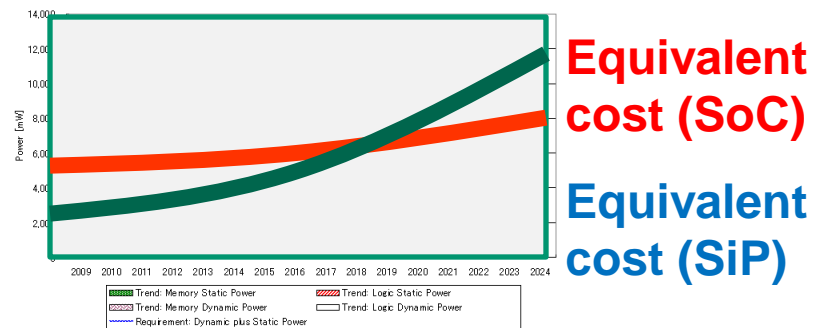
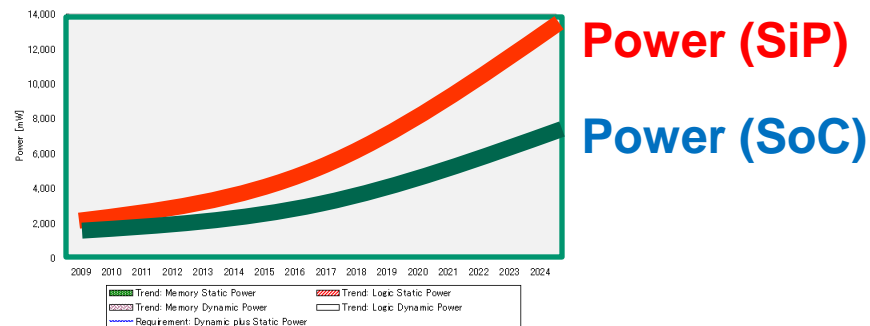
- NOTE: SOC vs. SIP tradeoffs depend on volume, development cost, performance, business model, other factors.

An Alternative Driver → Tuner / Demodulator

Inclusion of AMS/RF **sub-driver** from ITRS AMS driver



Tuner-demod case Study



Equivalent cost =
NRE + non-NRE per-board cost

Additional “rows” for combined analog-digital model

Requirement	Description
Tuner	Resolution, operating freqs, power
ADC/DAC	#bits, order, power, etc.
Demodulator /FEC decoder	Gain-bandwidth, power

- NOTE: SOC vs. SIP tradeoffs depend on volume, development cost, performance, business model, other factors.

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2011 Key Messages

DESIGN CHAPTER:

- There is a new low-power design roadmap!
- The new long-term Grand Challenges are (1) design of concurrent software and (2) design for reliability and resilience

SYSTEM DRIVERS CHAPTER:

- 2011 saw power-driven changes to the MPU frequency roadmap; we will soon see a power-driven device roadmap
- The SOC Consumer Drivers are being revised

IN GENERAL:

- Look for major growth of More Than Moore and 3D throughout the roadmap

2012+ Priorities

DESIGN CHAPTER

- Deeper integration of Power, 3D, and System design roadmaps throughout chapter
- Memory as first-class citizen
- Variability and Reliability roadmaps
- More Than Moore

SYSTEM DRIVERS CHAPTER

- Major updates of SOC Consumer Drivers
- Incorporate I/O, Analog/MS/RF in key System Drivers
- Collaboration with ERD: Emerging Research Architectures (where new devices, circuits, fabrics will be integrated)
- Continue efforts to align ITRS Drivers with iNEMI Emulators
- More Than Moore

Acknowledgments

- Thanks to the entire ITRS Design team, including...

Yoshimi Asada, Kenji Asai, Valeria Bertacco, Colin Bill, Ralf Brederlow, Yu Cao, Juan Antonio Carballo, John Darringer, Wolfgang Ecker, Dale Edwards, Eric Flamand, Paul Franzon, Tamotsu Hiwatashi, Masaharu Imai, Kwangok Jeong, Bill Joyner, Andrew Kahng, Masaru Kakimoto, Jong Ho Kang, Victor Kravets, Frederic Lalanne, Jingwei Lu, Vinod Malhotra, Masami Matsuzaki, Alfonso Maurelli, Nikil Mehta, Katsutoshi Nakayama, Sani Nassif, Nobuto Ono, Ralf Pferdmenges, Shishpal Rawat, Wolfgang Rosenstiel, Toshitada Saito, Jean-Pierre Schoellkopf, Gary Smith, Peter Van Staa, Leon Stok, Mikio Sumitani, Masahisa Tashiro, Hiroki Tomoshige, Tadao Toyoda, Shireesh Verma, Maarten Vertregt, Alfred Wong, David Yeh, Hak-soo Yu