

# PIDS Update

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Incheon, Korea

Speaker: Kwok Ng (PIDS U.S. Chair)



**US**

Ng, Kwok <sup>C</sup>
Chang, Chorng-Ping <sup>VC</sup>
Antoniadis, Dimitri
Bhavnagarwala, Azeez
Brewer, Joe
Bersuker, Gennadi
Cheung, Kin (Charles)
Dellin, Ted
Gallagher, Bill
Henderson, Christopher
Hutchby, Jim
Krishnan, Shrikanth
Lam, Chung
Maszara, Witek
Ning, Tak
Prall, Kirk
Stathis, James
Tsai, Wilman
Wong, Philip
Xu, Yanzhong
Yeap, Geoffrey
Yu, Scott
Zeitsoff, Peter

**PIDS Roster****Japan**

Wakabayashi, Hitoshi <sup>C</sup>
Inoue, Hirofumi <sup>VC</sup>
Akasaka, Yasushi
Futatsugi, Toshiro
Gohou, Yasushi
Hayashi, Yoshihiro
Hiramoto, Toshiro
Hisamoto, Digh
Ida, Jiro
Iwamoto, Kunihiko
Kasai, Naoki
Kurata, Hajime
Matsuo, Ichiro
Mogami, Tohru
Niwa, Masaaki
Oda, Hidekazu
Ohguro, Tatsuya
Sugii, Toshihiro
Takagi, Shinichi
Tanaka, Tetsu
Yoshimi, Makoro

C=Chair, CC=Co-Chair,  
VC=Vice-Chair

**Europe**

Boeuf, Frederic <sup>C</sup>
Burenkov, Alex
DeMeyer, Kristin
Jurczak, Malgorzata
Kuper, Fred
Lander, Robert
Poiroux, Thierry
Schulz, Thomas

**Taiwan**

Liu, Rich <sup>CC</sup>
Tsai, Cheng-tzung <sup>CC</sup>
Diaz, Carlos
Hsu, Hsing-Hui
Oates, Tony

**Korea**

Jeong, Moon-Young <sup>C</sup>
Oh, Sang Hyun
Park, Jongwoo



# Outline

- PIDS Mission and Technical Sub-Groups
  - Logic
  - Memory: DRAM
  - Memory: Nonvolatile Memory
  - Reliability
- 2011 Edition Summary
- Plans for 2012 Edition



- **PIDS** =  
**P**rocess **I**ntegration, **D**evices, & **S**tructures
- Mission:
  - Provide physical and electrical requirements and solutions for sustaining IC scaling in digital logic technologies and memory technologies.
  - Scopes:
    - Performance (speed, density, power, functionality...)
    - Structures
    - Process-integration challenges
    - Reliability



# PIDS Technical Sub-Groups

- Logic (Leads = Ng, Wakabayashi, Cheung, Chang)
  - HP = High Performance (speed) (e.g.,  $\mu$ P...)
  - LOP = Low Operating (Dynamic) Power (e.g., notebook...)
  - LSTP = Low Standby (Static) Power (e.g., cellular...)
  - III-V/Ge = (New) Alternate channel for low dynamic power and high speed

n

	HP	LOP	LSTP	III-V/Ge
Speed ( $I/CV$ )	Ref	lower	Lowest	Higher
Dynamic Power ( $CV^2$ )	Ref	Lowest	Lower	Lowest
Static Power ( $I_{off}$ )	Ref	Lower	Lowest	Ref

- Memory: DRAM (Lead = Inoue, Jeong)
- Memory: Nonvolatile (Leads = Liu, Inoue, Oh)
- Reliability (Leads = Cheung, Park)



## 2011 Update: Logic

- $CV/I$  slope of 13%/year maintained. (See plan for next year.)
- After series of workshops followed by survey (with other TWGs ERD/ERM/FEP), add III-V (for  $n$ -channel) and Ge (for  $p$ -channel) as alternate channel materials for high speed AND low dynamic power.  
Product introduction year = 2018.
- Add dynamic power metric  $CV^2$  on all logic options.  
Only as monitor, not as specs.
- $L_{gate}$  and  $V_{dd}$  curves “smoothed” out roughness but trends remain the same.

# 2011 Update: Logic

(cont'd)

A relative comparison of logic technologies.

	HP	LOP	LSTP	III-V/Ge
Speed ( $I/CV$ )	Ref = 1	0.5	0.25	1.5
Dynamic Power ( $CV^2$ )	Ref = 1	0.6	1	0.6
Static Power ( $I_{off}$ )	Ref = 1	$5 \times 10^{-2}$	$1 \times 10^{-4}$	1

## 2011 Update: DRAM

Updates were mostly based on survey performed by Japan PIDS, complete in March 2011.

- Half-pitch unchanged (compared to 2010 version) for near years. Minor changes for far years (slightly relaxed).
- Cell size factor transition from  $6F^2$  to  $4F^2$  unchanged (2013).
- Unchanged, Vertical Channel transistor will be launched in 2013, in place of Recessed Channel, and continues till end of roadmap.

## 2011 Update: Nonvolatile Memory

NAND flash survey had been performed by Japan PIDS (completed March 2011). Together with market observations, following changes had been made:

- Compared to 2010 Edition, half-pitch scaling is accelerated by 1 year.
- Product density (in Gb) is accelerated by 1 year.
- Introduction of 3-D NAND is delayed by 1 year to 2016.
- New 3-D table format:  
Distinguish 3-D NAND from 2-D NAND with separate values in half-pitch, MLC, density...
- Other NVM devices (NOR, MRAM, STT-MRAM, PCRAM) updated. STT-MRAM merged into same table.



## 2011 Update: Reliability

Introduce a new category for highly reliable system (e.g., medical) with more stringent early failure rate that improves by 15% year-over-year.



## Plans for 2012 Edition

- To address lower-power requirement, and with chip clock frequency increase per year has slowed down, transistor speed  $CV/I$  slope will be decreased from 13%/yr to 8%/yr. Consequences: Lower  $V_{dd}$  and relaxed gate length.
- From market announcement, bring MG forward from 2015 to 2012.
- Add new parameter in logic to reflect advantage of MG, in  $V_{dd}/I_{on}/W_{footprint}$
- Working with Purdue University TCAD modeling group to explore establishing public website and tools to project device characteristics.
- New DRAM survey will be completed by end of Feb. 2012. Additional survey items based on latest process technology (i.e., buried WL, cell FET materials, etc.) will be added.
- **New NAND survey will be conducted at same time.**

