

Modeling and Simulation ITWG

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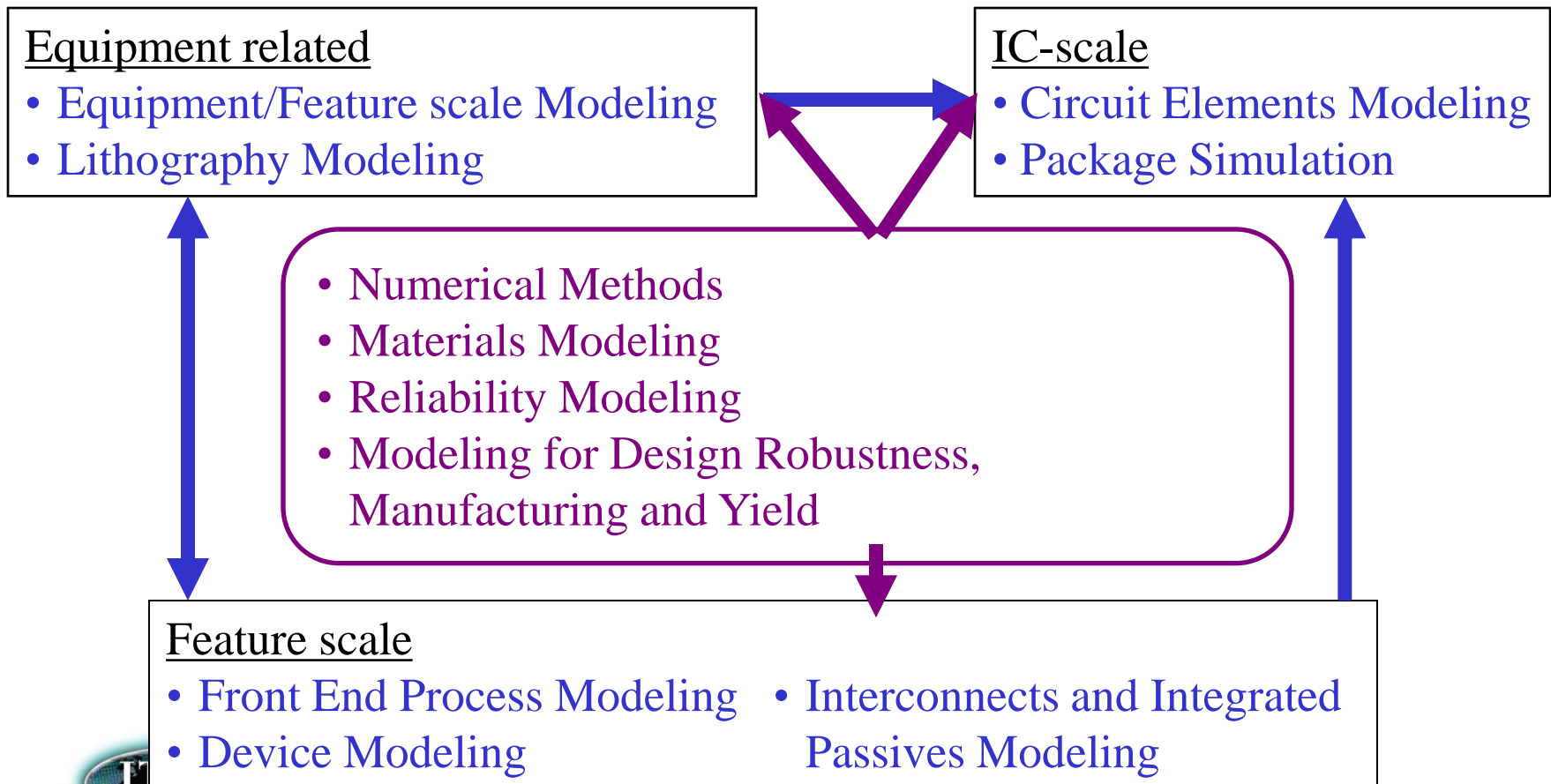
V. Moroz, Synopsys



Modeling & Simulation SCOPE & SCALES

Modeling Overall Goal

- Support technology development and optimization
- Reduce development times and costs



Key Messages

- Mission of Modeling and Simulation as cross-cut topic:
Support areas covered by other ITWGs
 - ⇒ Continued in-depth analysis of M&S needs of other ITWGs, based on documents + inter-ITWG discussions
 - ⇒ Strong links with ALL ITWGs – see also crosscut texts in 2007/9 ITRS
- Modeling and simulation provides an ‘embodiment of knowledge and understanding’. It is a tool for technology/device development and optimization and also for training/education
- Technology modeling and simulation is one of a few methods that can reduce development times and costs:
 - 2008 major action on assessment of industrial use of TCAD and reduction of development times and costs in best-practice cases



Development Time and Cost Reduction Estimate

Answers on question for average reduction of development time and costs in success case of simulation which occurred in environment of TCAD users:

Table MS3 Modeling and Simulation Technology Requirements: Accuracy [1] —Near-term Years

Year of Production	2009	2010	2011	2012	2013	2014	2015
DRAM $\frac{1}{2}$ Pitch (nm) (contacted)	52	45	40	36	32	28	25
MPU Physical Gate Length (GLph) (nm)	29	27	24	22	20	18	17
Estimated technology development cost reduction from use of TCAD (average across best-practice cases reported by industry) [2]	30%	32%	35%	37%	n.a.	n.a.	n.a.
Estimated technology development time reduction from use of TCAD (average across best-practice cases reported by industry) [2]	32%	34%	37%	39%	n.a.	n.a.	n.a.
<i>Lithography Modeling</i>							
Absolute CD prediction accuracy (incl. OP effects) for dense and isolated lines – % of actual CD (=printed gate length) [3]	1%	1%	1%	1%	1%	1%	1%

Definition different from estimate before 2008 which referred to cost reduction potential and was based on earlier survey



Basic Approach and Status of 2011 Work

- 1) Detailed cross-cuts worked out since 2003 – regularly updated together with other ITWGs – continued in 2011 as input to tables and text editing
- 2) Very long-term modeling also in ERM chapter – to be transferred into M&S in parallel to technology transfer to PIDS or other ITWGs
- 3) Analysis of potential solutions from other ITWGs especially important. Interaction with ERD/ERM for long-term challenges and requirements.
- 4) Detailed revision of M&S tables based on state-of-the-art & cross-cut requirements
- 5) Dedicated TCAD simulation support for PIDS assessment of future device performance started



Main Changes in 2011 Challenges

Titles of the challenges unchanged

Short-term challenges:

- “Lithography simulation including EUV”: One new item added, two old items skipped
- “Front-end process modeling for nanometer structures”: Two new items added, two old items skipped
- One new item added for “Integrated modeling of equipment, materials, feature scale processes and influences on device and circuit performance and reliability, including random and systematic variability”
- One new item added for “Electrical-Thermal-Mechanical Modeling for Interconnects and Packaging“
- Reorganization of some items for “Circuit Element and System Modeling for High Frequency (up to 300 Ghz) Applications”
- Several items modified

Long-term challenges:

- One item added in challenge “Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials”
- Some items slightly changed in challenges “Modeling of chemical, thermomechanical and electrical properties of new materials” , “Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials”, and “Optoelectronics modeling”

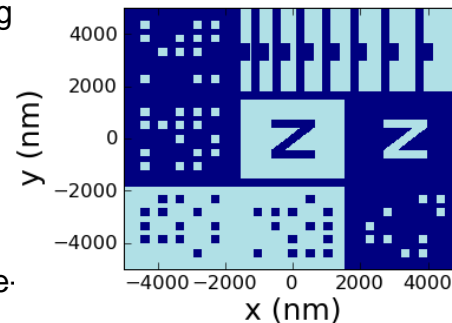


2011 Short-Term Difficult Challenges - ~~changes from 2010 in blue / red~~

Lithography Simulation including EUV

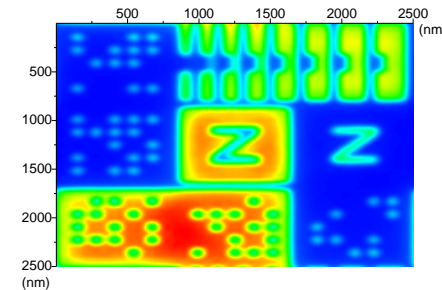
- ~~Models and experimental verification of optical and non-optical immersion lithography effects (e.g., topography and change of refractive index distribution)~~
- ~~Simulation of multiple exposure/patterning including database splitting~~
- ~~Multi-generation lithography system models~~ [Complementary lithography](#)
- Simulation of defect [inspection and characterization](#), influences/defect printing ~~in EUV~~. Mask optimization including defect [repair or](#) compensation
- ~~Optical~~ Simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including [EMF and resist effects](#), [and](#) extensions for inverse lithography
- Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects
- Predictive and separable resist models (e.g., mesoscale models) including line-edge roughness, accurate profiles, topcoat [and substrate \(underlayer\)](#) interactions, etch resistance, adhesion, mechanical stability, leaching, [swelling or slimming](#), and time-dependent effects in in single and multiple exposure
- Resist model parameter calibration methodology (including kinetic ~~and~~ transport [and stochastic](#) parameters)
- Fast, predictive simulation of ebeam mask making (single-beam and multibeam) [including short and long range proximity corrections](#)
- Simulation of directed self-assembly of sublithography patterns
- Modeling lifetime effects of equipment and masks, including lens and mirror heating effects
- Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning)
- Modeling metrology equipment [and data extraction](#) for enhancing ~~its~~ [model calibration](#) accuracy
- [Modeling of pellicle effects and pellicle defects simulation \(incl. double patterning, self-aligned patterning\)](#)

Example (Fraunhofer IISB): Large-area rigorous simulation of optical lithography



Mask layout
(dark-blue =
Cr absorber)

Mask scale
= 4 times
wafer scale

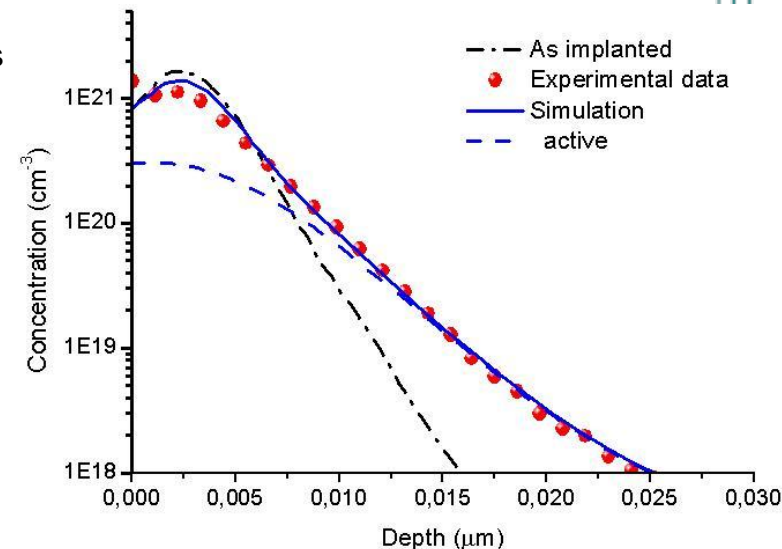
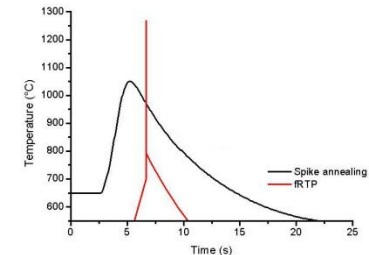


High
resolution
aerial image
computed
with Dr.LiTHO
(Waveguide +
new Imaging:
5.4 h on one
CPU with 2.8
GHz.
Additionally,
efficient
parallelization
possible).



2011 Short-Term Difficult Challenges – changes from 2010 in blue / red Front-End Process Modeling for Nanometer Structures

- Coupled diffusion/(de)activation/damage/stress models and parameters including low-temperature, SPER, and millisecond and microwave processes in Si-based substrate, that is, Si, SiGe, SiGe:C, Ge-on-Si, III/V-on-Si (esp. In-GaAs-on-Ge-on-Si), SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers. Accurate model for Stress-Induced Defects
- Implantation models for ions needed for new materials
- Models for alternative implantation methods : Plasma doping (e.g. for FinFets), cluster implantation, cryo or hot implants (incl. self-annealing)
- Diffusion in advanced gate stacks
- Predictive segregation and dose loss models
- Modeling of interface and dopant passivation by hydrogen or halogens
- ~~Modeling of cluster or cocktail implants~~
- ~~Modeling of plasma doping, e.g. for FinFETs. Predictive modeling of de-activation of dopants.~~
- Modeling of epitaxially grown layers: Shape, morphology, stress, defects, doping, diffusion, activation
- Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
- Efficient and robust 3D meshing for moving boundaries
- Front-end processing impact on device leakage (e.g. residual defects) and reliability
- Modeling the impact of front-end processing-induced damage to devices on their leakage, noise and reliability behavior during operation



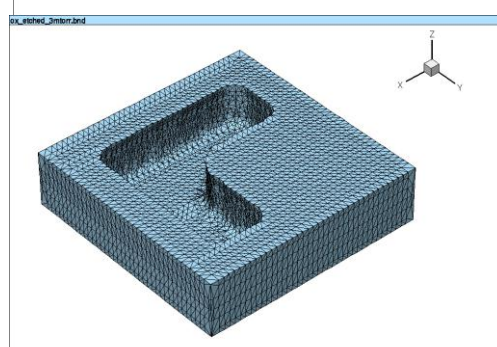
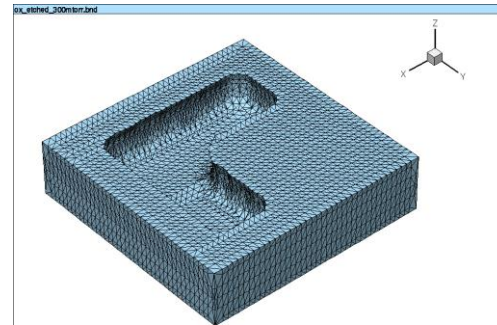
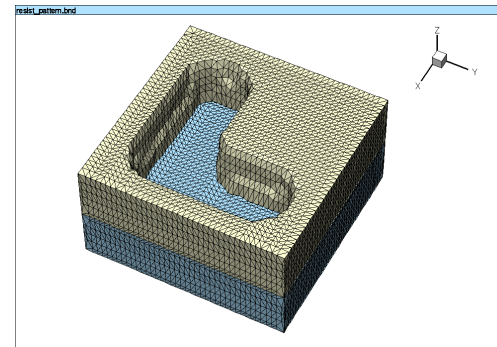
Source: P. Pichler et al. (FhG-IISB), Defect and Diffusion Forum 258-260, 510 (2006)



2011 Short-Term Difficult Challenges

Integrated modeling of equipment, materials, feature scale processes and influences on device and circuit performance and reliability, including random and systematic variability - changes from 2010 in blue / red

- Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-k metal gate); reaction mechanisms (reaction paths and (by-) products, rates ...), and simplified but physical models for complex chemistry and plasma reaction.
- Linked equipment/feature scale models (including high-k metal gate integration, [flows for RIE processes](#), damage prediction)
- Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
- Spin-on-dielectrics (stress, porosity, dishing, viscosity, ...) for high aspect ratio fills, [evolution during transformation and densification](#).
- Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
- Pattern/microloading effects in radiative annealing or plasma processing
- Propagation of process variations into circuit block simulation
- Simulation of [wafer](#) polishing, grinding and wafer thinning **in backend processings**
- Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulations
- [Modeling of impact of consumables \(e.g. resists, slurries, gas quality\) on process results](#)



Feature scale simulation of sputter etching: Initial geometry (top), simulation for 300 mTorr (middle) and 3 mTorr (bottom).

(From Fraunhofer IISB)

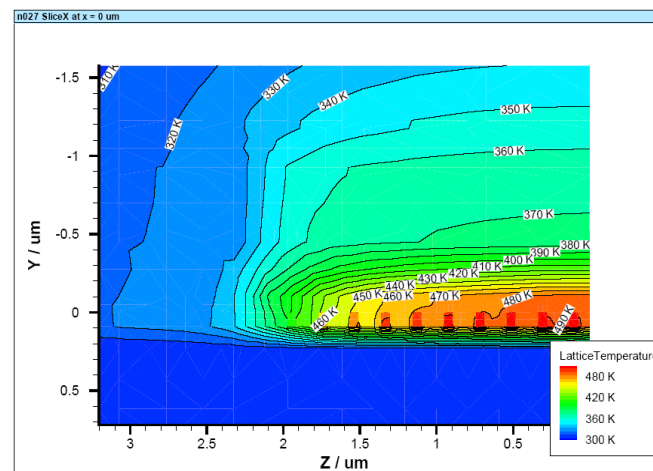
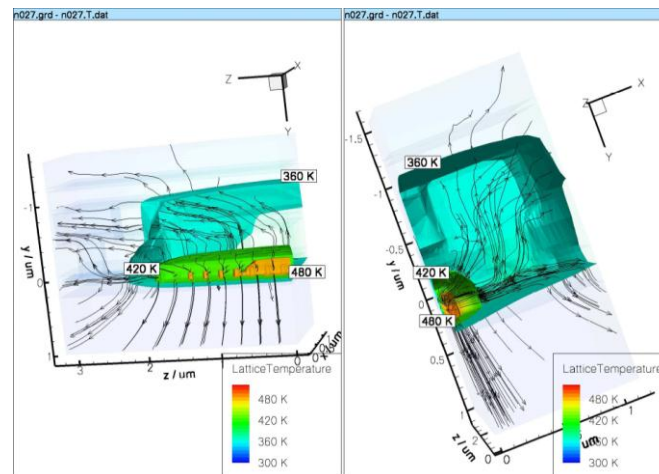


2011 Short-Term Difficult Challenges

Nanoscale Device Simulation Capability: Methods, models and algorithms

– changes from 2010 in blue / red

- General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
- Efficient models and tools for analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
- Models (incl. material models) to investigate new memory devices like [STT-MRAM](#), [nanoionic memories](#), [redox resistive memories](#), PCM/PRAM, etc.
- [Gate stack](#) Models for [gate stacks with ultra-thin/high-k dielectrics](#) [for all channel materials addressed above](#) w.r.t. electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport
- Modeling of salicide/silicon contact resistance and engineering (e.g. Fermi-level depinning to reduce Schottky barrier height)
- Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure and dopant [and materials](#) variations in order to assess the impact of variations on statistics of device performance
- Physical models for novel channel materials, e.g. [p-type Ge](#) and [compound III/V \(esp. n-type InGaAs-on-Ge-on-Si\)](#) channels...: Band structure, defects/traps, ...
- Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation. [Coupling between atomistic process and continuum or atomistic device simulation.](#)
- Reliability modeling for ultimate CMOS [and new memory devices](#)
- [Commercial](#) device simulators (software) for STT and [nanoionic redox resistive](#) memories
- Physical models for [\(mechanical\)](#) stress induced device performance [for advanced architectures \(esp. FinFET\) and/or novel materials](#)



Lattice temperatures in device
Source: Infineon / ESSDERC 2006



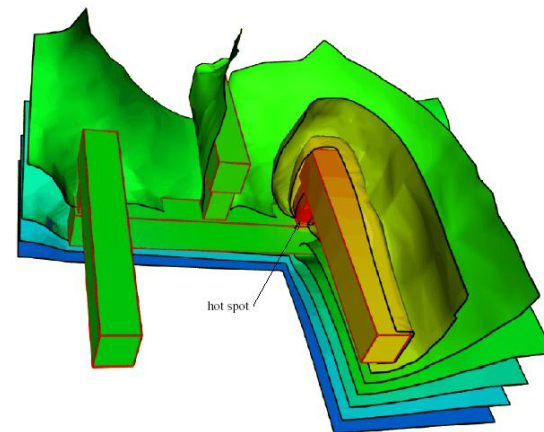
2011 Short-Term Difficult Challenges

Electrical-Thermal-Mechanical Modeling for

Interconnects and Packaging – changes from 2010 in blue / red

Needs

- Model thermal-mechanical, thermodynamic and electrical properties of low-k, high-k and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension
- Thermal modeling for 3D ICs and assessment of modeling and CAD tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, ...). Size effects (microstructure, surfaces, ...) and variability of thinned wafers.
- Signal integrity modeling for ~~stacked die~~ [3D ICs](#)
- Identify effects and apply/extend models which influence reliability of packages and interconnects incl. 3D integration (e.g. stress voiding, electromigration, fracture initiation, dielectric breakdown, piezoelectric effects)
- Physical models and simulation tools to predict adhesion and fracture toughness on interconnect-relevant interfaces (homogeneous and heterogeneous), packages and die interfaces
- Dynamic simulation of mechanical problems of flexible substrates and packages
- Models for electron transport in ultra fine patterned interconnects
- [Simulation tools for die, package and board that allow for coherent co-design](#)



courtesy TU Vienna / IST project MULSIC

Temperature distribution in an interconnect structure

2011 Short-term Difficult Challenges

Circuit Element and System Modeling for High Frequency (up to 300 Ghz)

Applications - changes from 2010 in blue / red

- Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package:
 - possibly consisting of different technologies,
 - covering and combining different modelling and simulation levels as well as different simulation domains - [including manufacturability](#)

- [Scalable active component circuit models including non-quasi-static effects, substrate noise and coupling, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling](#)

- [Introduction of new model features including non-quasi-static effects, substrate noise and coupling, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling](#)

- Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently

- [Scalable active component models for circuit simulation of new multigate MOSFET like double gate FDSOI, FinFET ...](#)

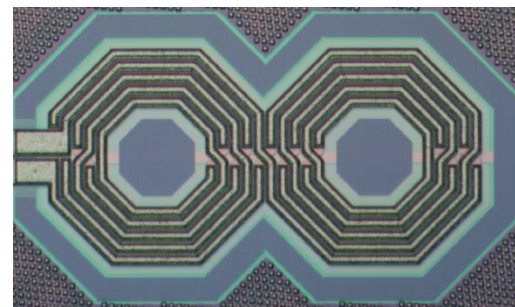
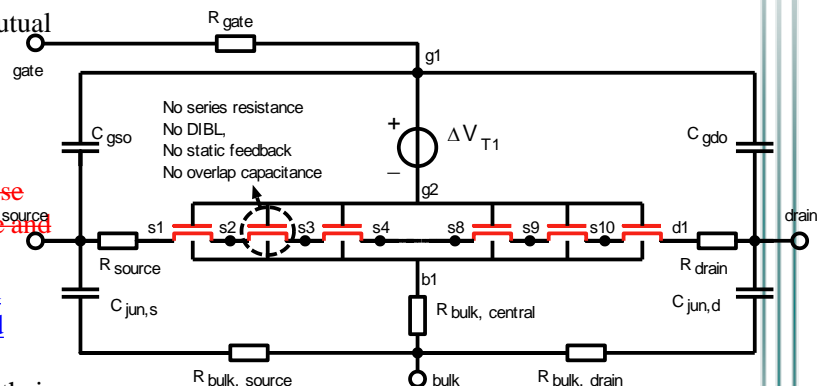
- Scalable passive component models for compact circuit simulation, including interconnect, transmission lines, ...

- Scalable circuit models for More-than-Moore devices including switches, filters, accelerometers, ...

- [Physical circuit element Compact models for new memory devices, such as PCM, and standardisation of models for III/V \(esp. InGaAs on Ge on Si\) devices](#)

- Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently

- Computer-efficient assessment of building block/circuit-level using process/device/circuit simulation, including process variations



(From NXP)



2011 Difficult Challenges

Changes from 2010
in blue / red

Difficult Challenges	Summary of Issues
Modeling of chemical, thermomechanical and electrical properties of new materials	<p>Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following:</p> <ol style="list-style-type: none"> 1) Layer stacks for gates, junctions and channels: Predictive modeling of dielectric constant, bulk polarization charge, ferroelectric/-magnetic properties, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, transport properties, reliability, breakdown, and leakage currents including band structure, phonon coupling, tunneling from process/materials and structure conditions 2) Models for novel integrations in 3D interconnects including data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. 4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	<p>Ab-initio modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping and doping by chemical functionalization, quantum dots, atomic electronics, multiferroic materials and structures, strongly-correlated electron materials, materials for non-charge-based beyond-CMOS devices.</p>
	<p>Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, ...). Modeling impact of geometry (esp., edge effects / edge roughness), interfaces and bias on transport for carbon-based nanoelectronics (carbon nanotubes and monolayer/bilayer graphene structures).</p>
	<p>Compact models for maturing emerging devices</p>
Optoelectronics modeling	<p>Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling</p>
	<p>Physical design tools for integrated electrical/optical systems</p>
NGL simulation	<p>Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal damage by electron scattering or charging effects)</p>
	<p>Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)</p>



2011 Requirement Tables

Only some general remarks here:

- Continued trend to delay items: Necessary research could not be done due to lack of resources (research funding)
- Several changes in technical details included
- Table continues to contain some items in “zebra” colour - according to ITRS guidelines: “Limitations of available solutions will not delay the start of production. In some cases, work-arounds will be initially employed. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity.”
 - ⇒ This means for simulation: It can be used, but with more calibration, larger CPU time/memory, less generality than in the end required ...
- Red here means “Solution not known, but this does not stop manufacturing”



More details given in ITRS M&S tables

Thank you

