

Test and Test Equipment December 2011 Incheon, South Korea

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Chapter Overview

- Test Drivers & Challenges
- Test & Yield Learning
- Test Cost
- Adaptive Test
- 3D device Test – [New for 2012](#)
- Test Technology Requirements
 - Test parallelism
 - SoC
 - Device types: Logic, Memory, RF/AMS, Specialty Devices
 - Device handling (Handlers, Probers)
 - Device Contacting (probing and package contacting)

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2011 Changes

- Updated Drivers, Difficult Challenges, and opportunities
- New Section on 3D Device Test Challenges
- Major Update to Adaptive Testing section
- Logic / DFT major rewrite
 - Added Fault Expectations using multiple fault models
 - Added test data volume given five compression assumptions
- Test Cost
 - Test cost survey update that quantifies current industry view
- Updates to Logic, SoC, RF, Analog, & Specialty devices

Drivers

Unchanged
Revised
New
Drop

- Device trends

- Increasing device interface bandwidth (# of signals and data rates)
- Increasing device integration (SoC, SiP, MCP, 3D packaging)
- Integration of emerging and non-digital CMOS technologies
- Complex package electrical and mechanical characteristics
- Device characteristics beyond one sided stimulus/response model
- 3 Dimensional silicon - multi-die and Multi-layer
- Multiple I/O types and power supplies on same device
- Fault Tolerant Architectures and Protocols

Drivers

Unchanged
Revised
New
Drop

- Increasing test process complexity
 - Device customization during the test process
 - Feedback data for tuning manufacturing
 - Dynamic test flows via “Adaptive Test”
 - Higher order dimensionality of test conditions
 - Concurrent Test
 - Maintaining Unit level Traceability

Drivers

Unchanged
Revised
New
Drop

- Economic Scaling of Test

- Physical and economic limits of test parallelism
- Managing (logic) test data and feedback data volume
- Managing interface hardware and (test) socket costs
- Balancing General Purpose Equipment vs. Multiple Insertions for System Test and BIST

Difficult Challenges

Unchanged
Revised
New
Drop

- Cost of Test and Overall Equipment Efficiency
 - CoT continues to be the primary driver for innovation
 - Traditional drivers for CoT are starting to be limited by OEE
- Test Development gating volume production
 - Increasing device complexity driving more complex test development
- Detecting Systemic Defects
 - Testing for local non-uniformities, not just hard defects
 - Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects

Difficult Challenges

Unchanged
Revised
New
Drop

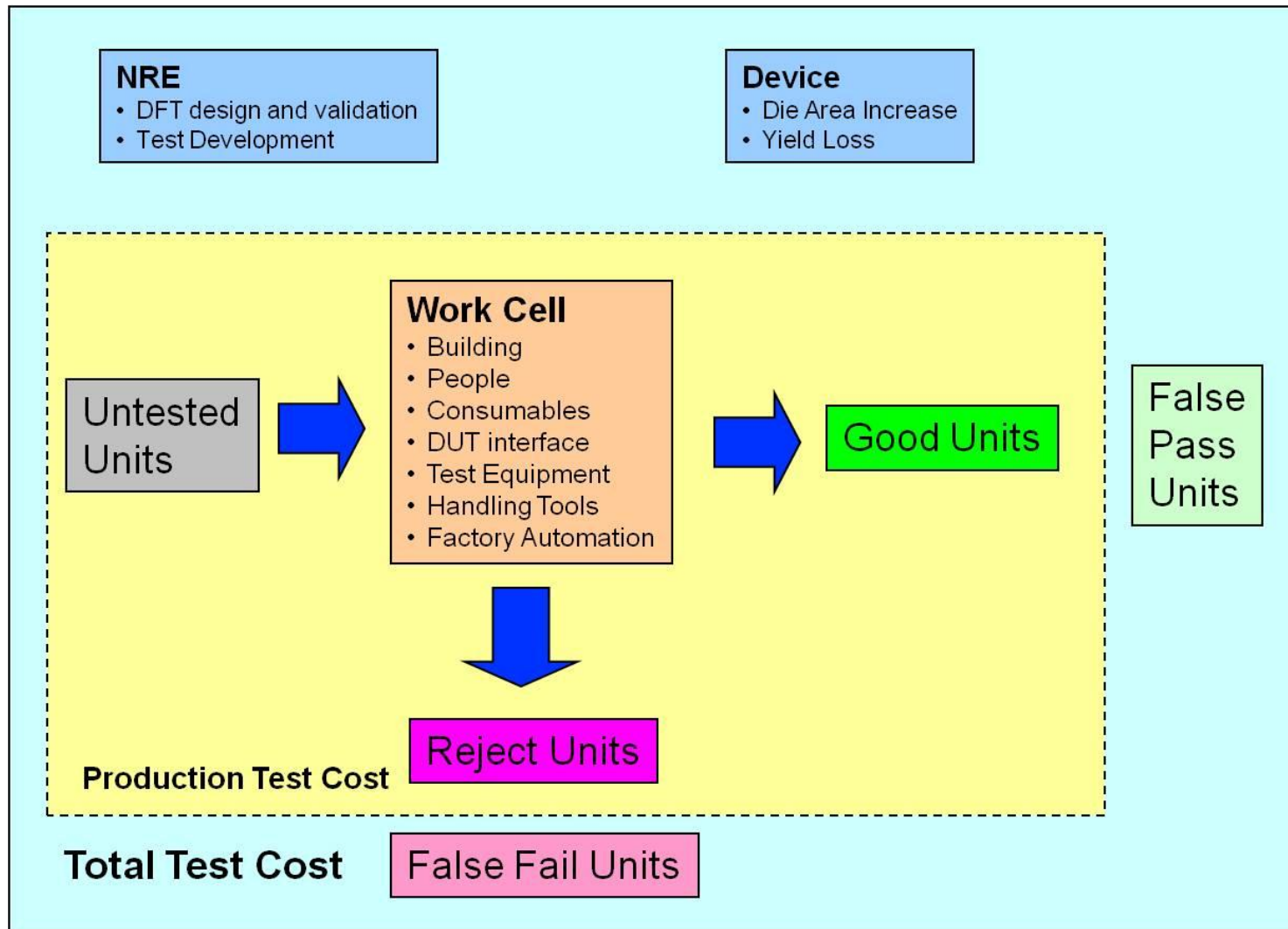
- Screening for reliability
 - Implementation challenges and effectiveness of screens
 - burn-in, IDDQ, and Vstress
 - Erratic, non deterministic, and intermittent device behavior
 - Mechanical damage during the testing process
 - Multi-die stacks/TSV
 - Power Management Issues

Future Opportunities

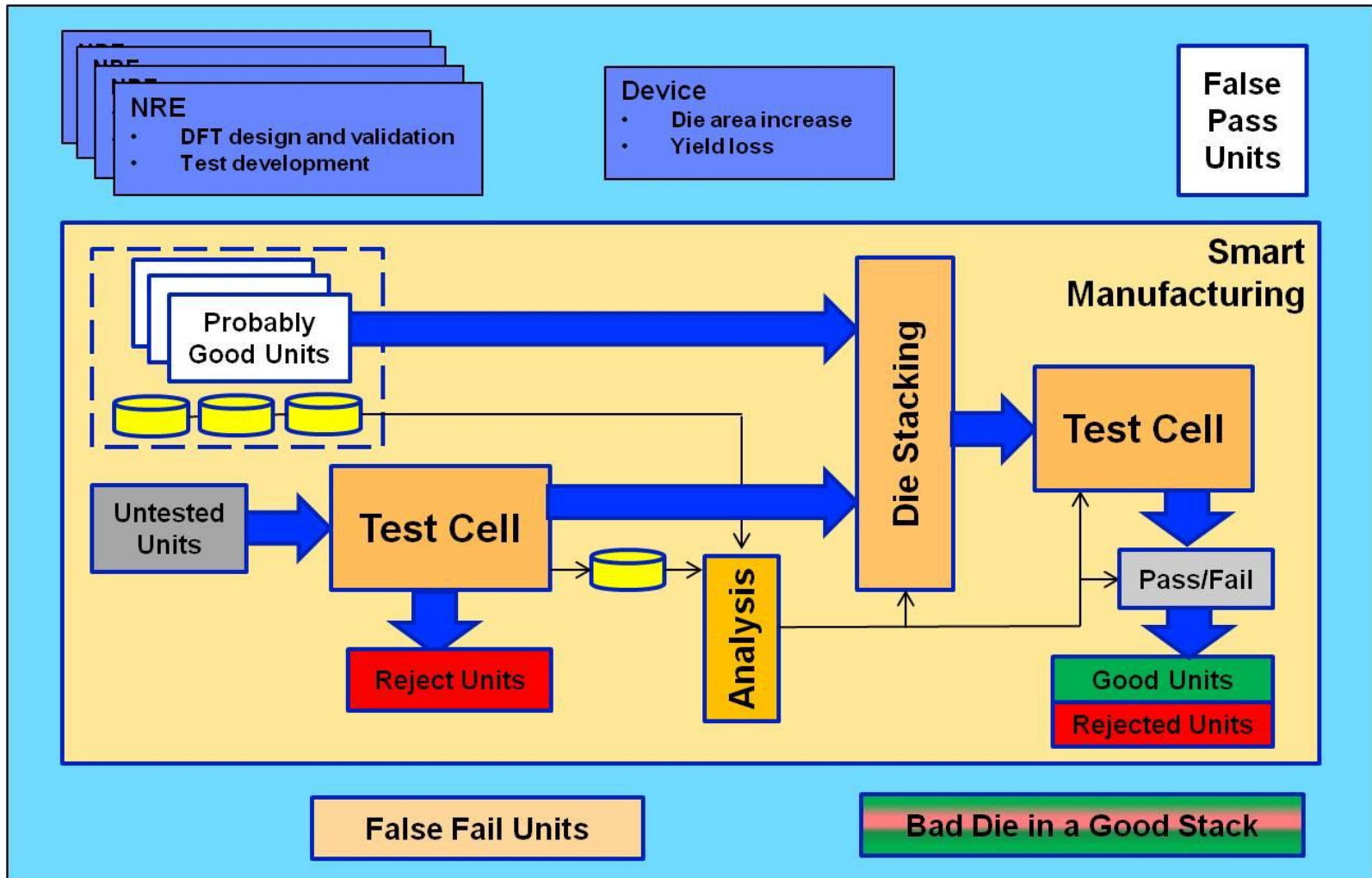
Unchanged
Revised
New
Drop

- Test Program Automation
 - Automatic generation of an entire test program
 - Tester independent test programming language
 - Resolve Mixed Signal test programming challenges
- Scan Diagnosis in the Presence of Compression
- Simulation and Modeling
 - Seamless integration of simulation & modeling into the testing process
 - Move to a higher level of abstraction with Protocol Aware test resources
 - Focused test generation based on layout, modeling, and adaptive feedback
- Convergence of Test and System Reliability Solution
 - Re-use of test collateral in different environments (ATE, Burn-in, System, Field)

Traditional Test Cost Components



3D Test Cost Components



2011 Test Cost Survey Update

Test Cost Metrics

Cost per unit
% of total Product Cost
Cost per second
Cost per megabit

Current Test Cost Drivers

ATE capital
Interface hardware
ATE utilization - NEW
Test program development
Test Time and Coverage

Current cost control Methods

Test Parallelism
Structural Test & Scan
Compression/DFT/BIST/BOST
Adaptive Test
Concurrent Test
Wafer-level at-speed testing

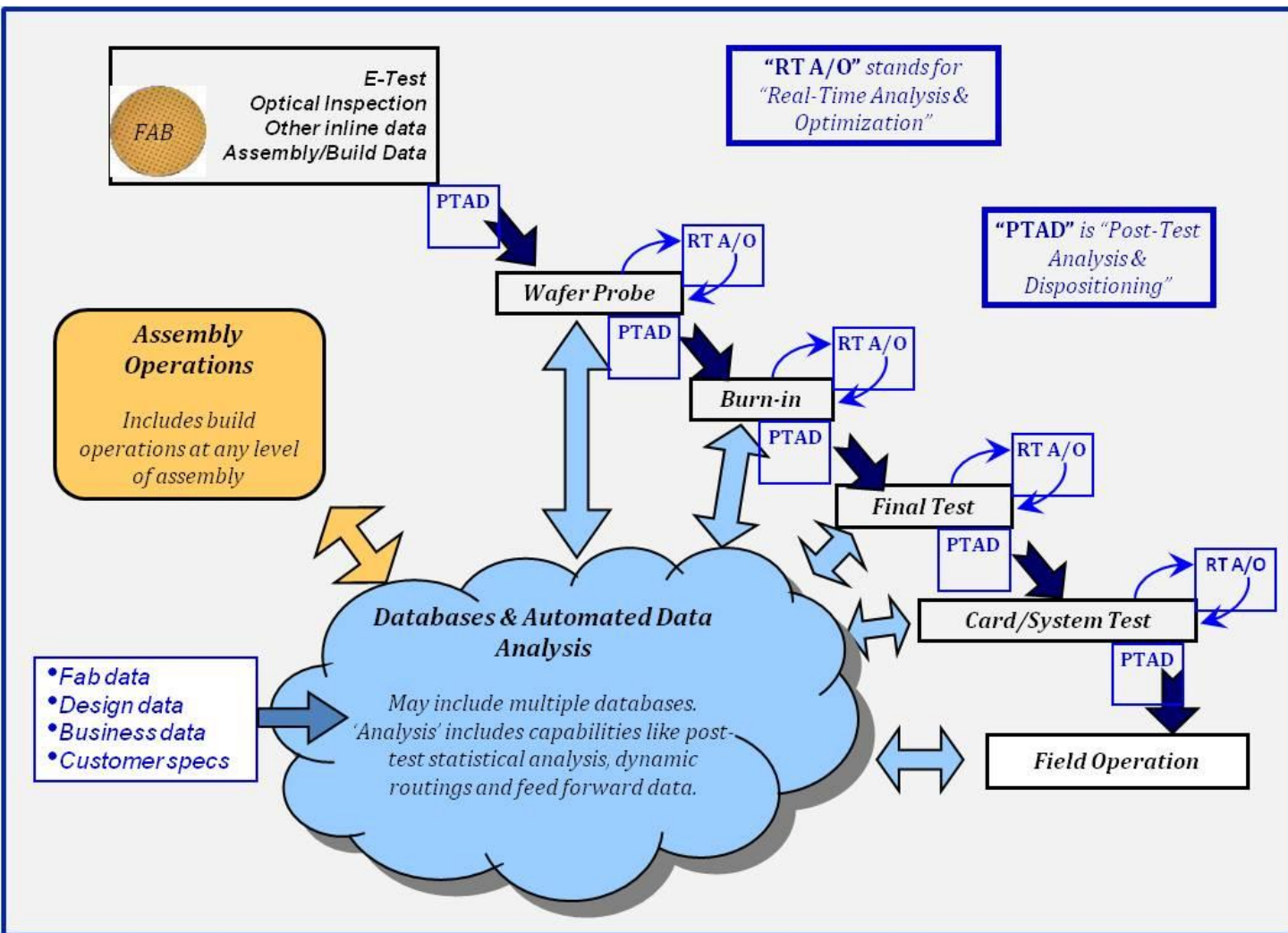
Future Cost Drivers

New Defects and Reliability problems
Test Requirements of packaging
Interfacing - NEW
Data (yield learning, traceability, test data) - NEW

Future cost control Methods

Wafer-level At Speed testing
Advanced embedded instruments
Adaptive Test
New contacting technologies
In system testing - NEW
Built-in Fault Tolerance

Adaptive Test



- Modified testing based on analysis of real-time results
- Benefits
 - Higher Quality
 - Fast Test Time Reduction
 - Lower cost
 - Fast yield learning
- Requires data infrastructure
 - Database
 - Analysis tools
 - Confidence
- Implementation is evolving

3D Device Testing Challenges

- Die level test access to all die in the stack
 - Communication thru the top die in the stack
- Test Flow / Cost / Resources
 - Test partitioning, non-traditional test structure
- Die to Die Interactions
 - Signal routing thru another die
- Debug / Diagnosis
- DFT
- Test data management, distribution, & security
- Power management and implications

2012-2013 Plans

- 3D / “Cube” device test
 - Test step insertion / flow for TSV
 - Manage power & heat
 - Singulated die handling
 - Reliability wafer test requirements
- DFT / BISx via new methods – New Focus Team
 - 3D devices
 - Eliminate digital test data and test programs
 - RF / AMS parametric testing
- 3rd party review of test chapter by users and universities
- Cost & adaptive test section updates
- Logic table refinement
- Concurrent test table addition?

Summary

- 3D stacked devices will change test paradigms
 - The methods and approach seem available
 - Considerable work ahead to implement
- Adaptive testing is becoming a standard approach
 - Significant test data accumulation, distribution, and analysis challenges
- Managing cost is overall challenge
 - Industry is pulling in cost reduction methodology

Thank You!

