ITRS - YE ITWG

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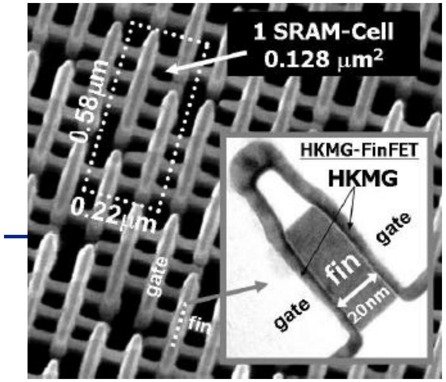
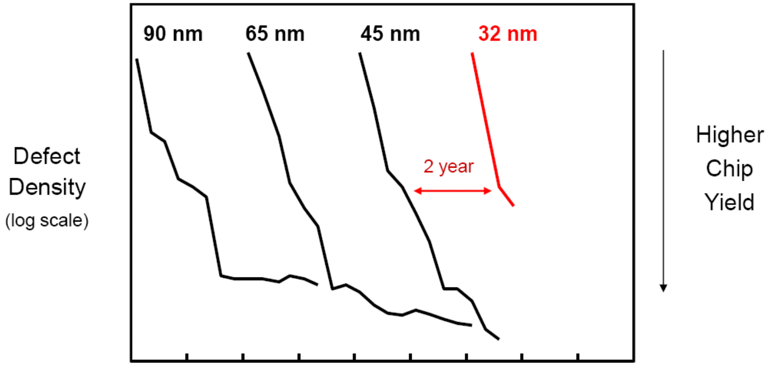
Scope of Yield Enhancement

- Aspects
  - Manufacturing of integrated semiconductor devices: numerous processing steps building the 3D structure of the chip (e.g. 9 Cu and low –k interconnect layers for 32 nm)
  - Yield: percentage of operating chips at the end of the manufacturing process



A bird's-eye view of 0.128µm2 FinFET SRAM cells (post silicide formation) Toschiba,

- Components
  - Determination and control of contamination
  - Inspection of structures and critical dimensions
  - Model to predict and calculate yield based on historic contamination levels (particulate and metals) and defects (failures)
  - Determination of kill ratios: Correlation between defects and yield



45 nm ramp production was the fastest
Presented by Mark Bohr (Intel) 02/2009

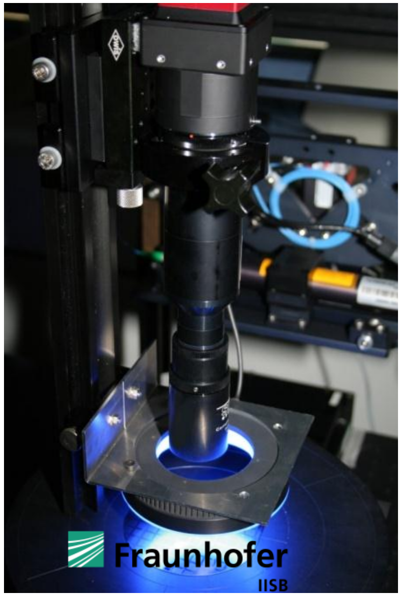
Gordon Moore: "There is no fundamental obstacle to achieving device yields of 100%." (Electronics, 38 (8), 1965)

Example: Inspection for ‘More than Moore’

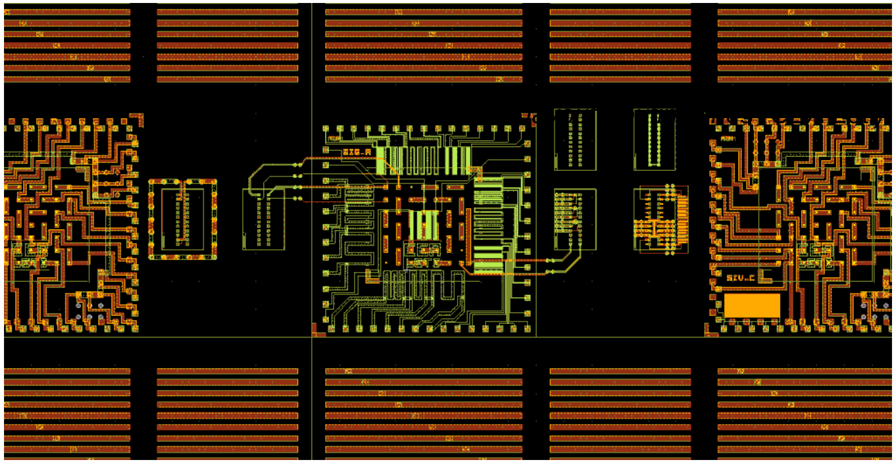
Applications

‘More Moore’
and
‘More than Moore’ technologies

- power electronics
- mechatronics
- MEMS applications
- packaging and assembly
- 3 D integration

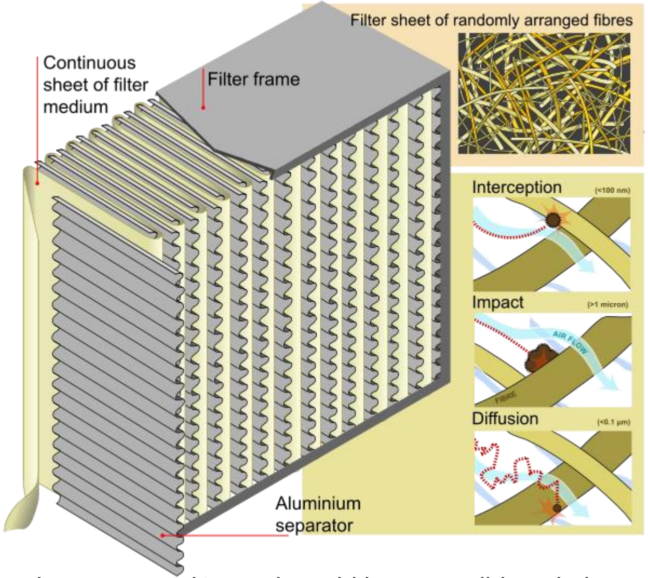


*Laboratory scale inspection setup fulfilling requirements of low cost components and large area inspection (4 mm *4 mm field of view at µm resolution) (example for 3D integration, EC & BMBF funded project JEMSIP3D under contract ENIAC Call 2008 / 120016)*



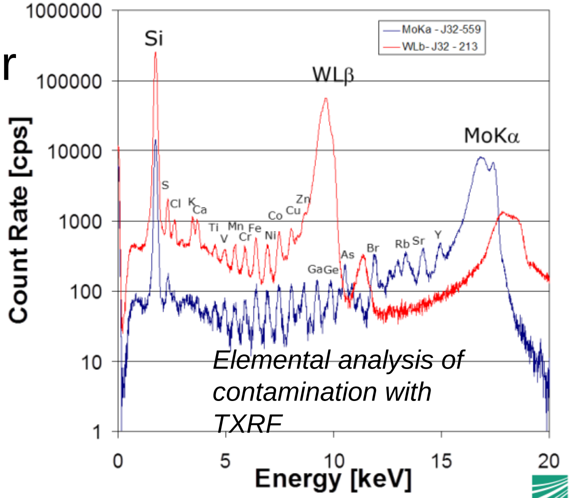
Contamination Analysis for Manufacturing Control

- Drivers
  - ultra clean manufacturing
  - unintended contamination of layers
  - dimensional, structural and compositional information
  - depth resolved quantification
  - non-volatile organic surface contamination
- Analytical Techniques for Manufacturing Control
  - x-ray metrology
  - GCMS
  - TBD

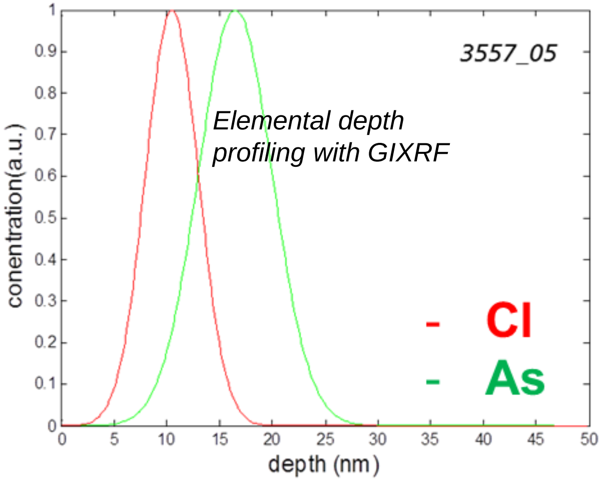


HEPA Filter for contamination free manufacturing (source wikipedia)

For metals, Grazing Incidence X-Ray Fluorescence (GIXRF) could be a possible solution providing dimensional quantification and qualification of surface near elemental contamination.



Elemental analysis of contamination with TXRF

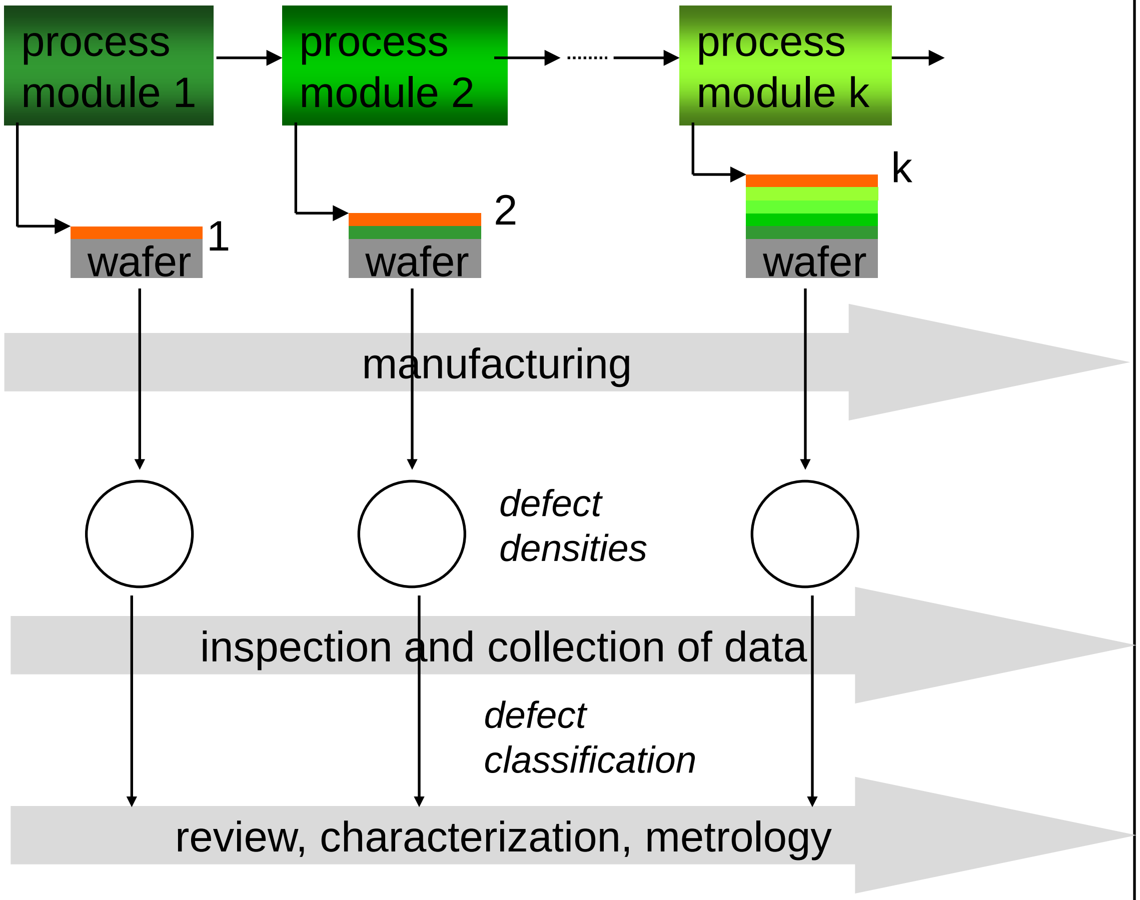


Elemental depth profiling with GIXRF

Fraunhofer
IISB

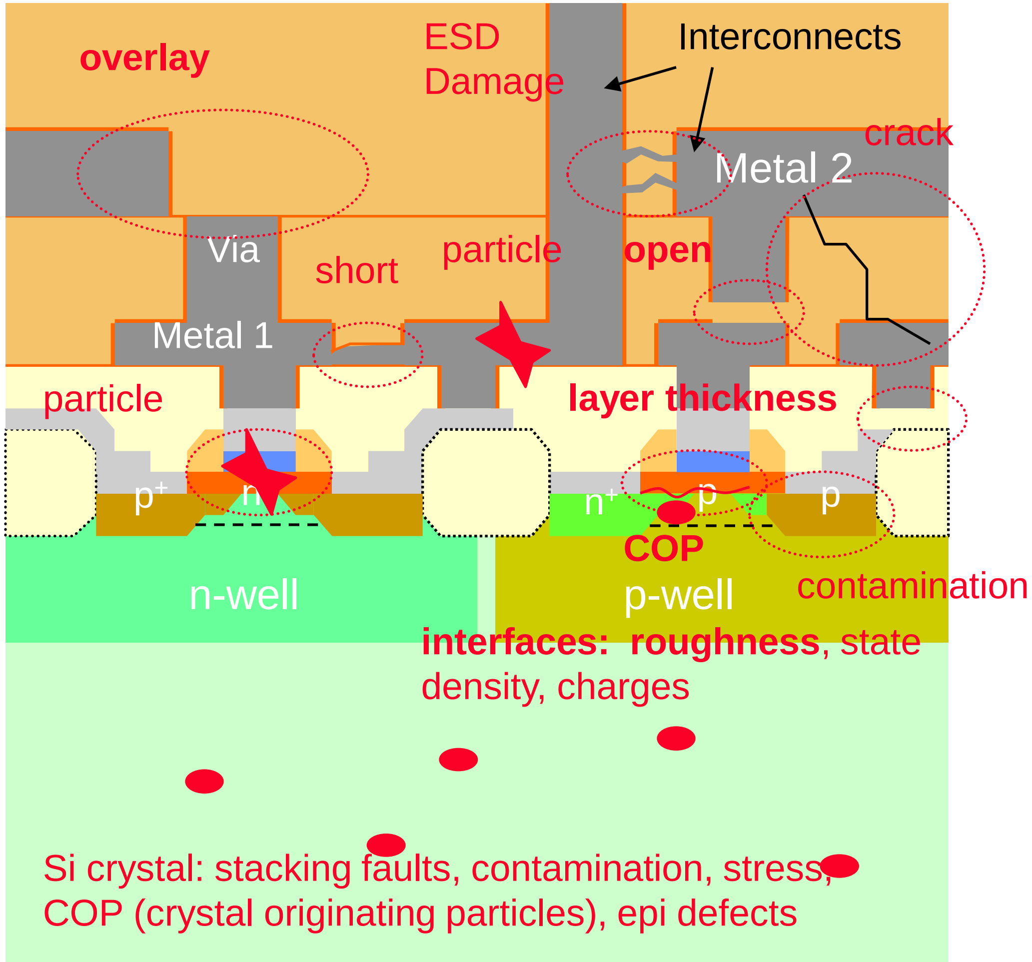
Objectives of Yield Enhancement

- **collect defect data**
  - tools for inspection and root cause analysis
  - automated defect classification and filtering
  - inspection strategy
- **yield management**
  - software
  - objective: to correlate data and find excursions
  - predict yield
- **defect data excursions**
  - define specs
  - procedure for clarification



Defects and Failure Mechanisms

- processes: litho, etch thin film implantation, planarization, cleaning,…
- faults and problems: defects as e.g. particles, flatness, layer properties, patterns, dimensions
- challenges
  - yield and defect map in 2 D
  - root cause analysis requires 3 D
  - model, predict, and forecast yield → YM&DB
  - requires fast and non-destructive inspection (defect density) and metrology (root cause analysis) for 2D and 3D structures → DDC
  - requires preventive defect and contamination control → WECC



(YM&DB: defect budget and yield modelling - DDC:

Organization of the Chapter 2011

- **Chair:** Lothar Pfitzner (Fraunhofer IISB)
  Co-Chair: Dilip Patel (ISMI)

- Difficult Challenges
  - Table YE 2
- Technology Requirements and Potential Solutions
  - Wafer Environment Contamination Control (WECC)
    - Chair: Kevin Pate (Intel) – USA, Andreas Neuber (AMAT) - Europe
    - Table YE 3
  - Characterization, Inspection & Analysis (CIA)
    - Chair: A. Nutsch and I. Thurner – Europe
    - Table YE 4, YE 5, YE 6
  - Yield Learning (YL – not active in 2011)
    - Chair: N.N.; Contributor defined by AMAT
  - Yield Model and Defect Budget (YMDB – not active in 2011)
    - Chair: N.N.

2012 YE ITWG Contributors (please update)

Europe

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Mao-Hsiang Yen (WECC, Winbond)
Cherng Guo (WECC, MXIX)

Malaysia

Guillaume Gallet (WECC, Camfil)

Thank you very much!

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Ravi Laxman (WECC, Air Liquide)
Hubert Chu (WECC, AMAT)
Robert Clark (WECC, TEL)

2011 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- ***Near Term (2012-2018)***
  - ***Detection and identification of Small Yield Limiting Defects from Nuisance -*** It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership and high throughput. Furthermore, it is a dare to identify yield relevant defects under a vast amount of nuisance and false defects.
  - ***Process Stability vs. Absolute Contamination Level –*** This includes the correlation to yield test structures, methods and data are needed for correlating defects caused by wafer environment and handling. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.
  - ***Detection of organic contamination on surfaces –*** The detection and speciation of nonvolatile organics on surfaces is currently not possible in the fab. There is no laboratory scale instrumentation available.

2011 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- ***Long Term (2019-2026)***
  - ***Next Generation Inspection -*** As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node. Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This pathfinding exercise needs to assess each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.

  - ***In - line Defect Characterization and Analysis –*** Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.

  - ***Next generation lithography -*** Manufacturing faces several choices of lithography technologies in the long term, which all pose different challenges with regard to yield enhancement, defect and contamination control.

WECC - Messages

- The WECC sub chapter was placed at the beginning of the yield chapter taking into account the attention of the community to this activity.

- The table YE3 was structured to a side-by-side comparisons of contamination control limits for the clean room environment and for the interior of FOUPs (direct wafer environment). Limit values for YE3 have been checked carefully, reviewed and missing values been added.

- FOUP cross-contamination problems from wafer and material outgassing together with the prevention and assessment of this challenge has been addressed in a so-called integrated approach. The effects of measures determining and controlling FOUP contamination, their effects per process step and q-time have been evaluated together with Factory Integration.

- Potential solutions have been tabulated for the FOUP cross-contamination challenge as well as for monitoring challenges for AMC in the clean room environment.

CIA - Messages

- CIA builds upon the basis of the previous ‘Defect Detection and Characterization’ chapter.

- The scope was defined in 2011 facing the demands in broad applications, e.g. in the area of ‘More Moore’ and ‘More than Moore’ technologies. Also power electronics, mechatronics and MEMS applications, furthermore, characterization, inspection and analysis demands and requirements from packaging and assembly have been taken into account. This major change of the scope was decided in the meetings of 2010/2011.

- Tables and potential solutions will be prepared for the revision in 2013.

Cross Cut Activity 2011 (Yield - Assembly)

- **Goal:** Implementation of Assembly requirements in the YE Roadmap
- **Approach:**
  initial survey
- **Responsible:**
  Ines Thurner (CONVANIT),
  Klaus Pressel (IFX)

ITRS activity between Assembly and Yield Enhancement

General definitions needed:

1. Definition of general questions to find out technology, thruput...
2. Do we need to separate development and volume production?

Initial question list

1. How important is yield monitoring and Improvement for you?
2. Do you have inspection tools to monitor the yield/quality of your process inline
   If yes do you use them
   A) routinely with a sampling
   B) for every part
   C) only if yield problems occur
3. What specification do you have for those inline tools that your are using?
   Thruput
   Sensitivity
   Other specifications
4. What are your major challenges with those tools?
5. Do you have specifications and applications for inline tools you did not find a solution for yet?
   If yes, what are those
6. Do you use offline analysis tools for yield problems
   If yes what are the challenges to transfer those into production?
7. Do you use SPC for the generated inline data?
8. Do you have additional analysis capability to analyze data in order to find tool correlations and yield potentials.
9. Do you see any additional challenges, specifications coming up with your next technologies? If yes, please describe.

Summary Spring 2011

- **Defect Budget Survey:**
  - two contributors from Europe identified in 2010
  - no Asian and US contribution
  - → subTWG suspended, see below

- **Organisation:**
  - the subchapters YL and DB&YM are suspended as a consequence of missing support from Asia & US & IDM
    Consequently, YE will not to be able to supply Electrical Defect Densities for ORCT tables!
  - the subchapter Defect Detection & Characterisation (DDC) will change to Characterization, Inspection & Analysis (CIA)
    - Scope:
      - supply tool specifications for leading edge defect density characterization & More than Moore
      - define requirements in the future for wafer contamination analysis on the surface, at interfaces and in the bulk
    - Contributors: IDM, Suppliers, WECC, P&A, MEMS

- **WECC (new):**
  - separation of reticle environment and wafer environment
  - separation of FOUP, RSP (Reticle Single Pod) and ambient environment

  → improvement / clarification of table YE7 proposed by Japan TWG

- **CTWG Meeting**
  - Include YE in back-end
  - Leading edge vs. MtM vs. mainstream technology

Summary Summer 2011

- **Efficient meeting of WECC**
  - AMC: solution tables were done; X-TWG activity with Factory Integration
  - UPW: organic speciation and particle risk model discussions continued
  - Precurser tables were discussed and updated
- **Improvement seen in CIA (characterization, inspection, analysis)**
  - Follow-up by telecon
  - Invite broader IDM community
- **Efficient X-TWG meetings with A&P, Interconnect, Litho, Test, Metrology, FEP, Factory Integration for clarification of open questions**

Outlook

Development/ Improvement of the Yield Enhancement chapter

- Reflection of current status and future requirements needs subsequent adjustment of outline and content of the chapter

- Determine the requirements for manufacturing by establishment of
  - Wafer Environment Contamination Control
  - Characterization, Inspection & Analysis
  - *Yield learning*
  - *Defect Budget and Yield Models*
- Enhance the contribution to the Yield Enhancement Chapter by:
  - Request to IDMs, ESIA, JEITA, KSIA, SIA, TSIA, ISMI, academia.
  - Broader invitation to equipment and metrology suppliers and software companies.

Please contribute further to YE Chapter

“Any contribution improves the roadmap. The Yield Enhancement Chapter reflects the needs for high yielding manufacturing of new technologies in the future. This supports your R&D and manufacturing efforts for new technologies and products.“