

Front End Processes

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2011 Winter Meeting FEP ITWG Participants

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2011 ITRS FEP Sub-TWG Leadership

- HP MPU ASIC - FEP 2
- LOP - FEP 3
- LSTP - FEP 4
 - Prashant Majhi (US)
 - Wei-Yip Loh (US)
- DRAM - FEP 5
 - Ho Jin Cho (KR)
- Floating Gate Flash - FEP 6
 - Mauro Alessandri (EU)
- Charge Trapping Flash - FEP 7
 - Mauro Alessandri (EU)
- PCM - FEP 8
 - Mauro Alessandri (EU)
- FeRAM - FEP 9
 - Yukinobu Hikosaka (JP)
- Starting Materials - FEP 10
 - Mike Walden (US)
 - Mike Goldstein (US)
- Surface Preparation - FEP 11
 - Joel Barnett (US)
- Therm/Thin Films/Doping - FEP 12
 - Prashant Majhi (US)
- Etch - FEP 13
 - Tom Lii (US)
- CMP - FEP 14
 - Darryl Peters (US)



Flash NOR/NAND Update

- Continue Flash NOR Roadmap through 2012 (still high demand)
- Consider the end of the life / removal of NOR Flash for next major ITRS revision in 2013
- Technology nodes and dielectric thickness based on ORTC tables and PIDS survey
- Added floating gate formation complexity for NAND due to low thickness, variable doping and mixed material scenarios
- Added control gate material scenarios
- Removed program/erase window since program/erase degradation not directly related to technology requirements
- Removed inter-poly dielectric conformality due to the evolution toward almost planar dielectrics



Phase Change Memory

- Continue PC Memories roadmap with update in numbers until next major update (2013)
- Monitoring implementation in production during 2012 with possible changes in roadmap timing
- Technology node reviewed in agreement with PIDS
- No change in table parameters, all numbers updated

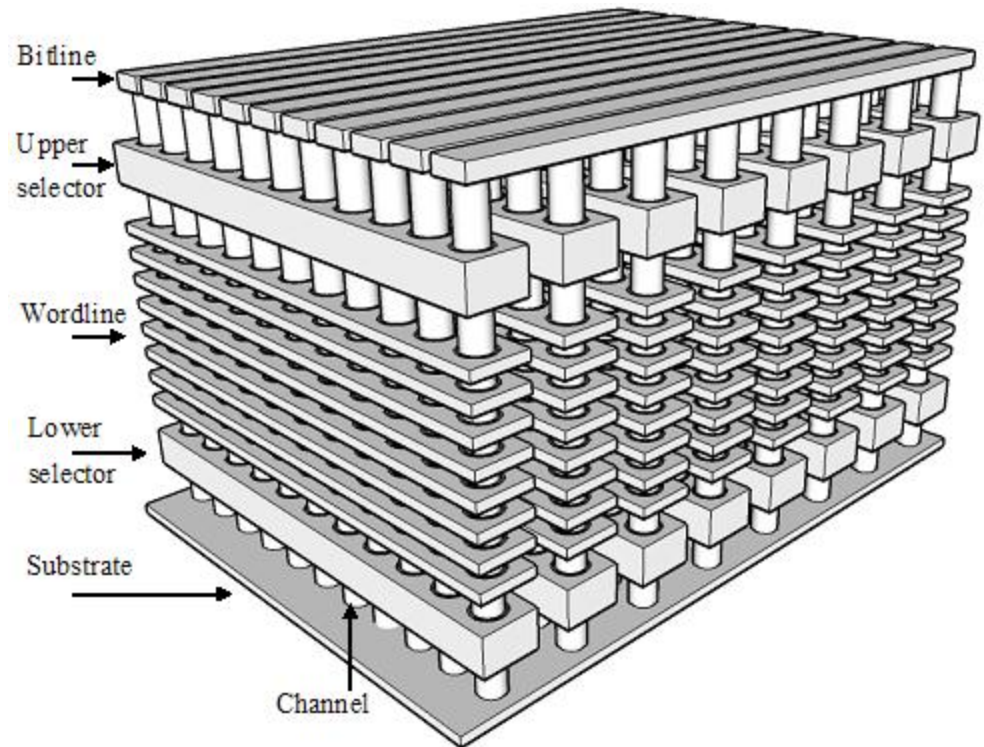
FeRAM

- Table parameters, general trends are unchanged



Charge Trap Memory

- Kept the current structure for planar CT NAND, all numbers updated
- 3D Memory requirements added as text - focus was on array with vertical channel and horizontal gate, which are the most widely published.
- Focus and discussion on 3D FEOL most critical parameters:
 - channel Si filling and properties (grain size, etc.)
 - Interface between channel Si and tunnel dielectric
 - Conformal and controlled formation of active dielectrics



Starting Materials

- Updated various table entries impacted by revised DRAM half-pitch values, chip and active transistor areas
- Reduced process-induced silicon removal from 10 to 5 nm for SOI thickness calculations
- Adjusted colorization to account for current capabilities versus the revised entries
- Noted 300 / 450mm parallel wafer diameter scenario in table reference
- Modified footnotes B, C, G and H to identify “pinning” of trend values that would actually be relaxed as a result of decreasing chip areas
- Updated potential solutions figure to capture 2011 status



Starting Materials (cont.)

- Continue to monitor industry activities related to 450mm development and assess impact on the Starting Materials table entries
- Treated edge roll-off in chapter text - continue to assess adding metrics (model development dependent) in future updates
- Considered the possible impact to wafer flatness requirements assuming adoption of EUV for lithography, again treated in chapter text



Surface Preparation

- Deleted the line “Silicon and oxide loss (Å) requirement per DRAM LDD clean step – significantly higher than the 0.1Å requirement for microprocessors.
- Included SiN loss metrics and corresponding text
- Added Metal capacitor loss requirement for DRAM, and corresponding text
- Changed per-clean-step Yield value in table from 99 to 99.9% and generated corresponding values
- Added row in for counts based on 65nm sized particles
- Added lines differentiating change to 450 mm and constant 300 mm wafer size requirements
- Reduced C spec to $1E12$ a/cm² – to reflect epi requirements
- Added Highly Selective Etch as a Category needing potential solutions



Surface Preparation

Table FEP11 Front End Surface Preparation Technology Requirements

Year of Production	Driver	Module	2011	2012	2013	2014	2015	2016
DRAM ½ Pitch (nm) (contacted)	DRAM		35.7	31.8	28.3	25.3	22.5	20.0
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	MPU/ASIC		38	32	27	24	21	18.9
MPU Physical Gate Length (nm)	MPU		24	22	20	18	17	15.3
Wafer diameter (mm)	D ½, M		300	300	300	450	450	450
Wafer edge exclusion (mm)	D ½, M		2	2	2	2	2	2
Front surface particles								
Killer defect density, $D_p R_p$ (#/cm ²) [A]	D ½	Gate	0.004	0.005	0.007	0.004	0.006	0.007
Critical particle diameter, d_c (nm) [B]	D ½	Gate	◆17.9	◆15.9	◆14.2	◆12.6	◆11.3	◆10.0
Critical particle count, D_{pw} (#/wafer) [C] 300 - 450 mm (99.9%) - Based on Critical Particle Diameter	D ½	Gate	◆12.6	◆12.6	◆12.6	◆34.2	◆34.2	◆34.2
Critical particle count, D_{pw} (#/wafer) [C] 300 - 450 mm (99.9%) 65nm	D ½	Gate	◆0.95	◆0.95	◆0.95	◆1.1	◆1.1	◆1.1
Critical particle count, D_{pw} (#/wafer) [C] 300 mm only (99.9%) Based on Critical Particle Diameter	D ½	Gate	◆12.6	◆12.6	◆12.6	◆12.6	◆12.6	◆12.6
Critical particle count, D_{pw} (#/wafer) [C] 300 mm only (99.9%) 65 nm	D ½	Gate	◆0.95	◆0.95	◆0.95	◆0.57	◆0.57	◆0.57

- Lines added for 300 mm and 300-450 mm wafer diameter approaches; particle counts for 65 nm sized particles
- 99.9% Gate Yield used for Calculations



Logic, Thermal, Thin Films, Doping

- Introduction of high mobility channels (year currently targeted at 2018) added into current tables
- Multi-gate device still listed as 2015 but recognized potential to pull in by as much as 3 years (2012 proposal)
- Ongoing efforts to match with PIDS on V_{dd} scaling and use common (with PIDS and design) V_{dd} , CV/I , I_{on} , I_{off} numbers employed to re-calculate the module specifications for FEP's HP, LSTP, LOP tables



Etch

- Y2012 wafer-to-wafer and lot-to-lot gate CD variation solution achieved with availability of advanced process control (APC)
- On etcher scatterometry gate CD measurement capability urgently needed to further improve wafer-to-wafer and lot-to-lot gate CD variation beyond Y2012



Etch

Potential Solutions

- **Fast switching gas and continuous plasma are under qualification for improving etch chamber throughput and CoO.**
- **Inert species low energy photo resist implant demonstrates great potential for improving line width roughness (LWR) issue.**



CMP Summary

- Obtained metrics from end users for RMG (POP and metal polish)
- Need to evaluate adding PCMP cleans for STI and HKMG, targeting 2013 revision
- Currently determining post CMP clean requirements for 2012 update



FEP Summary

- **Tables updated**
 - 300 mm and 300 → 450 mm approaches addressed
- **High-κ metal gate in high-volume manufacturing**
- **FinFET introduced sooner than expected**
- **SOI continues to make progress**
- **III-V high-mobility channels in research – 2018 introduction with ongoing assessment of timing**

