

ITRS - YE ITWG

**Conference in Hsin Chu (Taiwan)
December 16, 2009**

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International Technology Roadmap for Semiconductors

Hsin Chu December 16, 2009

Hsin Chu 2009 YE ITWG Participants

- 9 Participants (Europe, Japan, USA)
 - Takashi Futatsuki (Organo) WECC
 - Guillaume Gallet (camfil Farr) WECC
 - Astrid Gettel (GF) WECC
 - Jost Kames (artemis control) WECC
 - Hidehiro Masuko (ShinEtsu) WECC
 - Andreas Neuber (AMAT) WECC
 - Dilip Patel (ISMI) co-chair DDC
 - Lothar Pfitzner (IISB) – chair DDC
 - Yoshimi Shiramizu (NEC Electronics) WECC



Organization of the Chapter 2010

- **Chair:** Lothar Pfitzner (Fraunhofer IISB)
Co-Chair: Dilip Patel (ISMI)
- Difficult Challenges
 - Table YE 2
- Technology Requirements and Potential Solutions
 - Yield Learning (YL – not active – plan to reactivate 2010)
 - Chair: N.N.; Contributors to be defined by Samsung, AMAT
 - Yield Model and Defect Budget (YMDB – not active in 2010)
 - Chair: Sumio Kuwabara (NEC) - Japan
 - Table YE 3, (Deleted Tables →YE 4, YE 5)
 - Defect Detection and Characterization (DDC)
 - Chair: N.N. (Proposal D. Patel)
 - Table YE 6, YE 7, YE 8
 - Wafer Environment Contamination Control (WECC)
 - Chair: Kevin Pate (Intel) – USA, Andreas Neuber (AMAT) - Europe
 - Table YE 9



2009 YE ITWG Contributors

Europe

Ines Thurner (DDC; Qimonda)
Lothar Pfitzner (Chair; Fraunhofer IISB)
Andreas Nutsch (DDC; Fraunhofer IISB)
Andreas Neuber (WECC; Applied Materials)
Benoit Hirschberger (DDC; ST)
Astrid Gettel (WECC, Global Foundry)
Guillaume Gallet (WECC, Camfil Farr)
Jan Cavelaars (DDC; Crolles 2/ NXP)
Dieter Rathei (YMDB; DR Yield)
Francois Finck (DDC/YMDB; ST)
Christoph Hocke (WECC; Infineon)
Francesca Illuzzi (WECC; ST)
Hubert Winzig (WECC; Infineon)
Michael Lurie (WECC; Tower)
Michael Otto (WECC; Fraunhofer IISB)
Wolfgang Sievert (WECC, Honeywell)
Jochen Ruth (WECC, PALL)

Japan

Fumio Mizuno (DDC; Meisei Univ.)
Masakazu Ichikawa (DDC; Tokyo Univ.)
Isao Kojima (DDC; AIST)
Eiichi Kawamura (DDC; Fujitsu)
Akira Okamoto (WECC/DDC; Sony)
Yoshinori Nagatsuka (DDC; SEIKO-EPSON)
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Koichi Sakurai (DDC/YMDB; Renesas)
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Masahiko Ikeno (DB&YM; Hitachi HT)
Sumio Kuwabara (DB&YM; NEC EL)
Takanori Ozawa (YL/YMDB; Rohm)
Yoko Miyazaki (DDC; Accretech)
Yoshimi Shiramizu (WECC; NEC EL)
Yuichiro Yamazaki (DDC; Toshiba)
Ryu Shioda (YL, Agilent)
Katsunobu Kitami (WECC, Kurita)
Takahiko Hashidzume (DDC, Panasonic)
Kazuhiro Honda (DDC; JEOL)
Takashi Futatsuki (WECC; Organo)

Korea

Uri Cho (; Samsung)
Hyun Chul Baek (; Hynix)
Sang KyuPark (; Magna Chip)

Taiwan

Tings Wang (YL; Promos)
CS Yang (Winbond)
CH Chang (; SIS)
ChanYuan Chen (; TSMC)
CS Yang (; Winbond)
Jim Huang (; UMC)
Jimmy Tseng (; PSC)
Len Mei (; Promos Tech)
Steven Ma (; Mxic)

United States (cont.)

Dave Roberts (WECC; Air Products)
David Blackford (WECC, FMT)
Diane Dougherty (WECC;)
Dimitry Znamensky (WECC;)
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Frank Flowers (WECC; FMC)
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Jeffrey Hanson (WECC; TI)
Jian Wei (WECC; Mykrolis)
Jill Card (, Exponent)
John Degenova (WECC; TI)
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Joseph O'Sullivan (WECC; Intel)
Keith Kerwin (WECC; TI)
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Mark Camenzind (WECC; Air Liquide)
Mark Crockett (WECC; Applied Materials)
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Rick Udischas (WECC; Ais Liquide)
Rob Henderson (WECC; YieldService)
Biswanath Roy (WECC; Pall)
Sarah Schoen (WECC; Air Liquide)
Slava Libman (WECC; Intel)
Scott Anderson (WECC; Air Liquide)
Scott Covington (WECC, Purita)
Stephen Toebes (WECC; Brooks)
Steve Hues (WECC; Micron Technology)
Terry Stange (WECC; Hach Ultra)
Tony Schleisman (WECC; Air Liquide)
Tracey Boswell (WECC; Sematech)
Val Stradzs (WECC; Intel)
William Moore (WECC; IBM)
James S. Clarke (DDC; Intel)
Kevin Sequin (WECC; Donaldson)

Thank you very much!

United States

Dilip Patel (Co-chair, DDC, Intel)
Kevin Pate (WECC, Intel)
J. Ritchison (DDC; TI)
James Dougan (DDC; Freescale)
Allyson Hartzell (WECC; Exponent)
Aaron Shupp (WECC, PMS)
Andrew Bomber (WECC, Intel)
Barry Gotlinsky (WECC; Pall)
Bart Tillotson (WECC; Fujifilm Electronic
Materials)
Billy Jones (WECC; Qimonda)
Bob Latimer (WECC;)
Chris Long (WECC; IBM)
Chris Muller (WECC; Purafil)
Dan Rodier (WECC; PMS)
Dan Fuchs (WECC, BOCE)
Dan Wilcox (WECC; Spansion)



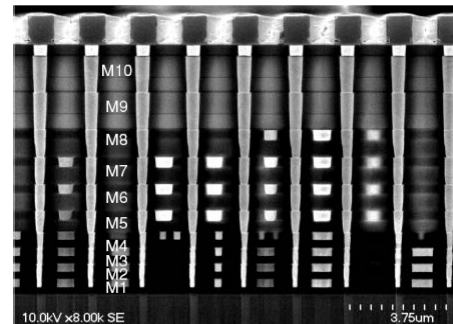
International Technology Roadmap for Semiconductors

Hsin Chu December 16, 2009

Scope of Yield Enhancement

- Aspects

- Manufacturing of integrated semiconductor devices: numerous processing steps building the 3D structure of the chip
- Yield: percentage of operating chips at the end of the manufacturing process

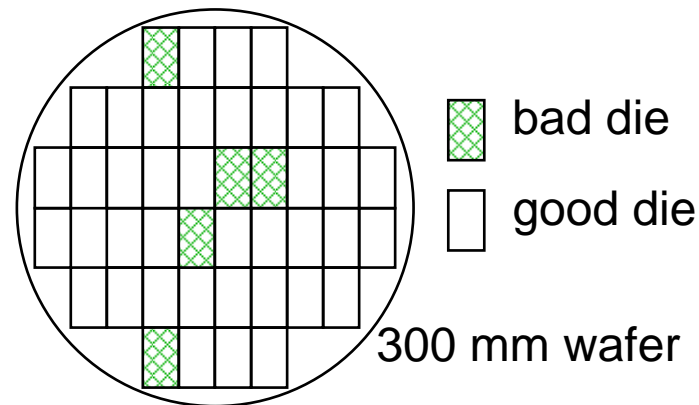


Takayuki Ohba, 21 FUJITSU Sci. Tech. J., 38,1,(June 2002): Cross-sectional SEM picture of 10-level Cu dual-Damascene structure fabricated using SiLK™ at the lower level (minimum feature size from M1 to M4) of multilevel interconnects.

- Components

- Determination and control of contamination
- Inspection of structures and critical dimensions
- Model to predict and calculate yield based on historic contamination levels (particulate and metals) and defects (failures)
- Determination of kill ratios: Correlation between defects and yield

$$\text{Yield} = \frac{\text{good die}}{\text{good die} + \text{bad die}}$$

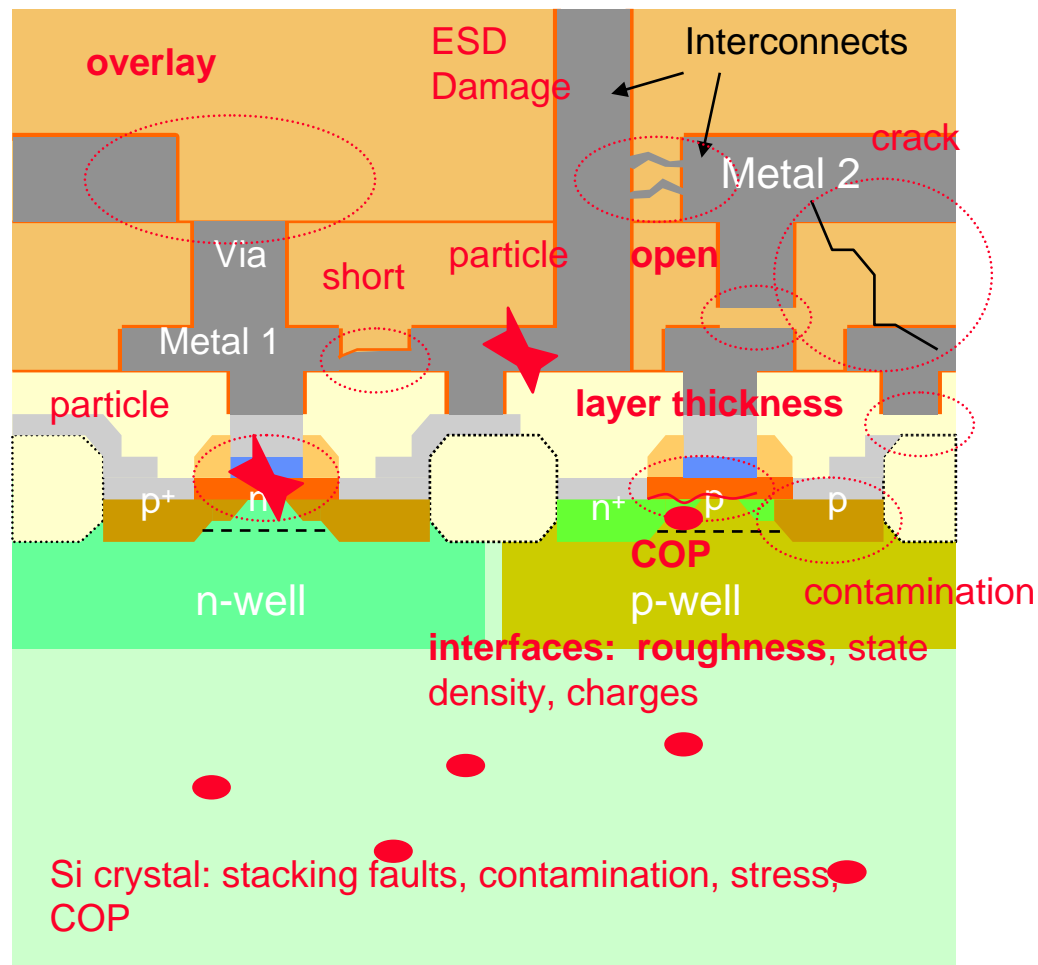


*Gordon Moore: "There is no fundamental obstacle to achieving device yields of 100%."
(Electronics, 38 (8), 1965)*



Defects and Failure Mechanisms

- processes: litho, etch thin film implantation, planarization, cleaning,...
- faults and problems: defects as e.g. particles, flatness, layer properties, patterns, dimensions
- challenges
 - yield and defect map in 2 D
 - root cause analysis requires 3 D
 - model, predict, and forecast yield → **YM&DB**
 - requires fast and non-destructive inspection (defect density) and metrology (root cause analysis) for 2D and 3D structures → **DDC**
 - requires preventive defect and contamination control → **WECC**



Revision: 2009 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- **Near Term (>16 nm)**
 - **Detection of Multiple Killer Defects / Signal to Noise Ratio** - Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.
 - **Non-Visual Defects and Process Variations** – Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.
 - **Process Stability vs. Absolute Contamination Level** – Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.
 - **Wafer Edge and Bevel Monitoring and Contamination Control** – Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems.



Revision: 2009 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- **Long Term (<16 nm)**
 - **Next generation inspection systems** – End of the capabilities of optical inspection.
 - **In - line Defect Characterization and Analysis** – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.
 - **Development of model-based design-manufacturing interface** – Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.
 - **Introduction of 450 mm wafers** – The introduction of 450 mm wafers is expected to impact the defect detection and characterization but as well defect budgets and yield models due to the large surface of the substrate. The introduction of 450 mm wafers requires a new generation of inspection tools.
 - **3D Inspection** – For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.



Introduction of 450 mm substrates

Impact of 450 mm Wafer Diameter on Equipment and Metrology

Diameter	300 mm	450 mm
Thickness	775 μm	925 μm
Area	706 cm^2	1589 cm^2

Impacted Areas	Focus Items
Processes	uniformity of processes, contamination, thermal effects/uniformity, (cleaning, polishing, deposition, etch, anneal, ..)
Lithography	increase of area by 2.25 times requires high performance – high speed litho
Handling	deformation (\rightarrow stress), transport issues, wafer translation (large distances, acceleration and settling times increase, vertical drift along the wafer)
Metrology	stages and handling, mapping capabilities, increase of area by 2.25 times requires high performance – high speed metrology (inspection), dimensional change due to thermal expansion coefficient, ...
Data Management	amount of data, data quality, ...



Revision: New 2009 Key Challenges

- ***Introduction of 450mm substrates*** - The introduction of 450mm wafers is expected to impact the defect detection and characterization but as well defect budgets and yield models due to the large surface of the substrate. The introduction of 450mm wafers requires a new generation of inspection tools.
 - The cost of ownership is impacted by throughput and tool cost. It will be difficult to maintain the throughput of inspection tools at the 450mm wafer size. Therefore, the tool costs are crucial.
 - 450mm handling for inspection has the risk of large substrate flexibility but also coordinate accuracy required for defect review.
 - Due the large surface a huge amount of inspection data will be obtained. Improvement of data quality and reduction of the amount of data will be important. Defect budgets and yield models are impacted by the unknown defect densities on the large substrates.



Revision 2009

- **Overall**
 - confirmation of key challenges
 - introduction of 450 mm as a new challenge
 - ISMI → to organize a new defect budget survey
- **DDC**
 - adjust tables to ORCT input
 - update colours and numbers
- **DB & YL**
 - outline for defect budget survey presented
 - discuss non – visible defects
 - Tables were deleted (not up to date)



Revision 2009

- **WECC:**

Focus items (Ultrapure Water, Chemicals, Gas, Airborne/Surface Molecular Contamination)

- Particles: Measurement, composition, critical size, identify yield correlation, deposition model
- Organics: Measurement, speciation, identify yield correlation, deposition model
- Ions and molecular contamination: Deposition model
- CVD/ALD precursor contamination control requirements
- Airborne Molecular Contamination integrated control concept, metrology requirements



Development/ Improvement of the Yield Enhancement chapter

- Reflection of current status and future requirements needs subsequent adjustment of outline and content of the chapter
- Request to IRC to encourage IDMs, JEITA, KSIA, TSIA academia contributing to ITRS to work with ISMI:
 - assure that sufficient contributors and resources are available
 - surveys required for future updates e.g. DB&YM

