2009 ITRS ORTC

Public Presentation 12/16/2009

Allan - Rev 1, 12/16/09

Work in Progress – Do Not Publish!

7/15 2009 ITRS ORTC Pre-Summary

1) ORTC Model Completed and delivered to TWGs for San Francisco TWG Interdependency Preparation
   1) MPU Model completed based upon Design TWG model proposals
   2) Memory Chip Size and density models complete based on Brussels proposal presentation by PIDS
   3) Some new features:
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      2) “Equivalent Scaling” Timing updated and compared to “Dimensional” Trends
      3) “More than Moore” white paper to be added to ITRS website at www.itrs.net
2) MPU M1 Update
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   3) Plus Smaller 60f^2 Design TWG SRAM 6t cell Design Factor
   4) Plus Smaller 175f^2 still proposed Logic Gate 4t Design Factor
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    1) Utilized Design TWG Model for Chip Size and Density Model trends – tied to technology cycle timing trends and updated cell design factors
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2007 ITRS Executive Summary Fig 4

Moore's Law & More

✓New work In 2009

Traditional ORTC Models

Functional Diversification (More than Moore)

Analog/RF | HV Power | Passives | Sensors Actuators | Biochips

Scaling (More Moore)

[Geometrical & Equivalent scaling]

Baseline CMOS: CPU, Memory, Logic

130nm
90nm
65nm
45nm
32nm
22nm
. . .
V

Interacting with people and environment

Non-digital content System-in-package (SiP)

Information Processing

Digital content System-on-chip (SoC)

Combining SoC and SiP: Higher Value Systems

Beyond CMOS

New in 2009:
- ✓ More than Moore "White Paper"
- ✓ More Commentary In ITWG Chapters

New in 2009:
- ✓ Survey updates to ORTC Models
- ✓ Equivalent Scaling Roadmap Timing Synchronized with PIDS and FEP

Online in 2008:
- ✓ SIP "White Paper" www.itrs.net/papers.html

New in 2009:
- ✓ Research and PIDS transfer timing clarified
- ✓ Work underway to identify next storage element

Source: 2009 ITRS - Executive Summary Fig 1

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[2009 – Unchanged]

2007/08 ITRS "Moore's Law and More" Alternative Definition Graphic

Baseline CMOS	Memory	RF	HV Power	Passives	Sensors, Actuators	Bio-chips, Fluidics

"More Moore"

"More than Moore"

Computing & Data Storage

Sense, interact, Empower

Heterogeneous Integration

System on Chip (SOC) and System In Package (SIP)

Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

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[2009 – Unchanged]

2008 ITRS "Beyond CMOS" Definition Graphic

Baseline CMOS	Ultimately Scaled CMOS	Functionally Enhanced CMOS	Nanowire Electronics	Ferromagnetic Logic Devices	Spin Logic Devices

32nm | 22nm | 16nm | 11nm | 8nm

Multiple gate MOSFETs

Channel Replacement Materials

Low Dimensional Materials Channels

New State Variable

New Devices

New Data Representation

New Data Processing

Algorithms

"More Moore"

"Beyond CMOS"

Computing and Data Storage Beyond CMOS

Source: Emerging Research Device Working Group

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"Equivalent Scaling Process Technologies Timing"

New for 2009

[PIDS/FEP – "Simplified Transistor Roadmap"] - [Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs (ENIAC Graphic)]

Source: 2009 ITRS - Exec. Summary Fig 7c

[Orig. Source: ITRS, European Nanoelectronics Initiative Advisory Council] (ENIAC)

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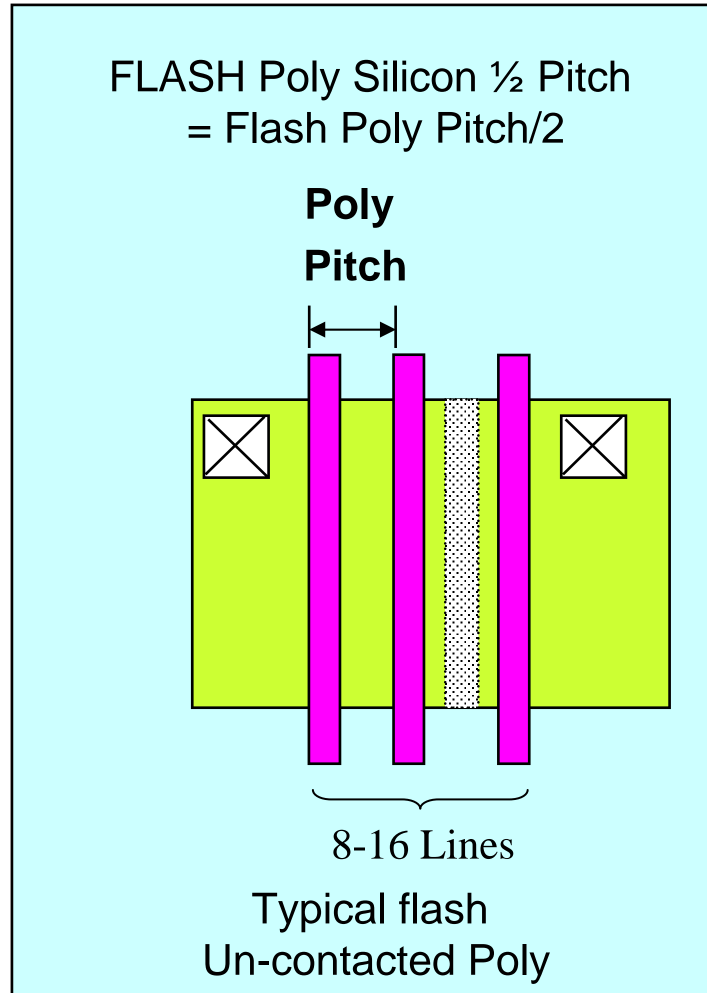
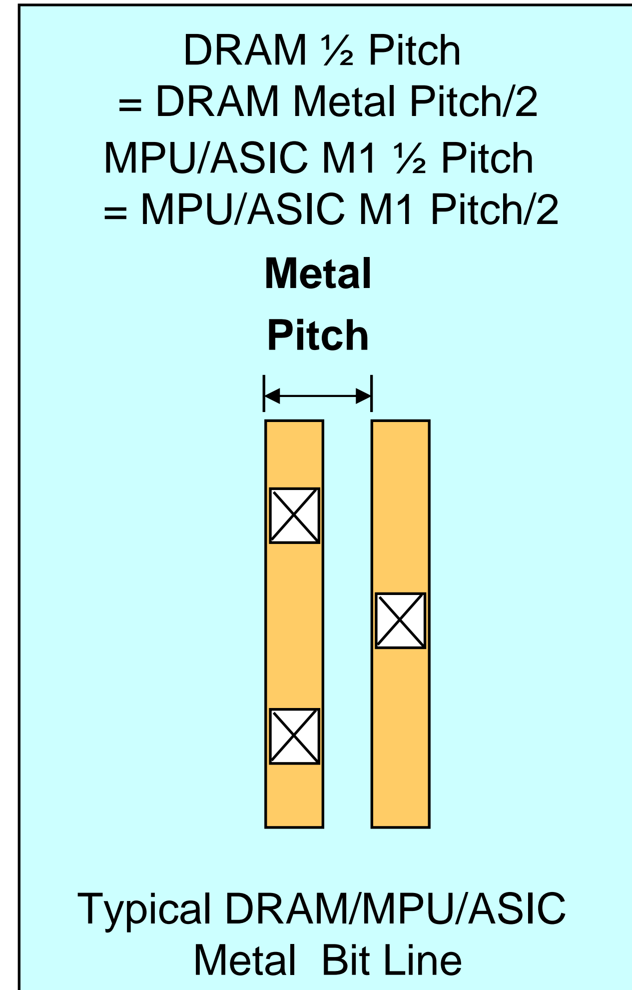
2009 Definition of the Half Pitch – unchanged

[No single-product "node" designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]





Source: 2009 ITRS - Exec. Summary Fig 1

2009 – Updated add ERD/ERM Research and PIDS Transfer

Production Ramp-up Model and Technology Cycle Timing

Development

Production

200K

20K

2K

200

20

2

Volume (Wafers/Month)

*Examples: 25Kwspm ~=
4.5Mu/mo @ 280mm2
10Mu/mo @ 140mm2
15Mu/mo @ 100mm2
22mu/mo @ 70mm2

Alpha Tool

Beta Tool

Production Tool

First Conf. Papers

First Two Companies Reaching Production

Additional Lead-time: ERD/ERM Research and PIDS Transfer

-24

-12

0

12

24

Months

Source: 2009 ITRS - Exec. Summary Fig 2a

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ERD/ERM Long-Range R&D and PIDS Transfer Timing Model Technology Cycle Timing

[Example: III-V MOSFET High-mobility Channel Replacement Materials]

New for 2009

Research | Development | Production

Transfer to PIDS/FEP (96-72mo Leadtime)

Alpha Tool | Beta Tool | Product Tool

First Tech. Conf. Device Papers Up to ~12yrs Prior to Product

First Tech. Conf. Circuits Papers Up to ~ 5yrs Prior to Product

1st 2 Co's Reach Product

Volume (Wafers/Month): 200K, 20K, 2K, 200, 20, 2

Months: -96, -72, -48, -24, 0, 24

III/V Hi-μ gate Example: 2011, 2013, 2015, 2017, 2019, 2021

Source: 2009 ITRS - Executive Summary Fig 2b

Work in Progress – Do Not Publish!

Including '11 snapshot Analysis

Figure 7a

2009 ITRS - Technology Trends

Memory

Nanometers (1e-9)

1000
100
10
1

1995
2000
2005
2010
2015
2020
2025

Year of Production

2009 ITRS Flash ½ Pitch (nm) (un-contacted Poly) - [2-yr cycle to 2010; then 3-yr cycle]

2009 ITRS DRAM ½ Pitch (nm) (contacted) [2.5yr cycle '00-'10, then 3-yr cycle]

2011
ORTC Targets
DRAM
40nm M1
Flash
28nm
Poly(uncont.)

16nm

Near-Term

Long-Term

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 7a

Work in Progress – Do Not Publish!

Including ’11 snapshot Analysis

Figure 7b

2009 ITRS - Technology Trends

Logic

1000
100
10
1

Nanometers (1e-9)

1995
2000
2005
2010
2015
2020
2025

Year of Production

2009 ITRS MPU/ASIC Metal 1 (M1) ½ Pitch (nm) [historical trailing at 2-yr cycle; extended to 2013; then 3-yr cycle]

2009 ITRS MPU Printed Gate Length (GLpr) (nm) [3-yr cycle from 2011/35.3nm]

2009 ITRS MPU Physical Gate Length (nm) [begin 3.8-yr cycle from 2009/29.0nm]

2011
ORTC Targets
“22nm”
(38nm M1)
GLpr 35nm
GLph 24nm

16nm

Near-Term

Long-Term

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 7b

Work in Progress – Do Not Publish!

Including survey input Analysis

Figure 8

Function Size

Memory & Logic

MPU/ASIC Alignment With Latest Design TWG Actual SRAM & Logic Gate Data

- 2009 DRAM Cell area per bit (1 bits/cell) (um2)
- 2009 Flash SLC area per bit (1 bits/cell) [SLC cell area/1] (um2)
- 2009 Flash MLC Ave area per bit (2 bits/cell) [SLC cell area/2] (um2)
- 2009 Flash MLC Ave area per bit (3 bits/cell) [SLC cell area/3] (um2)
- 2009 Flash MLC Ave area per bit (4 bits/cell) [SLC cell area/4] (um2)
- 2009 SRAM Cell (6-transistor) Area (um2)
- 2009 Logic Gate (4-transistor) Area (um2)

Square Micrometers (um2)

1.00E+04, 1.00E+03, 1.00E+02, 1.00E+01, 1.00E+00, 1.00E-01, 1.00E-02, 1.00E-03, 1.00E-04, 1.00E-05, 1.00E-06

DRAM $4f^2$ Added Beginning 2011

Flash
1) 2-yr Cycle Extended to 2010;
2) 3 bits/cell added 2009-2011;
3) 4 bits/cell moved To 2012

1995, 2000, 2005, 2010, 2015, 2020, 2025

Year of Production

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 8

Work in Progress – Do Not Publish!

Including ’11 snapshot Analysis

Figure 9a

Memory

2009 ITRS - Functions/chip and Chip Size

Gigabits (1e9) and Square Millimeters

10000.00
1000.00
100.00
10.00
1.00
0.10
0.01

1995
2000
2005
2010
2015
2020
2025

Year of Production

Flash SLC
1 Tera-bit!

2011:
DRAM 40nm; Flash/28nm
Model Bits/chip Generations

Flash
= 2x/2yrs

<143mm2
(22 x 6.5)

<60mm2
(11 x 5.5)

DRAM
= 2x/3yrs

Flash
"Hwang's
Law"
= 2x/1yr

DRAM
= 2x/2yrs

Average "Moore's
Law" = 2x/2yrs

- 2009 ITRS DRAM Functions per chip (Gbits)
- 2009 ITRS Flash (Gbits) SLC [2-year cycle]
- 2009 ITRS Functions per chip (Gbits) MLC (2 bits/cell)
- 2009 ITRS Functions per chip (Gbits) MLC (3 bits/cell) ADDED
- 2009 Functions per chip (Gbits) MLC (4 bits/cell)
- 2009 Flash Chip size at production (mm2)
- 2009 DRAM Chip size at production (mm2)

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 9a

Work in Progress – Do Not Publish!

Including ’11 snapshot Analysis

Figure 9b

Logic

2009 ITRS - Functions/chip and Chip Size

Million Transistors (1e6) and Square Millimeters

10000000
1000000
100000
10000
1000
100
10

2009 ITRS Cost-Performance MPU Functions per chip at production (Mtransistorst)

2009 ITRS High-Performance MPU Functions per chip at production (Mtransistors)

2009 Cost-Performance MPU Chip size at production (mm2)

2009 High-Performance MPU Chip size at production (mm2)

Average "Moore's Law" = 2x/2yrs

MPU = 2x/3yrs

MPU = 2x/2yrs

2011: “22nm”/(38nm M1) MPU Model Generations

<260mm2

<140mm2

1995 2000 2005 2010 2015 2020 2025

Year of Production

2009 ITRS: 2009-2024

Source: 2009 ITRS - Executive Summary Fig 9b

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Updated for 2009

Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution

W.P.C.=Total Worldwide Wafer Production Capacity* Sources SICAS

W.P.C. W.P.C. W.P.C. W.P.C. W.P.C. W.P.C. W.P.C. W.P.C. W.P.C. W.P.C. W.P.C.

Feature Size (Half Pitch) (μm)

10
1
0.1
0.01

Legend:
- >0.7μm
- 0.7-0.4μm
- 0.4-0.3μm
- 0.3- 0.2μm
- 0.2- 0.16μm
- 0.16-.12μm
- 0.08-.12μm
- <0.08μm

- = 2003/04 ITRS DRAM Contacted M1 Half-Pitch Actual
- = 2007/09 ITRS DRAM Contacted M1 Half-Pitch Target
- = 2009 ITRS Flash Uncontacted Poly Half Pitch Target
- = 2009 ITRS MPU/hpASIC Contacted M1 Half-Pitch Target

3-Year Cycle

2008/09 ITRS: 2.5-Year Ave Cycle for DRAM

2-Year DRAM Cycle

3-Year DRAM Cycle ; 2-year Cycle Flash and MPU

3-Year Cycle After 2010 for Flash; after 2013 For MPU

1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2013

Year

** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 2Q data for 2009. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

Source: 2009 ITRS - Executive Summary Fig 3

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2009 ITRS 450mm Update

[from Public ORTC San Francisco SEMICON, July, 2009]

ITRS IRC 2009 Position (Source 2009 Executive summary; 450mm Special Topic):

"….Intel, Samsung, and TSMC (IST) announced in May'08 that they will work together with suppliers, other semiconductor players and ISMI to develop 450mm with a goal of a pilot line in 2012. Full production may be 2-3 years after that[1]. This Public announcement and assessment may be subject to revision based on future statements; but it is the statement of record by these three companies and ISMI, as of the date of writing of the ITRS 2009 edition

The timing of the production ramp of 450 mm facilities (versus early pilot line capability) depends not only on the mastering of all technical issues, associated with this transition to a new diameter, but also on the preparedness of the industry. To assess the likelihood of that timing, the whole value chain must therefore be examined…"

"…Furthermore, and new in the 2009 ITRS, a 450mm Production Ramp-up Model Graphic has been provided (Figure 2c) to clarify the special dual "S-curve" timing required when a new wafer generation is being introduced [modeled after the experience with the 300mm wafer generation ramp on two succeeding technology cycles in the 2001-2003 (180nm-130nm M1) timeframe]…."

[1] Source: "May 2008"/ "Oct 2008 ISMI symposium"/Dec'08 ISMI 450mm Transition Program Status Update for ITRS IRC, Seoul, Korea [and also at SEMICON Japan]

2009 ITRS WORK IN PROGRESS – DO NOT PUBLISH

Work in Progress – Do Not Publish!

New for 2009

450mm Production Ramp-up Model

[2009 Figure 2c A Typical Wafer Generation Pilot Line and Production "Ramp" Curve]

Source: 2009 ITRS - Executive Summary Fig 2c

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