Front End Processes
2009 ITRS

ITRS Public Conference
December 16, 2009
Ambassador Hotel, Hsinchu, Taiwan

2009 Winter Meeting FEP ITWG Participants:
US: J. Butterbaugh, L. Larson, M. Walden, M. Goldstein
JP: I. Mizushima
EU: M. Alessandri

2009 FEP Sub-TWGs and Chairs

NEW STRUCTURE FOR FEP CHAPTER in 2009

DEVICE METRICS

- Logic Devices [HP, LOP, LSTP]: Prashant Majhi (US)
- DRAM Devices: Deoksin Kil (KR)
- Flash Devices: Mauro Alessandri (EU)
- PCM Devices: Mauro Alessandri (EU)
- FeRAM Devices: Yoshimasa Horii (JP)

PROCESS METRICS

- Starting Materials: Mike Walden (US), Mike Goldstein (US)
- Surface Preparation: Joel Barnett (US)
- Thermal/Thin Films/Doping: Prashant Majhi (US)
- Etch: Tom Lii (US)
- CMP: Darryl Peters (US)

FEP 2009 Participants

Danel Adrien, Mauro Alessandri, Luis Aparicio, Sehgal Aksey, Amulya Athayde, Souvik Banerjee, Joel Barnett, Twan Bearda, Meridith Beebe, Steve Benner, Ivan (Skip) Berry, Chris Borst, William Bowers, Ian Brown, Arifin Budihardio, Murray Bullis, Mayank T. Bulsara, Jeff Butterbaugh, George K. Celler, Cetin Cetinkaya, Luke Chang, Victor Chia, Phil Clark, Lee Cook, Jeffrey Cross, Suman Datta, Carlos H. Diaz, Roxanne Dulas, Paul Feeney, Graham Fisher, Nich Fuller, Mike Fury, Glenn Gale, Yehiel Gotkis, Mike Goldstein, Christina Gottschalk, Aomar Halimaoui, Qingyuan Han, Dick Hockett, Andrew Hoff, Yoshimasa Horii, Greg Hughes, William Hughes, Raj Jammy, Ravi Kanjolia, Bruce Kellerman, Deoksin Kil, Hyungsup Kim, Simon Kirk, Brian Kirkpatrick, Hiroshi Kitajima, Martin Knotter, Daniel Koos, Larry Larson, Jeff Lauerhaas, Yannick Le Tiec, Kun Tack Lee, Jooh Yun Lee, Tom Lii, Hong Lin, Prashant Majhi, Tom McKenna, Paul Mertens, Katsuhiko Miki, Ichiro Mizushima, Mansour Monipour, Paul Morgan, Brian Murphy, Anthony Muscat, Sadao Nakajima, Yasuo Nara, Masaaki Niwa, Toshihide Ohgata, Hiroshi Oji, Jin Goo Park, Friedrich Passek, Eric Persson, Darryl Peters, Gerd Pfeiffer, Jagdish Prasad, Rick Reidy, Karen Reinhardt, Hwa sung Rhee, Rob Rhoades, Marcello Riva, Jae Sung Roh, Akira Sakai, Archita Sengupta, YugYun Shin, James Shen, Wolfgang Sievert, Chris Sparks, Robert Standley, Sing Pin Tay, Bob Turkot, Steven Verhaverbeke, Hitoshi Wakabayashi, Mike Walden, Masaharu Watanabe, Han Xu

HP Logic Devices

- **New Table Structure**
  - Individual tables to focus on device metrics for HP, LOP, and LSTP
- **New scaling approach coordinated with PIDS**
  - reset CV/I benchmark in 2009 to 0.82 ps
  - CV/I improvement factor changed to 13% per year
- **New Model Assumptions and New Rows; Parasitic Resistance Constraint**
- **$I_{d, sat}$ not matched to PIDS table → Plan to resolve in 2010**

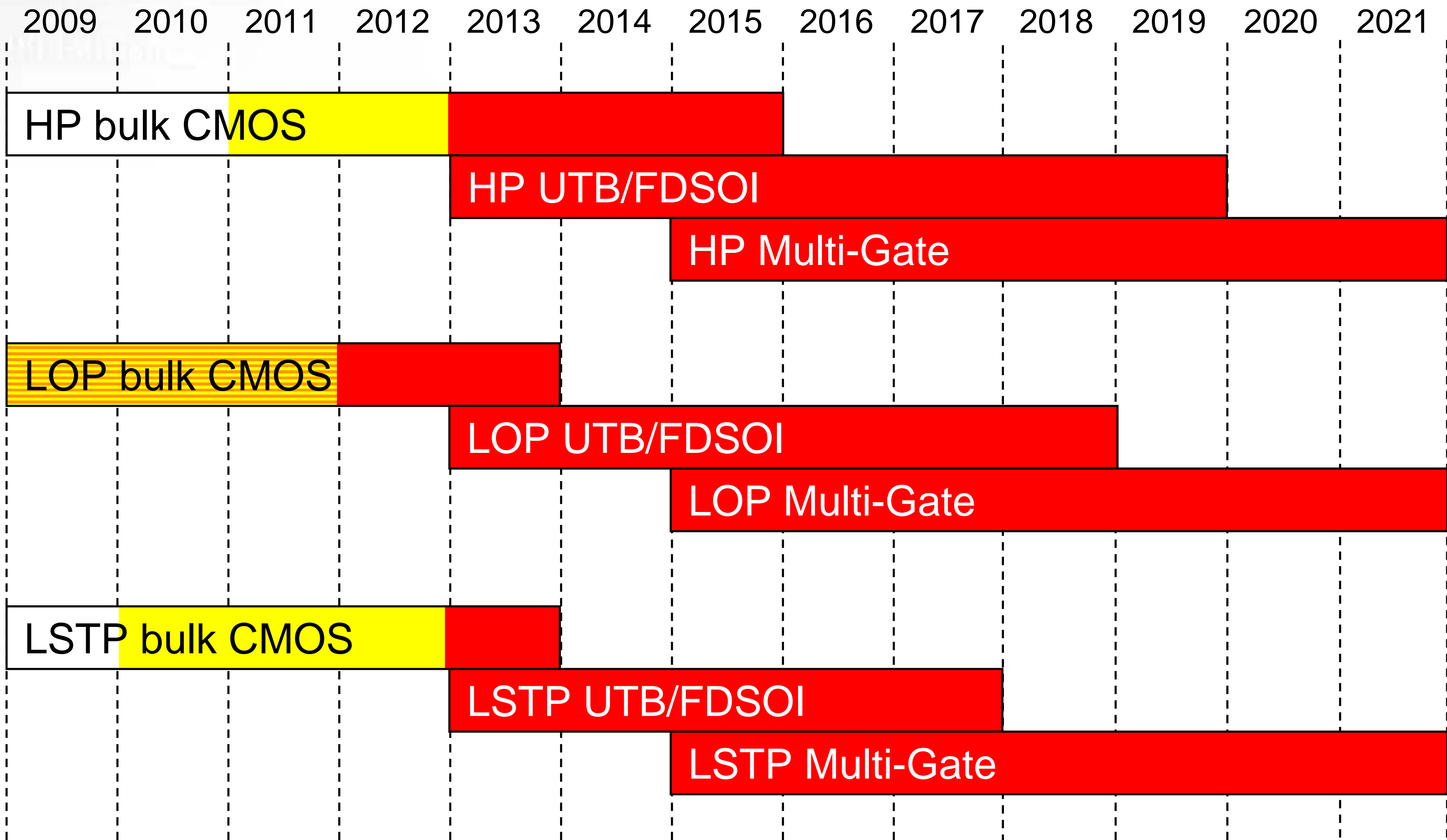
Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU Printed Gate Length (nm)	47	41	35	31	28	25	22
MPU Physical Gate Length (nm)	29	27	24	22	20	18	17
Supply voltage of operation (voltage scaling to ensure total active power consumption not to exceed heat removal rate)	**1**	**0.97**	**0.93**	**0.9**	**0.87**	**0.84**	**0.81**
Threshold voltage under linear drain bias conidition (V)	**0.33**	**0.3201**	**0.3069**	**0.297**	**0.2871**	**0.2772**	**0.2673**
Saturation drive current (mA/um)	**1.68**	**1.80**	**1.80**	**2.20**	**2.4**	**2.7**	**3.0**
Off-state current under high drain bias (nA/um)at room temperature	**100**	**100**	**100**	**100**	**100**	**100**	**100**

LSTP Logic Devices

- **New scaling approach coordinated with PIDS**
  - reset CV/I benchmark in 2009 [CV/I improvement factor changed to 13% per year]
  - include Poly/SiON gate stacks through 2010, possibly extended to 2013

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU Printed Gate Length (nm)	47	41	35	31	28	25	22
Physical gate length low standby power (LSTP) (nm)	38	32	29	27	22	18	17
EOT for bulk LSTP (nm) for 1.5E20-doped poly-Si	**1.2**	**1**	♦ 0.9	♦ 0.8	♦ 0.7		
EOT for bulk LSTP (nm) for metal gate		**1.3**	**1.2**	**1**	**0.9**		
EOT for FDSOI LSTP (nm) for metal gate					**1**	**0.95**	**0.9**
EOT for multi-gate LSTP (nm) for metal gate							**1.1**
Supply voltage of operation	**1.05**	**1.05**	**1.05**	**1**	**0.95**	**0.95**	**0.95**
Threshold voltage under linear drain bias conidition (V)	**0.33**	**0.3201**	**0.3069**	**0.297**	**0.2871**	**0.2772**	**0.2673**
Saturation drive current (mA/um)	**0.54**	**0.56**	**0.58**	**0.66**	**0.81**	**0.93**	**1.02**
Off-state current under high drain bias (nA/um) at R.T.	**0.10**	**0.10**	**0.10**	**0.10**	**0.10**	**0.10**	**0.10**

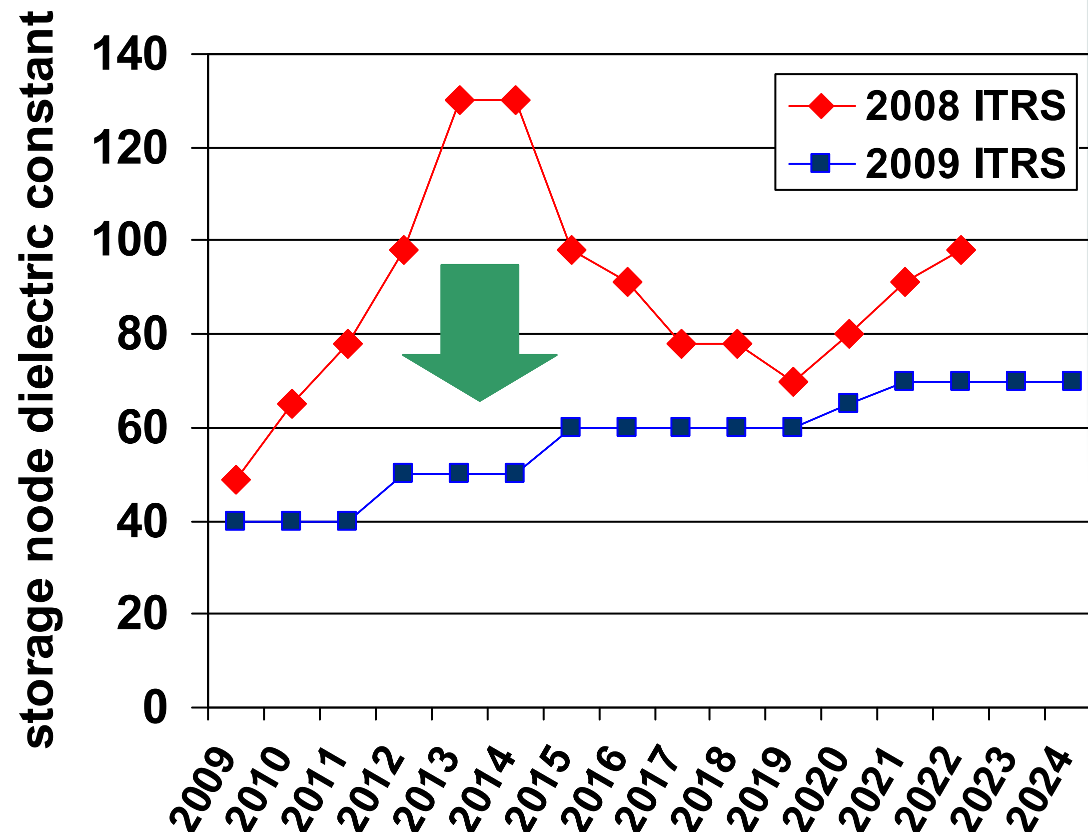
Timing of CMOS Innovations



DRAM

- ORTC/PIDS a factor drops from 6 to 4 in 2011 → this was not captured in 2009 FEP DRAM Table and will be corrected in 2010 update
- capacitance per cell reduced from 25 to 20 pF in 2012 due to expected introduction of buried word line
- capacitor dielectric constant reduced and no longer peaks at 130

- capacitor dielectric constant physical thickness reduced → no longer red
- A/R yellow in 2011 and red in 2013



Potential Dielectric Thickness Problem

Permittivity

400, 360, 320, 280, 240, 200, 160, 120, 80, 40, 0

0, 20, 40, 60, 80, 100, 120, 140, 160, 180, 200

Film thickness (Å)

Tox=0.5nm

Tox < 0.5nm

Tox > 0.5nm

BST, BST, BST, BST, STO, STO, Ta_2O_5, TaNbOx, ZrO_2, ZrO_2, Al_TiO_2

- Ru/STO(160)/Ru, SNU, 2006
- TaNbOx/Nb_2O_5(60)/Ru : Samsung, 2005, JVST
- Pt/Ta2O5(150)/Ru : Fujitsu, 1999, APL
- Pt/[1.67%Al-TiO2(80)]/Ru : SNU, 2005
- TiN/ZrO2(70)/TiN : Samsung, 2005, SSDM
- Pt/BST/Pt : SNU, 1999, TFS
- TiN/ZrO2(112)/TiN, Hynix, 2006
- Pt/BST/Pt : Samsung, 1997, APL
- Pt/STO(150)/SrO(25)/Ru : KAIST, 2006

2009 ITRS DRAM Roadmap

Physical thickness increases as the permittivity increases maintaining a certain leakage current → enough room?

Flash

- **Floating Gate Flash: need for transition to high-k interpoly dielectric moved to 25 nm for NAND and other minor adjustments**
- **New Table added for planar Charge-Trapping Flash that includes:**
  1. **Tunnel dielectric:** EOT thickness, Material/structure to be used, Max leakage current (for retention purpose) measured @ highest write/erase voltage, Erase/program time degradation at constant voltage
  2. **Charge Trapping layer:** Minimum trap density, Trap energy level, Minimum band offset vs conduction band of the tunnel dielectric and the blocking dielectric (eV), Dielectric constant, Material/structure to be used
  3. **Blocking Dielectric:** EOT thickness, Max leakage current (for retention purpose) measured @ highest write/erase voltage, Material/structure to be used
  4. **Gate:** Working function, Material/structure to be used

PCRAM

- **Added conformality of the PCM cell sealing dielectric.**
- **The challenge in this case is to achieve conformality within a very low thermal budget compatible with the phase change material**

Grey cells indicate the requirements projected for years before it reaches volume production.

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*
PCM ½ Pitch (nm) (contacted)	50	45	40	35	32
Phase change material min. conformality (%) [A]	70	90	90	90	98
PCRAM phase change material minimum operating temperature (°C) [B]	100	100	100	100	125
Heater max resistivity change during reset cycle and after 1E12 cycles (%)	5	5	5	5	5
Maximum Reset Current Density (A/ μm^2)	0.3-0.8	0.4-1.0	0.4-1.0	0.4-1.0	0.5-1.3
Cell Sealing Dielectric min. conformality (%)[E]	90	95	95	95	98

FeRAM

- **Table parameters, general trend are unchanged**
- **Trends in 4-year blocks**

Year of Production	*2009-2012*	*2013-2016*	*2017-2020*	*2021-2024*
FeRAM technology – F (nm) [A]	180	130	90	65
FeRAM cell size – area factor a				
in multiples of F2 [B]	22	16	14	12
FeRAM cell size (μm²) [C]	0.713	0.27	0.113	0.051
FeRAM cell structure [D]	1T1C	1T1C	1T1C	1T1C
FeRAM capacitor structure [E]	stack	stack	3D	3D
FeRAM capacitor footprint (μm²) [F]	0.33	0.106	0.041	0.016
FeRAM capacitor active area (μm²) [G]	0.33	0.106	0.1	0.069
FeRAM cap active area/footprint ratio	1	1	2.46	4.25
Ferro capacitor voltage (V) [I]	1.5	1.2	1	0.7
FeRAM minimum switching charge density (μC/cm²) [J]	13.5	34	30	30
FeRAM endurance (read/write cycles) [K]	1.00E+14	1.00E+15	>1.0E16	>1.0E16
FeRAM nonvolatile data retention (years) [L]	10 Years	10 Years	10 Years	10 Years

FeRAM
- forward to high density memory -

High-Density and High Speed 128Mb Chain FeRAM with SDRAM- Compatible DDR Interface
Shimojo et al. (Toshiba, VLSI technology symposium 2009)

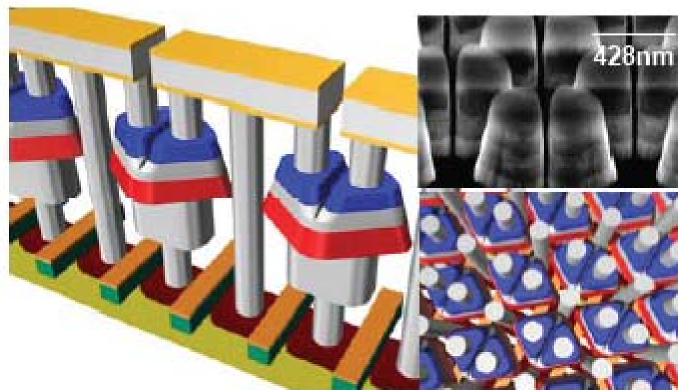


Fig. 1. A 3D image and a bird's-eye view of 128Mb Chain FeRAM™.

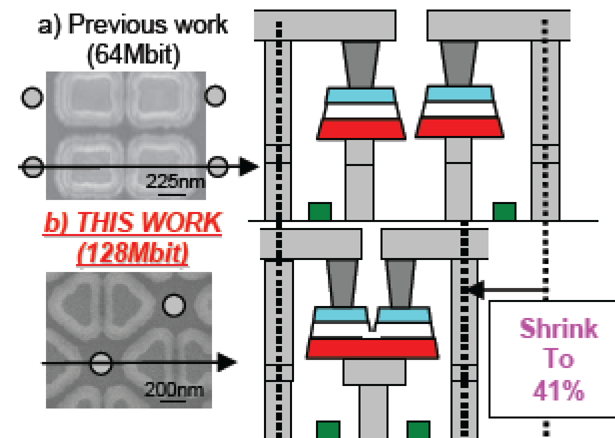


Fig. 3. Schematic view of 128Mb FeRAM in comparison with previous 64Mb FeRAM.

High-density cover film and low-damage ferroelectric capacitor etching technique realize 128Mb FeRAM.

Starting Materials

- Alignment of 450mm substrate timing with ISMI projections
- New ORTC and related chip size / gate length models have been utilized
- Pull-in of 45nm particle size from 2012 to 2010
- Defect densities no longer allowed to increase from the previous generations' values based upon industry realities
- Near-term improvement in SOI BOX and layer thickness capabilities noted – Partially depleted SOI removed from table beginning with 15nm MPU technology generation
- Colorization updated

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	52	45	40	36	32	28	25
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	54	45	38	32	27	24	21
Front surface particle size (nm), latex sphere equivalent (A)	≥65	≥45	≥45	≥45	≥32	≥32	≥32
Particles (cm^{-2})***	≤ 0.18	≤ 0.18	≤ 0.18	≤ 0.18	≤ 0.18	≤ 0.18	≤ 0.18
Particles (#/wf)****	≤ 126	≤ 126	≤ 126	≤ 126	≤ 126	≤ 286	≤ 286
Silicon-On-Insulator (SOI) Wafer* (99% Chip Yield)							
Edge exclusion (mm)*****	2	2	2	2	2	2	2
Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (nm) (D)	54-83	50-76	46-71	43–65	40–60	38–56	35–52
Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3σ) (nm) (E)		17-32	16-21	16–20	15–19	14–17	14–16
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3σ) (nm) (F)		40-66	36-60	34–56	30–50	28–46	26–42

Surface Preparation

- Particle metrics updated for changes in DRAM models
- Current particle metrology is a challenge at "Critical Particle Diameter"
- Material loss metrics colorization removed for DRAM
- Achieving material loss goals for advanced logic remains a challenge

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*52*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*54*	*45*	*38*	*32*	*27*
MPU Physical Gate Length (nm)	*29*	*27*	*24*	*22*	*20*
Front surface particles					
Killer defect density, D_pR_p (#/cm^2) [A]	0.033	0.043	0.033	0.042	0.053
Critical particle diameter, d_c (nm) [B]	◆ 25.8	◆ 22.5	◆ 20.0	◆ 17.9	◆ 15.9
Critical particle count, D_{pw} (#/wafer) [C]	◆ 113.3	◆ 113.3	◆ 113.3	◆ 327.2	◆ 327.2
Silicon and oxide loss (Å) on polysilicon blanket test wafers per LDD clean step—DRAM [K]	1.2	0.9	0.9	0.9	0.6
Silicon and oxide loss (Å) on polysilicon blanket test wafers per LDD clean step—Microprocessor/SoC/Analog [L]	0.4	◆ 0.3	◆ 0.3	◆0.3	◆0.2

ITRS

Thermal/Thin Films/Doping

- **Emphasis on Scaled Junctions (to allow for Lg scaling) and External Resistance (scaled contact Rco)**

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU Printed Gate Length (nm)	47	41	35	31	28	25	22
MPU Physical Gate Length (nm)	29	27	24	22	20	18	17
Drain extension X_j (nm) for bulk MPU/ASIC [A]	**13**	**12**	**10.5**	**9.5**	**8.7**	**8**	**7.3**
Maximum allowable parasitic series resistance for bulk NMOS MPU/ASIC × width ((Ω–μm) from PIDS [B]	**170**	**170**	**160**	**140**	**130**	**110**	**110**
Maximum drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/sq) [B]	**650**	**670**	**660**	**680**	**750**	**810**	**900**
Contact maximum resistivity for bulk MPU/ASIC (Ω-cm²) [I]	**1.60E-07**	**1.38E-07**	**8.00E-08**	**4.00E-08**	**2.00E-08**	**1.00E-08**	**8.00E-09**

Etch

- **New Methodology to address gate length variation**
  - contributions from lithography and etch cannot be treated separately
  - advanced process control allows lithography tools to make field-to-field adjustments to account for both lithography and etch variations across the wafer
  - Etch inputs coordinated between FEP and LITHO
  - Physical gate length variation include several random variations listed in table below

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*
MPU Printed Gate Length (nm)	47	41	35	31	28	25
MPU Physical Gate Length (nm)	29	27	24	22	20	18
L_{gate} 3 σ variation (nm) [D]	3.48	3.18	2.9	2.65	2.42	2.21
Lgate line width roughness 3 σ (nm) [E]	2.5	2.28	2.08	1.9	1.74	1.59
Across chip Lgate variation 3 σ (nm) [F]	1.5	1.37	1.25	1.14	1.04	0.95
Across wafer Lgate variation 3 σ (nm) [G]	1.4	1.29	1.18	1.08	0.98	0.9
Wafer to wafer within lot Lgate 3 σ (nm)	0.9	0.82	0.75	0.69	0.63	0.58
Lot to lot Lgate 3 σ (nm)	0.9	0.82	0.75	0.69	0.63	0.58
Through pitch Lgate variation 3 σ (nm) [H]	1.52	1.4	1.3	1.16	1.06	0.97

CMP

- Shallow Trench Isolation CMP requirements table New in 2009
  - CMP inputs coordinated between FEP and Interconnect TWGs
  - Scaled from 130nm Equipment Performance Metrics (EPM)
  - Real data from end users is difficult to obtain
  - Broadly applicable, accurate models are not available
  - Scaled EPMs will be used for baseline CMP metrics going forward, to be refined by data when available
- Defectivity, especially microscratches, are a challenge
  - Significant yield impact and reliability issue
- Improvements needed in WIW and WTW uniformity
- Post-CMP cleans are not addressed in ITRS
  - Cleans can have an impact on metal gate work function

FEP Difficult Challenges
≥ 16 nm (Metal 1 1/2-pitch)

- Strain Engineering
  - continued improvement for increasing device performance
  - application to FDSOI and Multi-gate technologies
- Achieving DRAM cell capacitance with dimensional scaling
  - finding robust dielectric with dielectric constant of ~60
  - finding electrode material with high work function
- Achieving clean surfaces free of killer defects
  - with no pattern damage
  - with low material loss (<0.2 A)
- High-k/Metal Gate
  - introduction to full scale manufacturing for HP, LOP, and LSTP
  - scaling equivalent oxide thickness (EOT) below 0.8nm
- 450mm wafers - meeting production level quality and quantity

FEP Difficult Challenges
< 16 nm (Metal 1 1/2-pitch)

- Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation.
- Lowering required DRAM capacitance by $4F^2$ cell scheme or like, while continuing to address materials challenges
- Continued achievement of clean surfaces while eliminating material loss and surface damage and sub-critical dimension particle defects
- Continued EOT scaling below 0.7 nm with appropriate metal gates
- Continued charge retention with dimensional scaling and introduction of new non-charged based NVM technologies

2009 FEP - Highlights

- **Logic Devices:**
  - Separate tables for HP, LOP, LSTP; CV/I reset with 13% pace; HP I_{off} set at 100nA/um
  - Incorporated new Lg pacing
- **DRAM Devices:**
  - Node capacitance adjusted for buried wordline; Capacitor dielectric requirement eased/smoothed
- **Non-volatile memories**
  - Flash – New Charge Trapping Flash Table added
  - PCRAM – Conformality of Sealing Dielectric added
  - FeRAM – minor changes; pacing captured in 4-year blocks
- **Starting Materials:**
  - Incorporated new ORTC scaling and recalculated allowable defects
  - Near-term improvement in SOI BOX and layer thickness capabilities noted (color changed)
- **Surface Preparation:**
  - Incorporated new ORTC scaling and recalculated allowable defects
  - Metrology not capable of monitoring killer defect size
- **Thermal/Thin Films/Doping:**
  - New table which is split from previous logic device tables
  - Emphasis on Scaled Junctions and External Resistance
- **Etch:**
  - New methodology for tracking gate length variation requirements accounting for currently used Advanced Process Control capabilities in lithography.
- **CMP:**
  - New table for 2009; scratches and uniformity requirements are projected