International Technology Roadmap for Semiconductors

Assembly and Packaging
2009

Assembly and Packaging Technical Working Group Participants and Collaborators for 2009

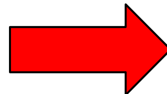
86 Members

- ✓ ***Representation from:***
  - ➢ ***Europe***
  - ➢ ***Japan***
  - ➢ ***Korea***
  - ➢ ***Taiwan***
  - ➢ ***United States***
  - ➢ ***Hong Kong***

- ✓ ***Meeting in Beijing for input from China***
- ✓ ***Active Collaboration with iNEMI and JISSO Roadmaps***
- ✓ ***Joint Project with MIT Microphotonics Center***

Major Activities 2009
Revision made to single chip package categories

Previous Categories
Low-cost/hand held
Cost performance
High performance
Harsh



New Categories
Low-end, Low-cost
Mobile/Handheld
Memory
Cost performance
High performance
Harsh

Major Activities 2009

Expanded coverage of :

- Wafer Level Packaging
- Wafer thinning, singulation and b onding for 3D integration
- Optoelectronics
- Through silicon vias

Added coverage of:

- *Photovoltaics*
- *LEDs*
- *Power devices*

ITRS

Cross TWG Activity

- ERM-new materials
- Design-3D co-design
- Wireless-MEMS
- Test-probably good die
- ESH- information on regulatory concerns
- Yield- yield analysis and optimization tools for packaging (WLP first)
- Interconnect (3D Integration)

Automotive Packaging

Metric	Specification
Automotive Maximum Temperatures (Ambient Temperatures)	
Passenger Compartment Dashboard, panel Hatrack	 +85°C +120°C
Chassis	

The rapid growth in hybrid and electric vehicles brings an additional class of electronics and a new subset of environmental conditions that are addressed in the 2009 Roadmap.

Metric	Specification
Storage Range	-55°C to 125 °C
Operating Range	-40°C to 150°C
Typical Mission Profile	-40 to - 20°C / 300h -20 to + 20°C / 600h 20 to +130°C / 4000h 130 to +140°C / 1000h +150°C / 100h
Vibration	40g / 10–1000Hz (depending on customer)
Mechanical Shock	50g / 11ms (depending on customer)

Major Activities 2009

Major revisions to tables for:

- *Optoelectronics*
- *System in Package*
- *Wafer thinning*
- *Wafer level Packaging*
- *Wafer Stacking/3D integration*

ITRS

Major Activities 2009

New tables for:

- Photovoltaics
- Power devices
- Packaging gaps and needs
- Optical Transceivers
- Packaging Consortia

ITRS

New Materials will be required

Working with ERM the Needs have been identified

Many are in use today

- Cu interconnect
- Ultra Low k dielectrics
- High k dielectrics
- Organic semiconductors
- Green Materials
  - Pb free
  - Halogen free

But improvements are neede d

Many are in development

- *Nanotubes*
- *Nano Wires*
- *Macromolecules*
- *Nano Particles*
- *Composite materials*

Functional Diversification and "More than Moore" are driving rapid change in Packaging Technology

Everything is changing:

- Architectures
- Materials
- processes
- equipment

ITRS

ITRS Assembly and Packaging TWG and MIT's Microphotonics Center are Collaborating on 3D Implementation of a Computing SiP

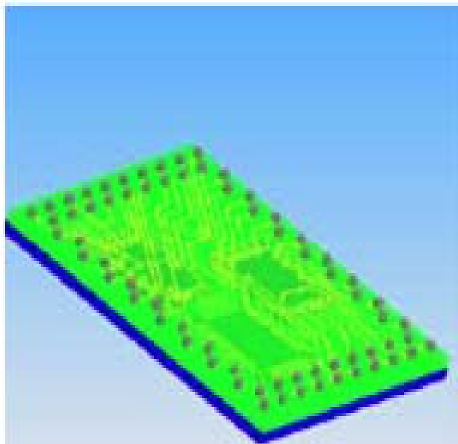
This project is intended to identify the difficult challenges and potential solutions for Complex 3D integration with SiP

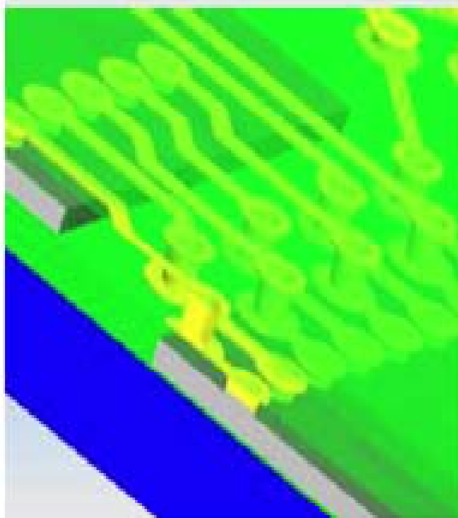
The Target is Tera-scale computing by 2015

- Implementation of a 3D Integrated Computing SiP targeting Capability in 2015
  - This Project illustrates the technical challenges for packaging posed by technology nodes below 45nm

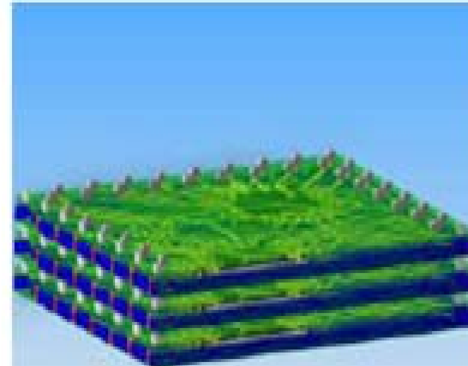
ITRS

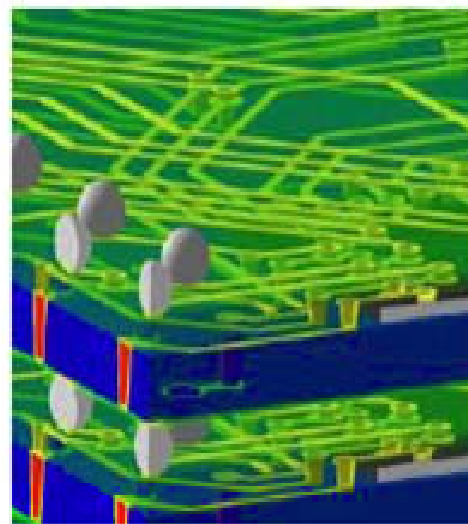
The Design Parameters





Target date for production:	2015
Number of Cores:	1000
Core transistor speed:	1GHz
Electrical pins off-chip max:	25GHz
Optical connections/ Package:	1
Optical bandwidth	1Tbyte/S
Power, ground and clock connections through substrate	#TBD
Total power per package:	TBD
Die size:	
Memory	$557mm^2$
Logic	$310mm^2$
Optical	TBD
Die thickness	
CPU:	25um
Memory:	25um
Total power per package:	TBD
Maximum power density:	TBD
Hot spot distribution:	TBD
Max. Junction temperature:	~85°C
Operating Voltage:	400mV

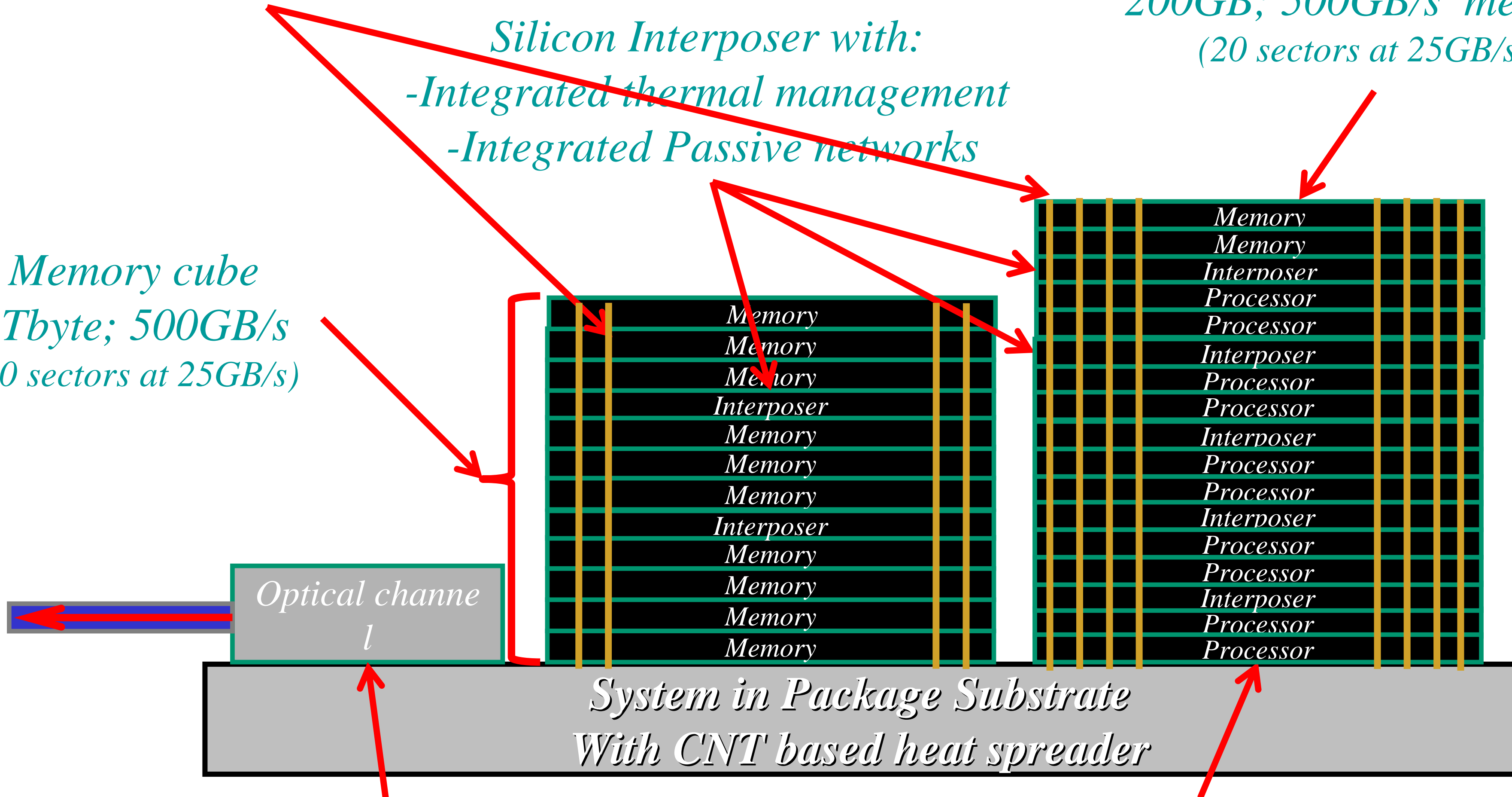




Tera-scale Computing by 2015

TSV die to die connection

200GB; 500GB/s memory
(20 sectors at 25GB/s)



1TB/s optical transceiver for:
- Off package communication
- On package routing

Processor with 1000 cores/10 layers
Core transistor speed 1GHz
25um thick wafer (~400mV power)

ITRS

Tera-scale Computing by 2015

Collaboration underway to identify challenges and define solutions

ITRS Technical working subgroups are addressing:

- TSV technology
- Thermal management
- Die to die bonding
- Power integrity
- SiP integration
- Optical signaling
- Package substrate requirements

ITRS

Significant Gaps Remain

Packaging Technology is experiencing a wave of innovation but significant gaps and unresolved technology needs remain which are summarized in the following slides

Packaging/Gaps/Technology Needs Summary

Priority	< 5 Years (Tactical) Gaps/Needs	Category	Comments:
H	Industry ownership for creating a roadmap that covers the emergence of "more than Moore" type of packaging integration technologies (System in Package, MEMS, sensors, analog centric technologies, opto electronics, heterogeneous integration including all of the above, etc.)		ITRS has been driven by primarily by CMOS logic and memory circuits. We are seeing the emergence of System in Package, MEMS, sensors, analog centric technologies, heterogeneous integration, etc. which are
H	Through Silicon Vias development and productizatio needs acceleration. Key is high throughput processes and equipment, hi reliability data, design rules ava		
H	Molding Compounds with better prope cost.		te
H	SiP components and systems reliab drive the need for tools and proce available. Test access will be a li and new approaches will be ne		on nd
H	Better understanding of interf science of adhes delamination of packaging materials and interfaces in use today is needed. This area is one of the key areas that will impact future yield and reliability.		ith low

Better understanding of interfacial science of adhesion / delamination of packaging materials and interfaces i n use today is needed. This area is o ne of the key areas that will impact future yield and reliability.

acceleration.

ey issues:

- high throughput processes and equipment
- high integrated yield
- reliability data
- design rules availability and cos t

Packaging/Gaps/Technology Needs Summary Continued

Priority	< 5 Years (Tactical) Gaps/Needs	Category	Comments:
H	There is no clear consensus regarding the preferred flip chip interconnect method for FCCSP/FCPOP products in 28nm node and beyond. Standardization to drive the required economies of scale and industry infrastructure development are needed.	S/O	The use of solder plated bumps, Cu pillar, Au stud, area array and/or perimeter bump patterns, lines and spaces, via pitch design rules, etc. are addressed in the ITRS. Optimization and standards are required to meet the cost/performance targets.
H	Flip chip packaging with tighter pitch, lower processing temperature and reduced cost are needed to complement the performance and other advantages of flip chip technology for packaging.	R/O	Low cost and high reliability for large, thin die flip chip will require additional research and optimization.
H	There is a need to increase R&D investment to accelerate progress in under fill technology. New disruptive technology / out of the ... as the pitch shrinks and ...		New materials will be required. Potential solutions include pre-applied ...
H	Need lower cost silicon interpose... passive devices		
H	Package warpage at elev... reflow simulation) will drive th... and potentially new packaging structures.		
M	Need for optimized, lower cost of ownership and high throughput equipment for wafer scale packaging and System in Package		
M	The packaging of thinned die will require new, cost effective equipment and processes.	R/O	This issue becomes more critical as wafer diameter increases and die thickness decreases, issues include stress relief, surface thickness variation, wafer warpage, handling after thinning, singulation, packing/shipment methods from wafer fabs to packaging houses.
M	New equipment capability to support assembly of SiP with variety of components including ICs, passives, optical devices, MEMS, biochips on the same substrate	R/O	Greater flexibility, versatility and precision will be required, as well as the ability to handle new processes and materials.
M	Need new high thermal conductive materials chemistry for high thermal density devices	R/O	The new materials properties required have been included in the Emerging Research Materials Chapter.

There is a need to increase R&D investment to accelerate progress in under fill technology. New disruptive technology / out of the box thinking is required as the pitc h shrinks and die size increased.

Packaging/Gaps/Technology Needs Summary

Priority	> 5 Years (Strategic) Gaps/Needs	Category	Comments:
H	Clear identification of packaging technologies needed to help close the gap required to continue scaling until new device technologies being researched to rep are available.	D/M/S	Packaging technology will partially close the gap while research institutions complete the R&D for new device technologies, in order to
H	There is a need to increase R&D in packaging technology and to incr of that investment to meet the ITRS.		
H	Package substrates component in ad improving but There is a need for innovations and potentia disruptive technologies to help to reverse This is the primary cost limiting factor		
H	Medical electronics packaging processes, that are bio-c and compatible with MRI systems		and reach greater levels of miniaturization are needed.

Package substrates remains the most expensive component in advanced packages. The trend is not improving. There is a need for innovations and potentially for new disruptive technologies to help to reverse this trend. This is the primary cost limiting factor for packaging.

that are bio-compatible, RoHS compliant and compatible with MRI systems.

Category for > 5 year (Strategic) Gaps
Design = D
Energy & Environment = E
Manufacturing = Mfg
Materials = M; System Integration = S

Packaging/Gaps/Technology Needs Summary Continued

Priority	> 5 Years (Strategic) Gaps/Needs	Category	Comments:
H	Improved design systems providing ele... and mechanical co-design and simu... be used as predictors of packa... high level of confidence will ... the packaging requireme... added to the agenda...		
M	Future gener... incorpora... prop... w... d... Eme... address... and new sa... new materials.		

Future generation of packaging technology will incorporate a wide range of new materials with properties not availabe today. These will include materials with both higher and lower dielectric constants, improved electrical and thermal conductivity. The desired materials properties have been delivered to the Emerging Research Materials TWG. Will need to address the issues of new processes, new equipment and new safety issues required to incorporate these new materials.

Category for > 5 year (Strategic) Gaps
Design = D
Energy & Environment = E
Manufacturing = Mfg
Materials = M; System Integration = S

Thank You