Modeling and Simulation ITWG

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2009 Modeling & Simulation SCOPE & SCALES

Modeling Overall Goal

- Support technology development and optimization
- Reduce development times and costs

Equipment related
- Equipment/Feature scale Modeling
- Lithography Modeling

IC-scale
- Circuit Elements Modeling
- Package Simulation

- Numerical Methods
- Materials Modeling
- **NEW: Reliability Modeling**
- Renamed: Modeling for Design Robustness, Manufacturing and Yield

Feature scale
- Front End Process Modeling
- Device Modeling
- Interconnects and Integrated Passives Modeling

Key Messages

- Mission of Modeling and Simulation as cross-cut topic:
  Support areas covered by other ITWGs
  ⇒ Continued in-depth analysis of M&S needs of other ITWGs, based on documents + inter-ITWG discussions – holds also for 2009
  ⇒ Strong links with ALL ITWGs – see also crosscut texts in 2007/9 ITRS
- Modeling and simulation provides an 'embodiment of knowledge and understanding'. It is a tool for technology/device development and optimization and also for training/education
- Technology modeling and simulation is one of a few methods that can reduce development times and costs:
  - 2008 major action on assessment of industrial use of TCAD and reduction of development times and costs in best-practice cases

Basic Approach and Focus of 2009 Work

1) Detailed cross-cuts worked out since 2003 – regularly updated together with other ITWGs – continued in 2009 as input to tables and text editing

2) Detailed revision of M&S tables based on state-of-the-art & cross-cut requirements

3) (11) M&S subchapters being prepared by multi-regional editing teams

4) Major action on assessment of use of TCAD in companies:
   - 2008 action: WWW questionnaire worked out and distributed to industrial TCAD users (NOT to developers!) - about 140 replies received
   - Results has been used for update of cost reduction estimate & as input to 2009 work

Development Time and Cost Reduction Estimate

Answers on question for average reduction of development time and costs in success case of simulation which occurred in environment of TCAD users:

ORTC INDEX	*Table MS3 Modeling and Simulation Technology Requirements: Accuracy* [1] ~~and Speed~~ *—Near-term Years*									
ITWG INDEX	*Year of Production*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
	DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
	MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
DELETED	~~Technology development costs reduction potential if TCAD is appropriately used [2]~~	~~40%~~	~~40%~~	~~40%~~	~~40%~~	~~40%~~	~~40%~~	~~40%~~	~~40%~~	~~40%~~
ADD	Estimated technology development cost reduction from use o TCAD (average across best-practice cases reported by industry) [2]	27%	27%	30%	32%	35%	37%	n.a.	n.a.	n.a.
ADD	Estimated technology development time reduction from use o TCAD (average across best-practice cases reported by industry) [2]	30%	30%	32%	34%	37%	39%	n.a.	n.a.	n.a.
	Lithography Modeling									
WAS	Absolute CD prediction accuracy (incl. OP effects) for dense and isolated lines – % of actual CD (=printed gate length) [3]	3%	3%	3%	3%	3%	3%	3%	3%	3%

Definition different from estimate of preceding years which referred to cost reduction potential and was based on earlier survey

Main Changes in 2009 Challenges

Titles of the challenges unchanged – except for ~~"Ultimate~~ Nanoscale Device Simulation Capability: Methods, models and algorithms that contribute to prediction of CMOS limits

Short-term challenges:

- 1 to 3 new items for each of the short-term challenges
- For 3 short-term challenges, one item each removed
- Several items slightly modified

Long-term challenges:

- One some items slightly changed in two long-term challenges

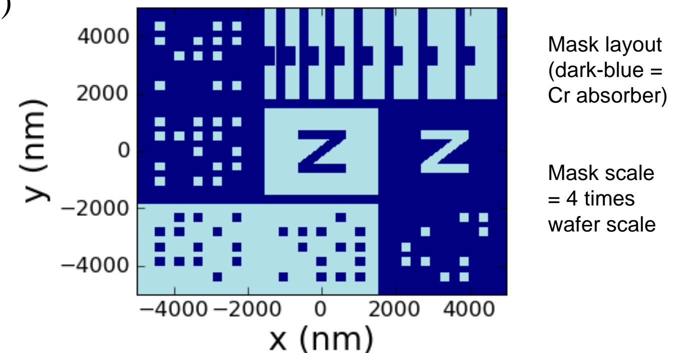
2009 Short-Term Difficult Challenges- changes compared to 2008 in blue/red

Lithography Simulation including EUV

Needs

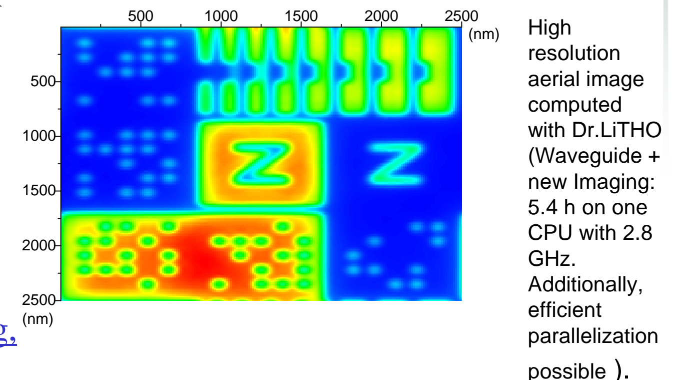
- ~~Experimental verification and simulation of ultra-high NA vector models, including polarization effects from the mask and the imaging system~~
- Models and experimental verification of optical and non-optical immersion lithography effects (e.g. topography and change of refractive index distribution)
- Simulation of multiple exposure/patterning including data base splitting
- Multi-generation lithography system models
- Simulation of defect influences / defect printing in EUV. Mask optimization including defect compensation.
- Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography
- Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects ~~and ultra-high NA effects (oblique illumination)~~
- Predictive resist models (e.g. mesoscale models) incl. line-edge roughness, etch resistance, adhesion, mechanical stability, leaching, and time-dependent effects in single and multiple exposure; resist processing techniques special for double patterning
- Resist model parameter calibration methodology (including kinetic and transport parameters)
- Simulation of e-beam mask making (single-beam and multibeam)
- Simulation of direct self-assembly of sublitho patterns
- Modeling lifetime effects of equipment and masks
- Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning)
- Modeling metrology equipment for enhancing its accuracy

Example (Fraunhofer IISB): Large-area rigorous simulation of optical lithography



Mask layout (dark-blue = Cr absorber)

Mask scale = 4 times wafer scale



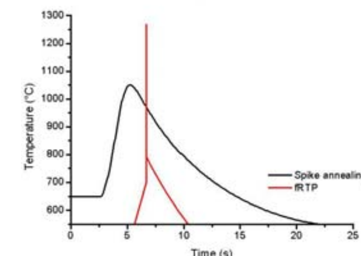
High resolution aerial image computed with Dr.LiTHO (Waveguide + new Imaging: 5.4 h on one CPU with 2.8 GHz. Additionally, efficient parallelization possible).

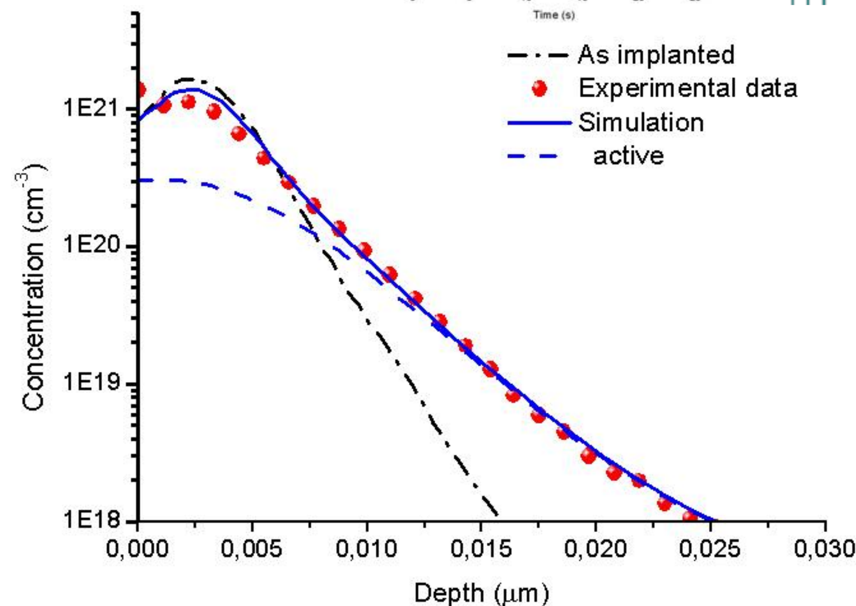
2009 Short-Term Difficult Challenges – changes from 2008 in blue/red

Front-End Process Modeling for Nanometer Structures

Needs

- Coupled diffusion/activation/damage/stress models and parameters incl. SPER and millisecond processes in Si-based substrate, that is, Si, SiGe:C, Ge-on-Si, ~~GaAs,~~ III/V-on-Si, SOI, epilayers and ultra-thin body devices, taking into account possible anisotropy in thin layers
- Modeling of interface and dopant passivation by hydrogen or halogens
- Modeling of cluster or cocktail implants
- Modeling of plasma doping, e.g. for FinFETs
- Modeling of epitaxially grown layers: Shape, morphology, stress, defects, doping
- Modeling of stress memorization (SMT) during process sequences
- ~~Characterization tools/methodologies for ultra-shallow geometries/junctions, 2D low dopant level, and stress~~
- Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
- Efficient and robust 3D meshing for moving boundaries
- Front-end processing impact on leakage (e.g. residual defects) and reliability





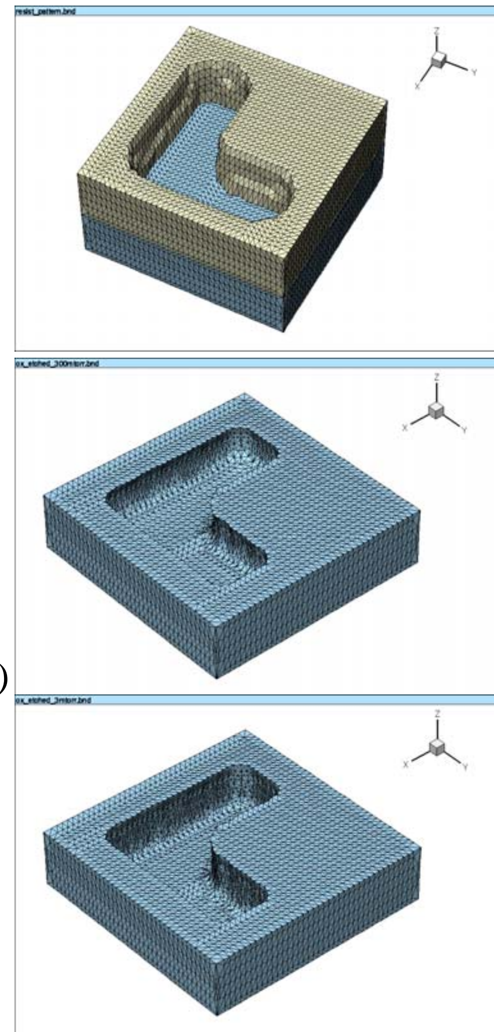
Source: P. Pichler et al. (FhG-IISB), Defect and Diffusion Forum 258-260, 510 (2006)

2009 Short-Term Difficult Challenges

Integrated Modeling of Equipment, Materials, Feature Scale Processes and Influences on Devices, including variability – changes compared to 2008 in blue

Needs

- Fundamental physical data (e.g. rate constants, cross sections, surface chemistry for ULK, photoresists and high-k metal gate); reaction mechanisms (reaction paths and (by-)products, rates ...) , and simplified but physical models for complex chemistry and plasma reaction
- Linked equipment/feature scale models (including high-k metal gate integration, damage prediction)
- Deposition processes: MOCVD, PECVD and ALD, electroplating and electroless deposition modeling
- Spin-on-dielectrics (stress, poriosity, dishing, viscosity, …) for high aspect ratio fills
- Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
- Simulation of polishing, grinding and wafer thinning in backend processing
- Efficient extraction of impact of equipment- and/or process induced variations on devices and circuits, using ~~process and device~~ simulation



Feature scale simulation of sputter etching: Initial geometry (top), simulation for 300 mTorr (middle) and 3 mTorr (bottom).

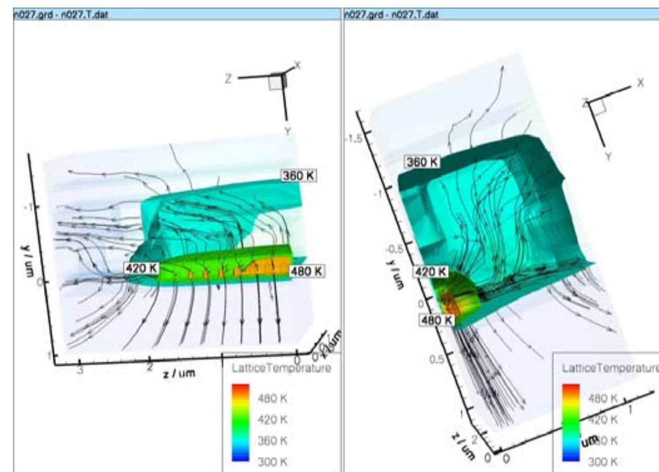
(From Fraunhofer IISB)

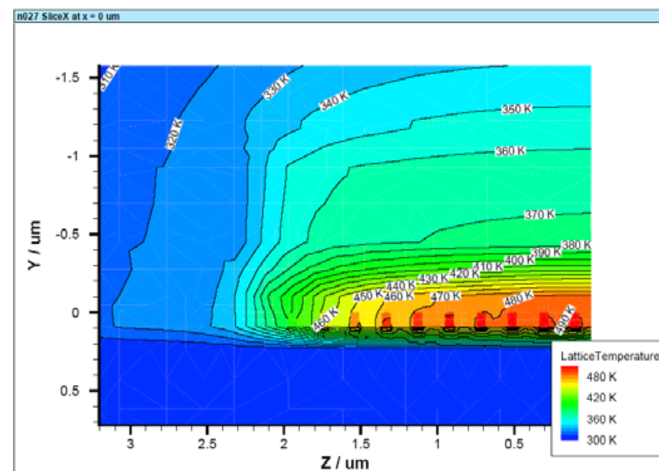
2009 Short-Term Difficult Challenges

Ultimate Nanoscale Device Simulation Capability: Methods, models and algorithms that contribute to prediction of CMOS limits – changes from 2008 in blue/red

Needs

- ~~Methods, models and algorithms that contribute to prediction of CMOS limits~~
- General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
- Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
- Models (incl. material models) to investigate new memory devices like MRAM, PCM/PRAM, etc
- Gate stack models for ultra-thin dielectrics w.r.t. electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport
- Modeling of contact resistance and engineering (e.g. Fermi-level depinning to reduce Schottky barrier height)
- Efficient device simulation models for statistical fluctuations of structure and dopant variations and efficient use of numerical device simulation to assess the impact of variations on statistics of device performance
- Physical models for novel materials, e.g. high-k stacks, Ge and compound III/V channels ….: Morphology, band structure, defects/traps, ….
- Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation
- Reliability modeling for ultimate CMOS
- Physical models for stress induced device performance





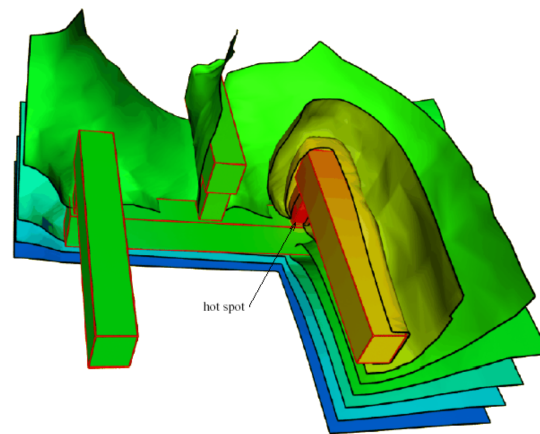
Lattice temperatures in device
Source: Infineon / ESSDERC 2006

2009 Short-Term Difficult Challenges

Electrical-Thermal-Mechanical-~~Electrical~~ Modeling for Interconnects and Packaging – changes from 2008 in blue/red

Needs

- Model thermal-mechanical, thermodynamic and electrical properties of low-k, high-k and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron
- Thermal modeling for 3D ICs and assessment of modeling tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, …). Size effects (microstructure, surfaces, ...) and variability of thinned wafers.
- Signal integrity modeling for stacked die
- Model effects which influence reliability of packages and interconnects incl. 3D integration (e.g. stress voiding, electromigration, fracture, dielectric breakdown, piezoelectric effects)
- Physical models to predict adhesion on interconnect-relavant interfaces (homogeneous and heterogeneous)
- Simulation tools for ~~of~~ adhesion and fracture toughness characteristics for packaging and die interfaces
- Dynamic simulation of mechanical problems of flexible substrates and packages
- Models for electron transport in ultra fine patterned interconnects



courtesy TU Vienna / IST project MULSIC

Temperature distribution in an interconnect structure

2009 Short-term Difficult Challenges

Circuit Element and System Modeling for High Frequency (up to 160 Ghz) Applications

-Changes from 2008 in blue/red

Needs

- Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3Dand package:
  - possibly consisting of different technologies,
  - covering and combining different modelling and simulation levels as well as different simulation domains
- Scalable active component circuit models including non-quasi-static effects, substrate noise and coupling, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling
- Scalable passive component models for compact circuit simulation, including interconnect, transmission lines, ~~RF MEMS switches,~~ …
- Scalable circuit models for more-than-moore devices including switches, filters, accelerometers, ...
- Physical circuit element models for new memory devices, such as PCM, and standardisation of models for III/V devices
- Computer-efficient inclusion of aging, reliability and variability including their ~~its~~ statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
- Efficient building block/circuit-level assessment using process/device/circuit simulation, including process variations

(From Philips)

2009 Difficult Challenges < 16 nm

Difficult Challenges < 16 ~~22~~ nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following:
	1) Gate stacks: Predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions.
	2) Models for novel integrations in 3D interconnects including airgaps and data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties
	3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. ~~Modeling-assisted metrology.~~
	4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	Ab-initio modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping, quantum dots, atomic electronics, multiferroic materials and structures, strongly correlated electron materials) Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …). Modeling impact of geometry, interfaces and bias on transport for carbon-based nanoelectronics
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling. Physical design tools for integrated electrical/optical systems
NGL Simulation	• Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal damage by electron scattering or charging effects) • Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process

2009 Requirement Tables

Only some general remarks here:

- Continued trend to delay items: Necessary research could not be done due to lack of resources (research funding)
- Many changes in technical details included
- Table continues to contain some items in “zebra” colour - according to ITRS guidelines: “Limitations of available solutions will not delay the start of production. In some cases, work-arounds will be initially employed. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity.“
  - ⇒ This means for simulation: It can be used, but with more calibration, larger CPU time/memory, less generality than in the end required ...
- Red here means “Solution not known, but this does not stop manufacturing”

More details given in tables & ITRS text

Thank you