2009 Litho ITRS Update

Lithography iTWG

July 2009

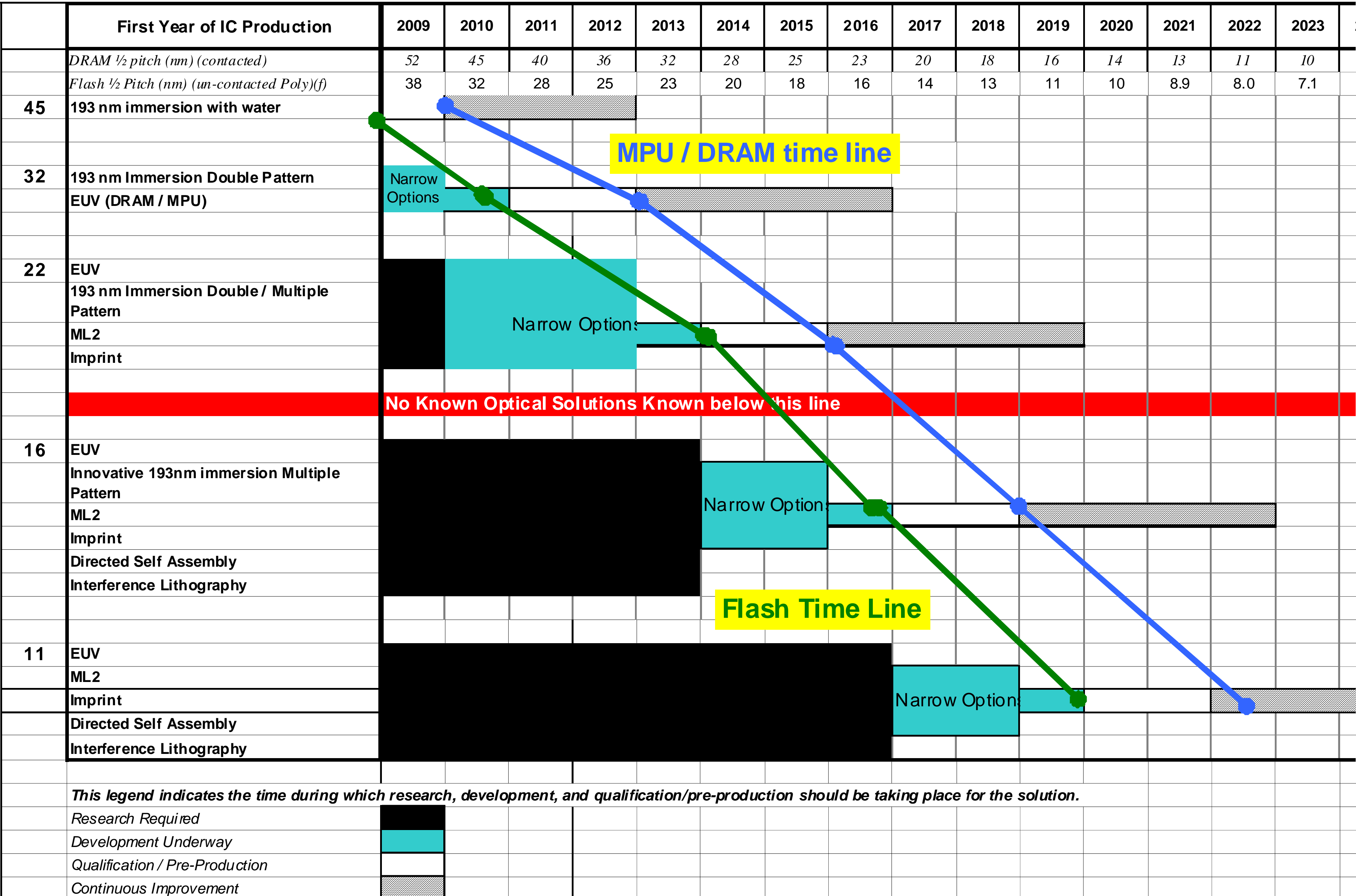
Outline

- Lithography Potential Solutions
- Major Challenges

ITRS Working Group

- United States
  - Greg Hughes SEMATECH (Chairs)
  - Mike Lercel IBM
- Japan
  - Takayuki Uchiyama NEC (Chair)
  - Naoya Hayashi DNP
  - Masomi Kameyama Nikon
  - Tetsuo Yamaguchi NuFlare
- Taiwan
  - Anthony Yen TSMC (Chair)

Potential Solutions 2009



Preferred Technology by Year

2008 SEMATECH Litho Forum survey results

2008 Combined Surveys

45nm HP | 32nm HP | 22nm HP

Response %

60%
40%
20%
0%

2008 2010 2012 2014 2016

193 dry SE
193i SE
193/193i DP
193 HIL#
EUVL+
NIL
ML2

\# Includes Double Patterning + Includes EUVL extension in 2016

2009 Litho Requirements

Table LITH3 Lithography Technology Requirements Version 2 - 05/08/2009

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
DRAM ½ pitch (nm) (contacted)	52	45	40	36	32	28	25	23	20	18
DRAM										
DRAM ½ pitch (nm)	52	45	40	36	32	28	25	23	20	18
CD control (3 sigma) (nm) [B]	5	4.7	4.2	3.7	3.3	2.9	2.6	2.3	2.1	1.9
Contact in resist (nm)	57	50	44	39	35	31	28	25	22	20
Contact after etch (nm)	52	45	40	36	32	28	25	23	20	18
Overlay [A] (3 sigma) (nm)	10	9.0	8.0	7.1	6.4	5.7	5.1	4.5	4.0	3.6
k1 193 / 1.35NA	0.36	0.31	0.28	0.25	0.22	0.20	0.18	0.16	0.14	0.12
k1 EUVL		0.83	0.74	0.66	0.59	0.52	0.47	0.58	0.52	0.46
Flash										
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23	20	18	16	14	13
CD control (3 sigma) (nm) [B]	4	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
Contact in resist (nm)	42	35	31	28	25	22	20	18	16	14
Contact after etch (nm)	38	32	28	25	23	20	18	16	14	13
Overlay [A] (3 sigma) (nm)	12	10.5	9.4	8.3	7.4	6.6	5.9	5.3	4.7	4.2
k1 193 / 1.35NA	0.26	0.22	0.20	0.18	0.16	0.14	0.12	0.11	0.10	0.09
k1 EUVL		0.61	0.55	0.49	0.43	0.39	0.33	0.41	0.37	0.33
MPU										
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	54	45	38	32	27	24	21	19	17	15
MPU gate in resist (nm)	47	41	35	31	28	25	22	20	18	16
*MPU physical gate length (nm) **	29	27	24	22	20	18	17	15	14	13
*Gate CD control (3 sigma) (nm) [B] ***	3.0	2.8	2.5	2.3	2.1	1.9	1.7	1.6	1.5	1.3
Contact in resist (nm)	66	56	47	39	33	29	26	23	21	19
Contact after etch (nm)	60	51	43	36	30	27	24	21	19	17
Overlay [A] (3 sigma) (nm)	13	11	9.5	8.0	6.7	6.0	5.3	4.7	4.2	3.8
k1 193 / 1.35NA	0.37	0.31	0.26	0.22	0.19	0.17	0.15	0.13	0.12	0.11
k1 EUVL		0.83	0.70	0.59	0.50	0.44	0.39	0.49	0.44	0.39
NA required for Flash (single exposure)	1.43	1.70	1.91	2.14						
NA required for logic (single exposure)	1.16	1.38	1.64	1.94	2.31					
NA required for double exposure (Flash)	1.02	1.22	1.36	1.53	1.72	1.93	2.17			
NA required for double exposure (logic)	0.80	0.95	1.12	1.34	1.59	1.78	2.00			
EUV NA minimum		0.25	0.25	0.25	0.25	0.25	0.25	0.35	0.35	0.35

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Single Litho Tool Overlay

2009 Litho Requirements

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Restricted Definition of CD - one direction, single pitch, single iso dense ratio.

2009 Lithography Techniques

Table LITH1 Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography for MPU and DRAM

MPU M1 contacted ½ pitch	*65 nm*	*45 nm*	*32 nm*	*Optical 22 nm*	*EUV 22 nm*
k 1 Range [A]	*0.31–0.40*	*0.28–0.31*	*0.18-0.28*	*0.14-0.22*	*0.58*
Design rules	Litho friendly design rules		Double exposure compatible design		Simple High k1 Design
Restrictions (cumulative)	Features on grid	Restricted feature set	Double exposure compatible design	Restricted feature set for Multi Exposure	None
Masks (Optical proximity correction)	Model-based OPC with vector simulation, SRAF, polarization corrections	All previous approaches + variation of OPC intensity by location in circuit.	All previous approaches + Dense OPC. & Source Mask Optimization	All previous approaches + Inverse Lithography	Simple Model based OPC. Similar Patterning Complexities 120nm node
(Gate and M1 layer mask type)	APSM, hiT EPSM, dual dipole	Binary, APSM, CLpsm, hiT EPSM, double exposure with 2x larger pitch			EUV (Binary)
(Contacts/ vias layers mask type)	Binary, EPSM, HiT PSM	EPSM, HiT PSM	HiT EPSM, double exposure with 2x larger pitch		EUV (Binary)
Resist					
Thickness	<225 nm	<160 nm	<120 nm	<66nm	<66nm
Substrate	ARC, hard masks, top coats		ARC, hard masks, top coats, contrast enhancing layers		Hard masks

NO Optical Solutions

Difficult Challenges > 22nm

Difficult Challenges > 22 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features
	Registration, CD, and defect control for masks
	Eliminating formation of progressive defects and haze during exposure
	Understanding and achieving the specific signature and specifications for a Double Patterned mask
	Establishing a stable process so that signatures can be corrected.
Double patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures
	Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
	Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
	Photoresists with independent exposure of multiple passes
	Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.

Difficult Challenges > 22nm

Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time
	ROI for small volume products
	Resources for developing multiple technologies at the same time
	Cost-effective resolution enhanced optical masks and post-optical masks, and
	450 mm diameter wafer infrastructure
Process control	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3s overlay error
	Controlling LER, CD changes induced by metrology, and defects < 10 nm in size
	Greater accuracy of resist simulation models
	Accuracy of OPC and OPC verification, especially in presence of polarization effects
	Lithography friendly design and design for manufacturing (DFM)

Difficult Challenges <= 22nm

EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components
	Cost control and return on investment
	Resist with < 1.5 nm 3s LWR, < 10 mJ/cm2 sensitivity and < 20 nm ½ pitch resolution
	Fabrication of Zero Printing Defect Mask Blanks
	Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection)
	Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs)
	Controlling optics contamination to achieve > five-year lifetime
	Protection of EUV masks from defects without pellicles
	Fabrication of optics with < 0.10 nm rms figure error and < 7% intrinsic flare
Resist materials	Limits of chemically amplified resist sensitivity for < 22 nm half pitch due to acid diffusion length
	Materials with improved dimensional and LWR control add (limits)
	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Low defects in resist materials (size < 10nm)
	Line width roughness < 1.4nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair)
	Mask process control methods and yield enhancement
	Cost control and return on investment

Difficult Challenges <= 22nm

Category	Challenge
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective post-optical masks
	Cost effective 450mm lithography systems
	Achieving ROI for small volume products
193 nm Immersion Multilple Patterning	Cost control and return on investment
	Wafer processing to tighter overlay and CD controls
	Mask fabrication to tighter specifications
Metrology and defect inspection	Defect inspection on patterned wafers for defects < 20 nm
	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3s
	Metrology for achieving < 2.8 nm 3s wafer overlay error
	Template inspection for 1X Imprint Patterned Masks
	Phase shifting masks for EUV
Gate CD control improvements and process control	Development of processes to control gate CD < 1.5 nm 3s with < 1.4 nm 3s line width roughness
	Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3s overlay error, especially for imprint lithography
Maskless Lithography	Wafer Throughput
	Cost control and return on investment
	Die-to-database inspection of wafer patterns written with maskless lithography
	Pattern placement - including stiching
	Controlling variability between beams in multibeam systems
Imprint Lithography	Defect-free Imprint templates at 1X dimensions
	Infrastructure for 1X technology Templates (key here is inspection!)
	Template fabrication to tighter specifications
	Protection of Imprint templates from defects without pellicles
	Mask Life time
	Throughput
	Cost control and return on investment
	Overlay
	Process control methods to compensate for systematic CD and overlay errors

Summary

- Lithography solutions for 2010
  - 45 nm half-pitch CoO is Driving 193 Immersion Single Exposure for DRAM/MPU
  - Flash using Double Patterning (Spacer) for 32 nm half-pitch
- Lithography solutions for 2013
  - 32 nm half-pitch Double patterning or EUV for DRAM/MPU
  - 22 nm half-pitch Double patterning or EUV for Flash
- Double exposure / patterning requires a complex set of parameters when different exposures are used to define single features
- LER and CD Control Still remain as a Dominant Issue
- Mask Complexity for Double patterning
- Mask Infrastructure for EUV