Test and Test Equipment

July 2009

San Francisco, USA

Roger Barth - Numonyx

ITRS Test TWG

2009 Test TWG

Name	Affiliation
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Mike Bienek	AMD
Amit Majumdar	AMD
Peter Maxwell	Aptina
Calvin Cheung	ASE
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Tetsuo Tada	Bunri University, Japan
Shawn Fetterolf	IBM
Anne Gattiker	IBM
Phil Nigh	IBM
Jody Van Horn	IBM
Dennis Conti	IBM
Frank Poehl	Infineon
Wendy Chen	KYEC
Yi Cai	LSI
Jerry McBride	Micron

Name	Affiliation
Roger Barth	Numonyx - Chair
Wataru Uchida	Renesas (STRJ)
Sejang Oh	Samsung
Steven Slupsky	Scanimetrics
Davide Appello	STMicroelectronics
Sridhar Kannan	Stream Processors
Prasad Mantri	Sun Microsystems
Tom Williams	Synopsys
Bill Price	T2C2
Brad Robbins	Teradyne
Steve Comen	TI
Takumi Aoki	Toshiba (STRJ)
Phil Burlison	Verigy
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Erik Volkerink	Verigy
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Paul Roddy	Consultant
Peter Muhmenthaler	Consultant
Rene Segers	Consultant

2009 Drivers

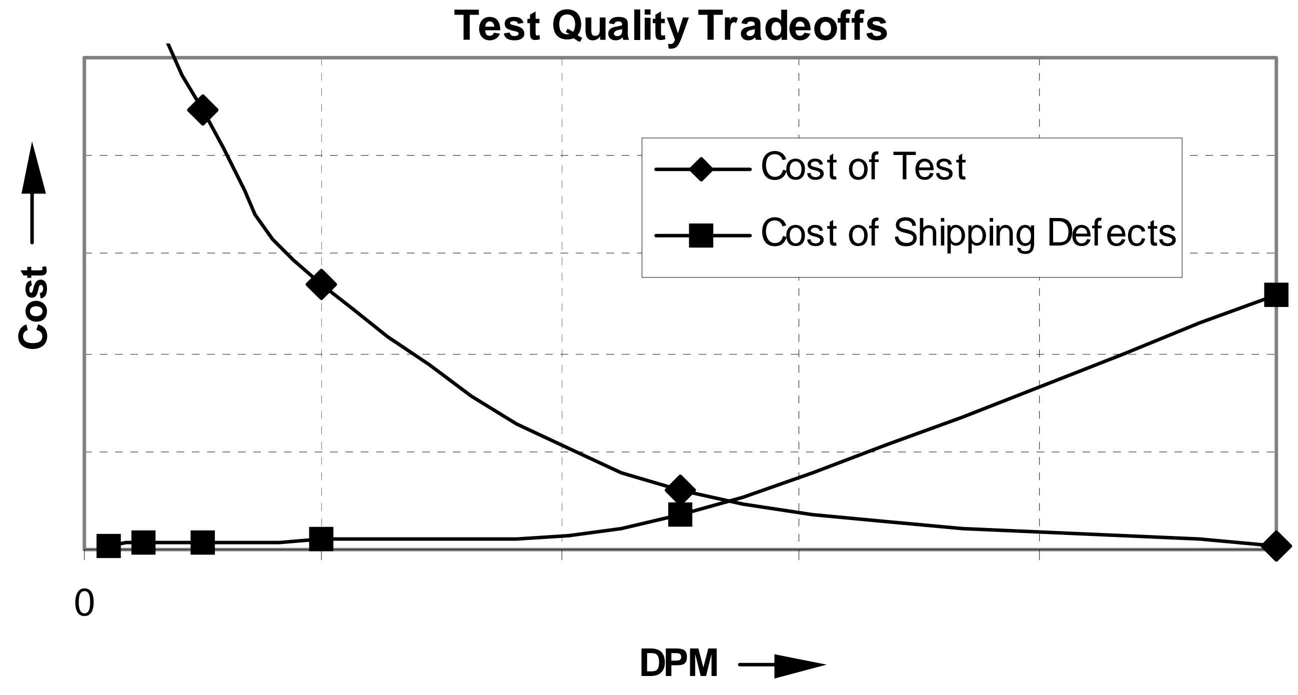
- Device trends
  - Increasing device interface **bandwidth** (# of signals and data rates)
  - Increasing **device integration** (SoC, SiP, MCP, 3D packaging)
  - Integration of emerging and **non-digital CMOS** technologies
  - **Complex package** electrical and mechanical characteristics
  - Device **characteristics beyond** one sided **stimulus/response** model
  - **Multiple I/O types and power supplies on same device**
- Increasing test process complexity
  - Device **customization** during the test process
  - "**Distributed test**" to maintain cost scaling
  - **Feedback** data for tuning manufacturing
  - **Dynamic test flows via "Adaptive Test"**
- Continued economic scaling of test
  - **Physical limits** of test parallelism
  - Managing (logic) test data and feedback **data volume**
  - Effective limit for speed difference of **HVM ATE versus DUT**
  - Managing **interface hardware** and (test) socket costs
  - Trade-off between the **cost of test** and the **cost of quality**
  - **Multiple Test insertions** due to **System test and BIST**

Economic Scaling of Cost of Test

- Goal: Maintain Moore's Law learning per technology
- Effective use of DFT die size budget per litho
- Make the device appear "smaller"
  - Concurrent test of similar structures or cores
  - Memory folding and compression
- Higher parallelism on reduced pin interfaces
- Self Test
- Reuse of older tools
- Guaranteed "performance" by proving "functionality"
- Techniques for "specialty" devices
  - LCD Display drivers, MEMS, Imaging devices

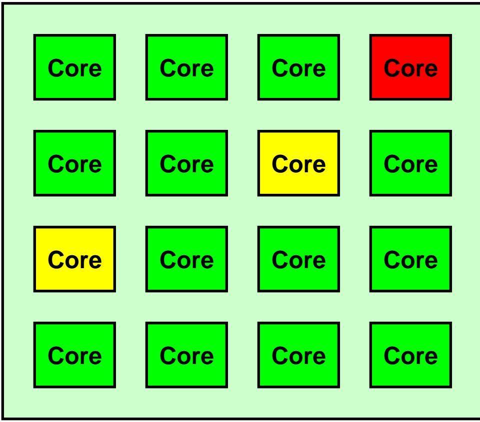
Cost of Quality

- Test is a balance of DPM and cost
- Shipped defect cost is more than bad components
  - Customer relationships, goodwill, penalties



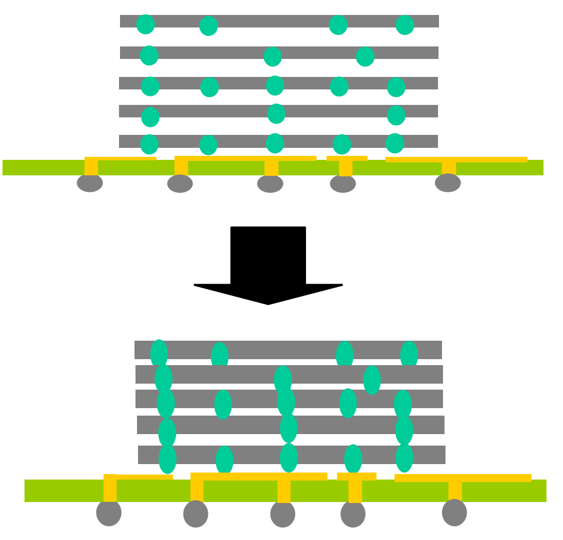
Fault Tolerant Devices “Bad but Good”

- “Adapt or Repair”
- Homogeneous multi-core device…not all cores need be good
  - Identify with “Smart kernel” or continuous test…
  - …Ignore the core
  - …Fix (run slower or tailor operations)
- Memory
  - Allow or correct bad bits / blocks
  - Background memory checker
  - Wear leveling
- Image sensors without the “perfect” image
  - What is perfect?



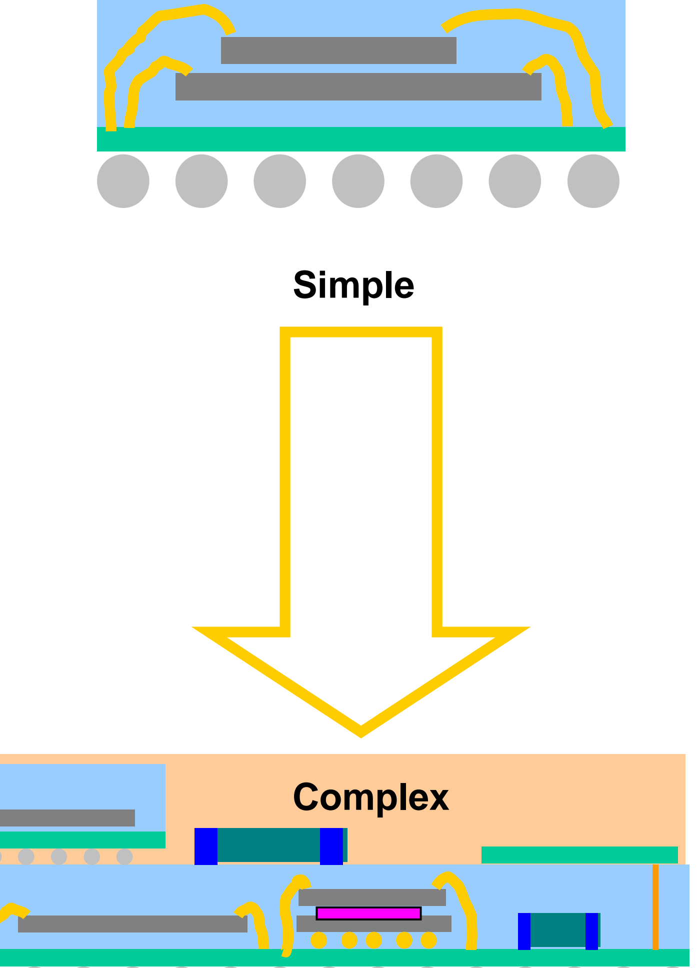
3D Devices

- Multiple die system
  - Sub-systems designed to operate and be assembled together
  - Process optimized for contents of each die
  - Connection by potentially 1000's of TSVs (Thru Silicon Via's)
- Design, Interconnect, Assembly and Test problem
- DFT Requirements
  - Testability of each die
  - Via continuity checks
    - For signal and non-signal vias
    - 3-5 um via cannot be probed! ESD!
  - N+ die test methodology as die added
  - Final "System" test
- Doable!



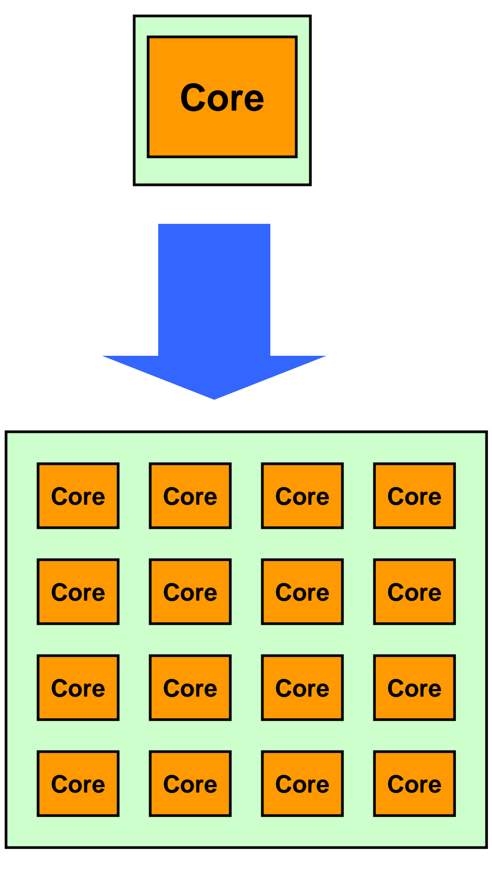
System in Package (SiP)

- Targets low power devices
- Challenges
  - High yield with low test cost
  - Standardized test strategy for mini-systems
- Potential test solutions
  - Design for die, debug and system test
  - Per die BIST
  - KGD with minimal post test
    - “KGD” defined as Functional and Structural good?



High End Logic

- Trend: Single to Multi core
  - Forecast: 22 cores by 2020
- I/O GT/s increasing
  - Aligned to number of cores
  - Multi-lane HS serial to 20GT/s
- Non-diff I/O will remain below 2 GT/s
  - Accuracy and noise limitations
- Structural test at low speed
  - Vectors increasing with Flip-Flop count



2008 update

MPU "GHz" by "Cores"

CPU "GHz"

1000
100
10
1
0.1
0.01
0.001
0.0001

1970 1980 1990 2000 2010 2020 2030

Actual
Forecast

CLK (GHz)
Clk Roadmap
Cores * Clock

~17x

Assumes 2007 CLK & cores roadmap

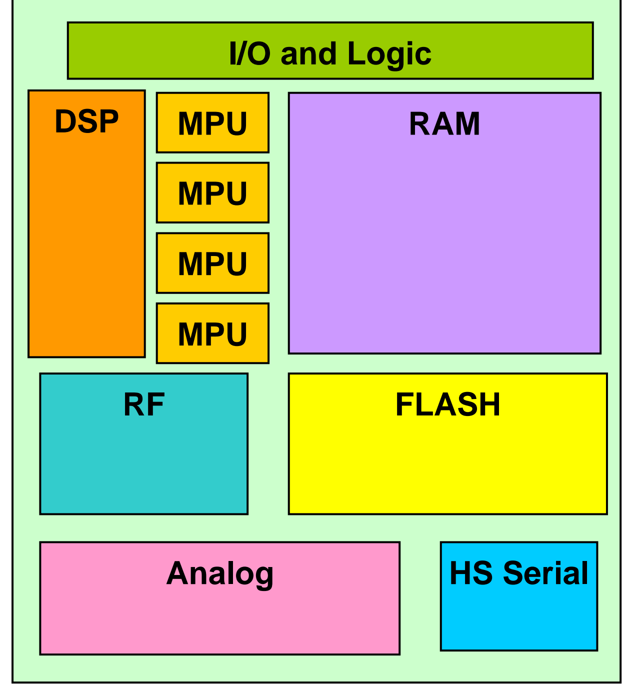
Pentium
8080
4004

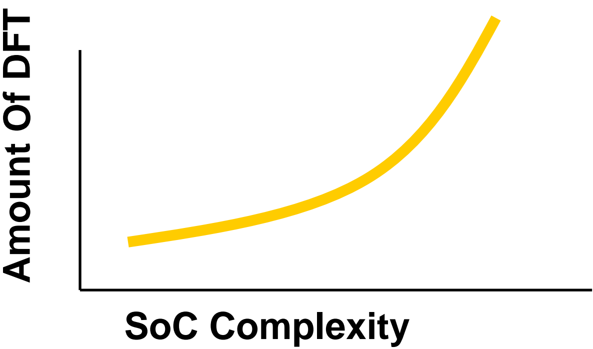
Multiple cores will continued historic "GHz" trend with a slower ramp in CLK rates

SoC – Consumer Logic

- > **1000** cores by 2020
  - MPU / logic
  - Memory
  - Analog / RF
  - HS serial

- SoC test challenges
  - Management of per core DFT
  - Standardization of core “wrappers”
    - IEEE 1500 core test
    - IEEE P1687 JTAG chip-test
  - High Data Compression (>100)





DFT Compression Potential Solutions

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Required compression	80	200	300	500	750	1300	2000	3300	4800	7300	12000	2000	35000	67000	?	?
1-dimentional Test-cube compression (100X)																
2-dimentional Spatial compression(500X)																
3-dimentional Time correlations compression(1000X)																
Multi-dimensional compression(5000X)																

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

- Development is necessary to get very high levels of data compression
- Demonstrated techniques are just approaching 1000x
- 100k data compression necessary out in time

Test Time Reduction Potential Solutions

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Required Test time reduction	1x	2x	2x	2x	2.5x	2.5x	2.5x	3.2x	3.2x	3.2x	4.2x	4.2x	4.2x	5.6x	?	?
Multi-site Test																
Core-Parallel Test																
Test Vector Reduction (include compression)																
Test per clock																

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

- Driven by SoC
- Assume increasing design complexity and transistor count cannot be increase test time

Proliferation of Cores

10000
1000
100
10
1

CPU total cores
CPU Unique cores
Consumer total cores
Consumer Unique cores

Consumer devices lead CPUs in core quantity and types

~10x

Consumer

CPU

2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022

Test Data Volume

CPU - Concurrent Core Test
Consumer - Concurrent Core Test
CPU - No Concurrent Test
Consumer - No Concurrent Test

CPU

Consumer

Giga Pin Vectors

10,000
1,000
100
10
1

2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022

Concurrent core test can reduce test data volume

Assumes only identical cores are tested in parallel.

4-10x Reduction in Test Data volume with Concurrent Test

High Speed Interfaces

SONET	Ethernet	FC
SATA	PCIe	Infiniband
XAUI	OIF	SAS
FB DIMM	25Gbps standards	

PHY Bit Rate (Gb/s): 0.1, 1, 10, 100, 1000

Year: 1990, 1995, 2000, 2005, 2010, 2015, 2020, 2025

Physical Limit due to packaging and test socket

Technology Leverage Point

Test Sockets are not able to support controlled impedance contacts at >15 GT/s

- Bit bandwidth increasing – Physical limit? Test limit?

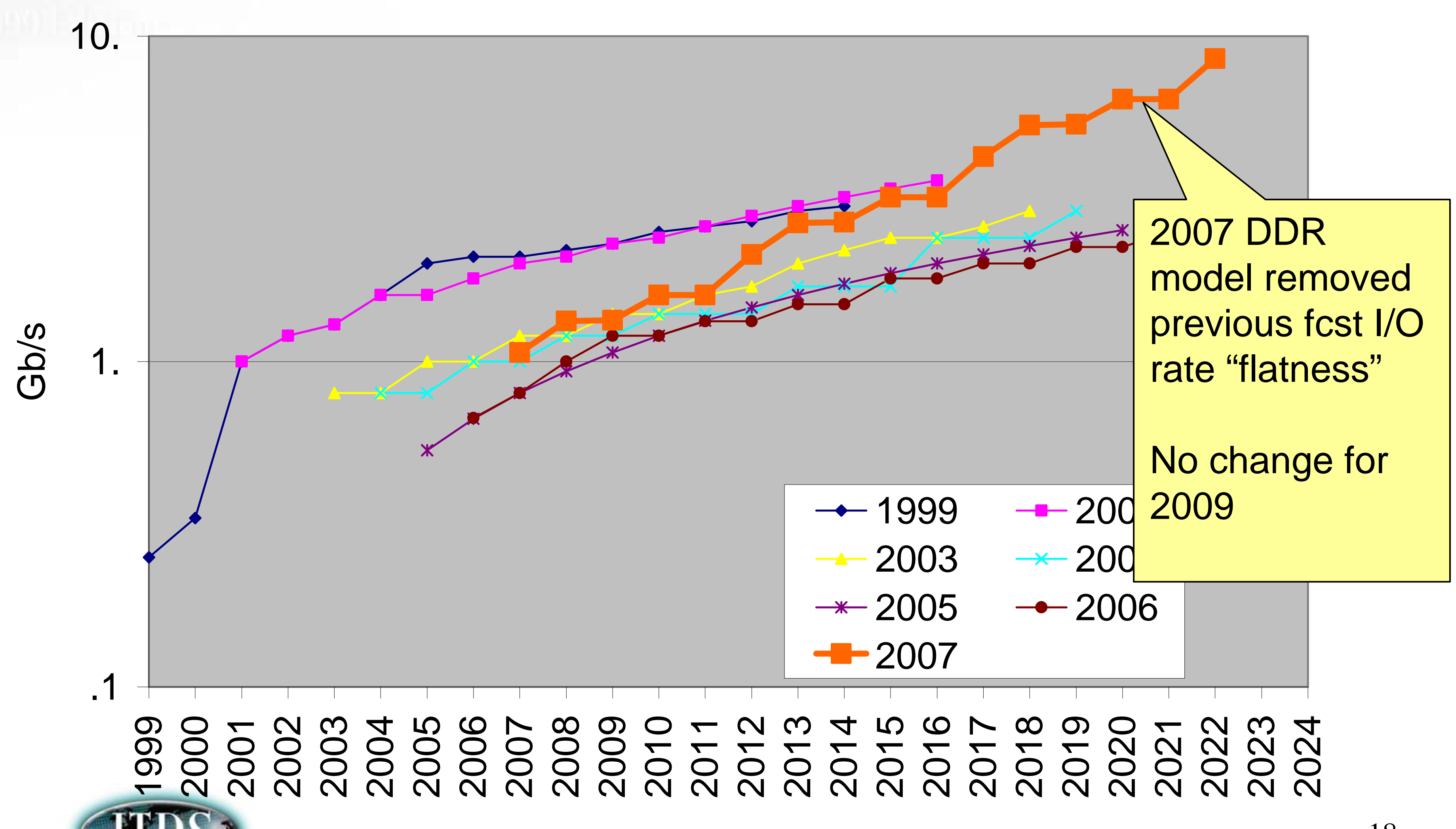
DRAM Model

- DDRx family trends
  - 3 primary bit rates
  - two optional rates
  - Intro year
    - First two speeds
- DDRx to DDRy cycles
  - 2000→2007 - 3 years
  - 2007+ - 5 years

		single I/O MegaTransitions per second						
	Clk	SDR	DDR	DDR2	DDR3	DDR4	DDR5	DDR6
1997	133	133						
1998	133	133						
1999	166	166						
2000	166	166	266 333					
2001	200		400					
2002	200		400					
2003	266			400 533				
2004	333			666				
2005	333			666				
2006	400			800				
2007	533			1066	800 1066			
2008	666				1333			
2009	666				1333			
2010	800				1600			
2011	800				1600			
2012	1066				2133	1600 2133		
2013	1333					2666		
2014	1333					2666		
2015	1600					3200		
2016	1600					3200		
2017	2133						3200 4266	
2018	2666						5333	
2019	2666						5333	
2020	3200						6400	
2021	3200						6400	
2022	4266							6400 6532

DDR5 and DDR6 roadmaps are pure speculation

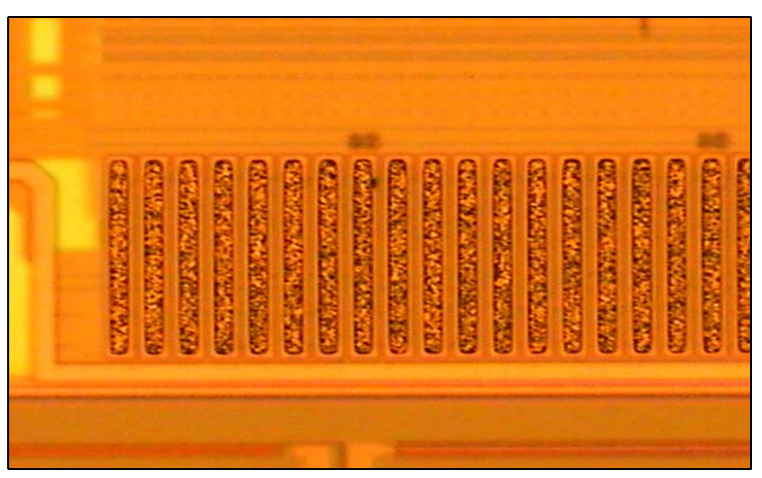
DRAM I/O Data Rate



Specialty Devices

1.5x30mm - Linear CCD Image Sensor

- LCD drivers
  - Form factor of 30mm x 1.5mm
  - Long bond pads on 20um centers
- Image sensors
  - Micro lens check with pupil test
- 3 axis MEMS Accelerometer
  - Consumer drop/rotate applications



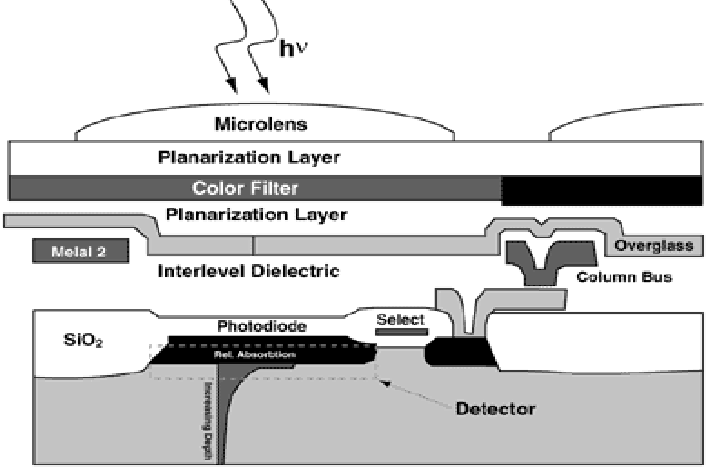


Image sensor structure cross section

Mechanical Handling Complexities

- Small ball pitches on high parallelism memory (>0.4mm)
- Very small packages (2mm x 3mm)
- Testing and handling of < 20um “thin” die
- High test parallelism
- Product specific optimizations
- 450mm wafers

Roadmap Changes for 2009

- DFT
  - Test compression and test time potential solutions
- Test Cost
  - Test cost survey completed to quantify industry issue
  - Test parallelism dependency modified based on I/O count
- Adaptive Test
  - New chapter section shows necessity for cost effective test
- Prober
  - Complete redo of prober table to address parallelism and power
- Probecard
  - LCD display driver probe added as driver
- Handler
  - Add 10-50 Watt handler category
- Test Sockets
  - Socket BW limitations; new contacting solutions needed