Metrology Roadmap
2009

Europe	Bart Rijpers (ASML)
Japan	Yuichiro Yamazaki (Toshiba) Eiichi Kawamura (Fujitsu Microelectronics) Masahiko Ikeno (Hitachi High-Tech)
Korea	
Taiwan	
North America	Meridith Bebe (Technos) Ben Bunday (ISMI) Alain Diebold (CNSE – Univ. Albany) Brendan Foran (Aerospace) Dick Hockett (EAG Labs) Jack Martinez (NIST) George Orji (NIST) Dave Seiler (NIST)

2009 ITRS Changes

		2008	2010	2012	2014	2016	2018
	Flash 1/2 pitch (nm)	***45***	***36***	***28***	***22***	***18***	***14***
	DRAM ½ Pitch (nm)	**59**	**45**	**36**	**28**	**23**	**17.9**
	MPU Printed Gate Length (nm)	**47**	**41**	**31**	**25**	**19.8**	**15.7**
	MPU Physical Gate Length (nm)	**29**	**27**	**22**	**18.4**	**15.3**	**12.8**
	Wafer Overlay Control (nm) - 20% DRAM	**11.9**	**9.0**	**7.1**	**5.7**	**4.5**	**3.6**
	Wafer Overlay Control Double Patterning (nm)	**8**	**6**	**5**	**4**	**3**	**3**
	Lithography Metrology						
Gate	Physical CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	3.0	2.8	2.3	1.9	1.6	1.3
Gate	Wafer CD metrology tool **uncertainty** (3s, nm) at P/T = 0.2	0.60	0.55	0.46	0.38	0.32	0.27
Gate	Etched Gate Line Width Roughness (nm) <8% of CD	2.3	2.1	1.8	1.5	1.2	1.0
Dense Lines	Printed CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	4.7	3.7	2.9	2.3	1.9	1.5
Dense Lines	Wafer CD metrology tool **uncertainty** (3s, nm) at P/T = 0.2	1.1	0.8	0.7	0.5	0.4	0.3
	Double Patterning Overlay Metrology						
	Double Exposure and Etch - Process Range (nm)	8.4	6.4	5.1	4.0	3.2	2.5
	Double Exposure and Etch - **Uncertainty** (nm)	1.68	1.27	1.01	0.80	0.64	0.51
	Spacer PEE process						
	First pass CD control (after etch) - Process Variation (nm)	3.9	3.0	2.4	1.9	1.6	1.3
	First pass CD control (after etch) - Uncertainty (nm)	0.8	0.6	0.5	0.4	0.3	0.3
	Front End Processes Metrology						
	High Performance Logic EOT equivalent oxide thickness (EOT), nm	1.1	0.65	0.5	0.5	0.5	0.5
	Logic Dielectric EOT Precision 3σ, nm	0.0044	0.0026	0.002	0.002	0.002	0.002
	Interconnect Metrology						
	Barrier layer thick (nm)	5.2	3.3	2.4	1.7	1.3	1.1
	Void Size for 1% Voiding in Cu Lines	5.937785598	4.5	3.571652367	2.834822362	2.25	
	Detection of Killer Pores at (nm) size	5.937785598	4.5	3.571652367	2.834822362	2.25	

Lithography Metrology for Advanced Patterning

Double Exposure

Metrology Need:

Latent Image CD

CD-AFM after both exposures but no Solution for CD between exposures

Double Patterning

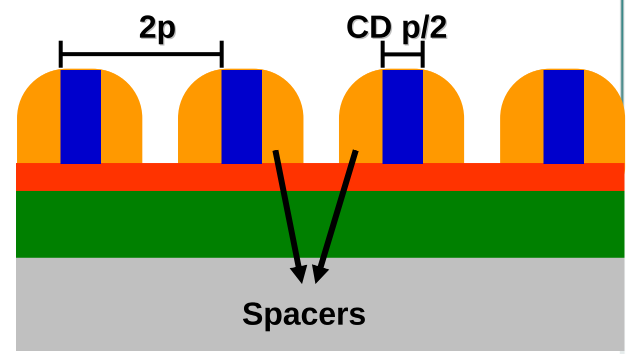
Metrology Need:

Overlay with

Precision of 70%

Of Single Layer

Spacer Patterning



Metrology Need:

Spacer Thickness on Sidewall

Spacer Profile

22 nm Dense lines

Metrology Challenges for Advanced Litho Processes

Double Exposure	Double Patterning	Spacer Double Patterning
32/22 nm 1/2 Pitch		
For alignment need to measure latent image in	Sidewall Angle (SWA) and Height Accuracy for odd and	Spacer sidewall Thickness Uniformity across entire
	Overlay at resolution (i.e. with targets at device size) : what is	SWA of odd and even lines
		shape
Mask ima... M...		uniformity ...er
	Mask CD Uniformity Metrology	...ormity Metrology

2 Population CD, SWA, height and pitch

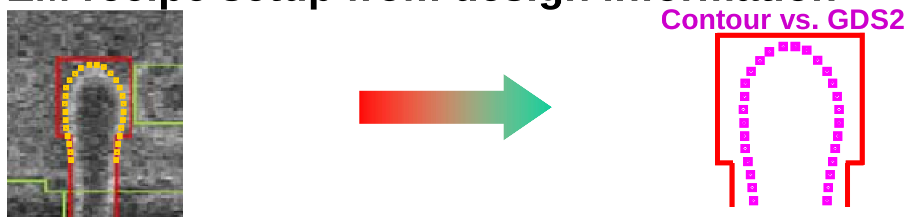
Potential Solution -> scatterometry

Q: is there enough sensitivity for odd-even line scenario

Metrology for Latent Image at 1st exposure might be avoided using AEC/APC approaches & CD/Overlay after double exposure

Contour Metrology

- **For CD-SEMs, Design-Based Metrology (DBM) applications allow for practical SEM verification of design intent, through the collection of feature 2D contour shape information and comparison to GDS files.**
  - **automatic CD-SEM recipe setup from design information**



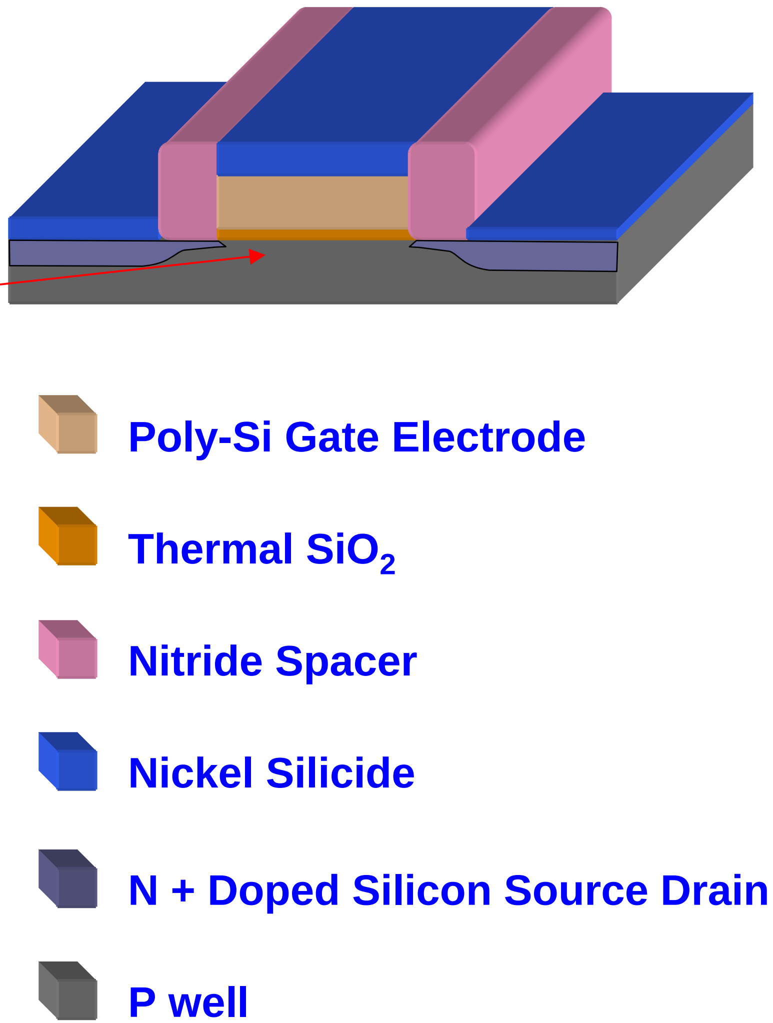
- **DBM applications very important for development and verification of OPC**
  - **number of measurements for successfully developing OPC is expected to grow exponentially with technology generation.**
  - **metrology interfaces with the Design for Manufacturing (DFM) community.**

- **Contour fidelity is a prevailing challenge**
  - **Accuracy of contour extraction → strong implications for OPC**
  - **Accuracy of registration → strong implications for in-die overlay**

- **Remaining work : *define:***
  - **contour error source testing methodologies**
  - **contour reference metrology**
  - **SEM modeling for contours**

FEP Metrology

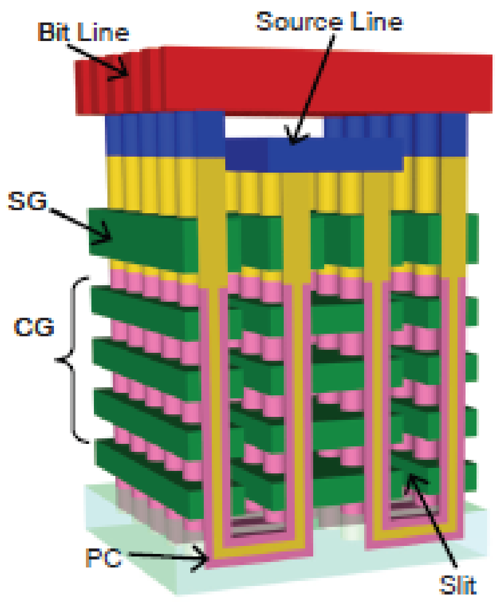
- **New High K – Metal Gate Materials**
- **III-V and SiGe Channels**
- **New Memory Materials (e.g. Phase Change Memory -- polycrystalline chalcogenide)**



FEP Metrology

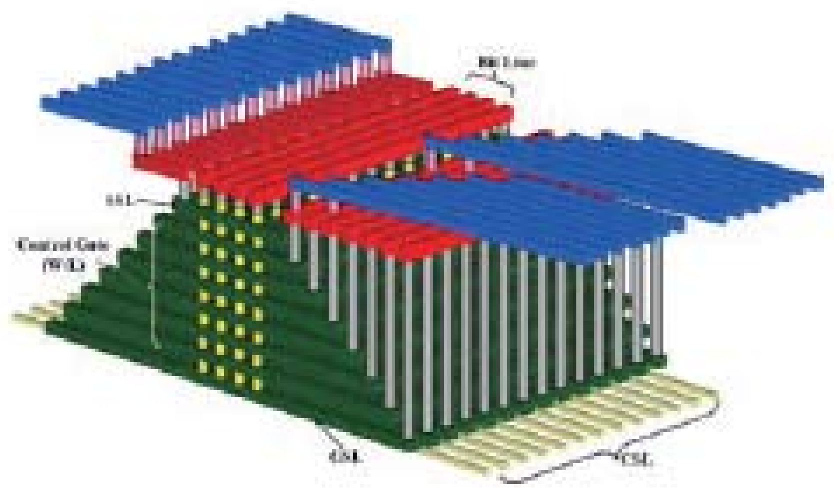
3D Metrology – Complex structure measurement and inspection are required

e.g. high A/R holes, film thickness & properties on sidewall



Pipe-shaped BiCS Flash Memory

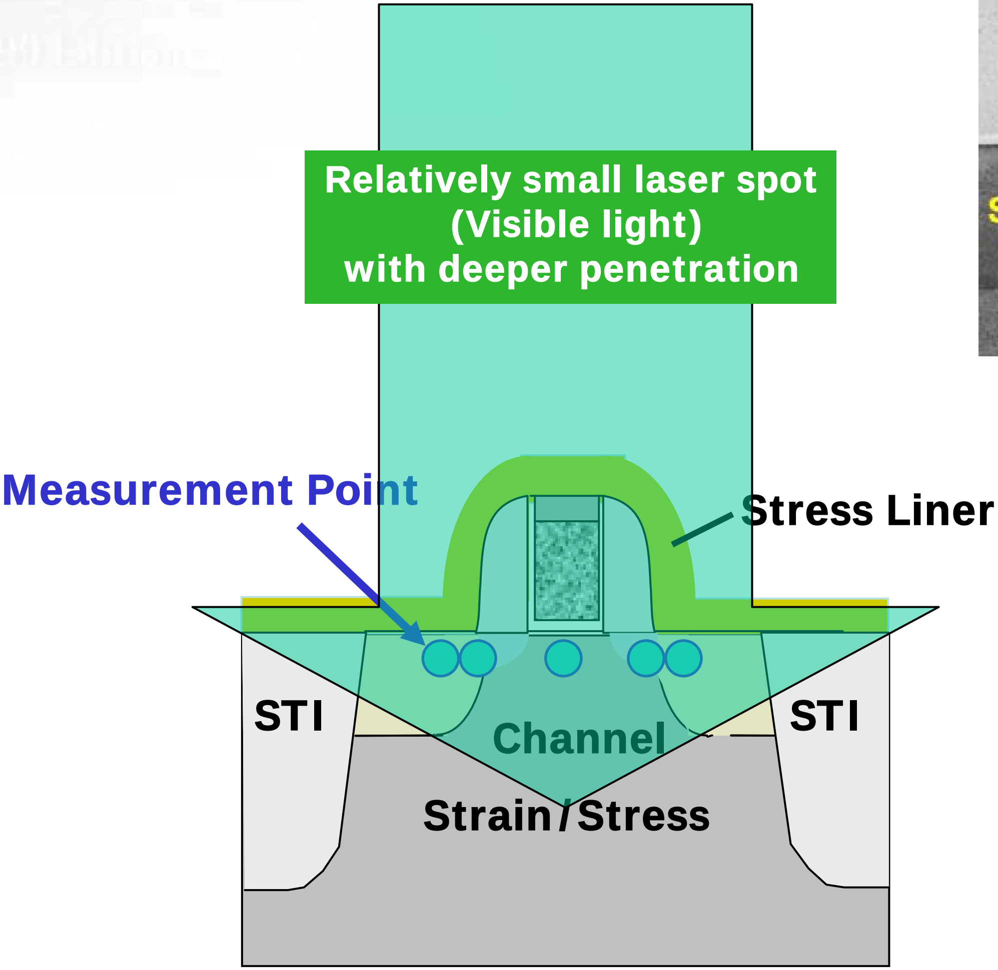
(R. Katsumata, Toshiba)

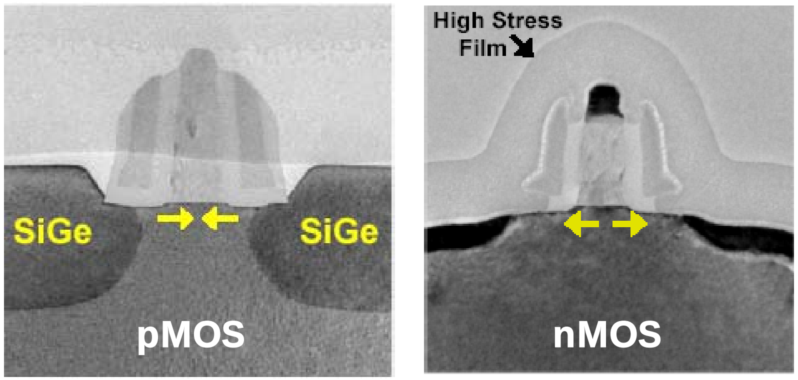


TCAT (Terabit Cell Array Transistor)

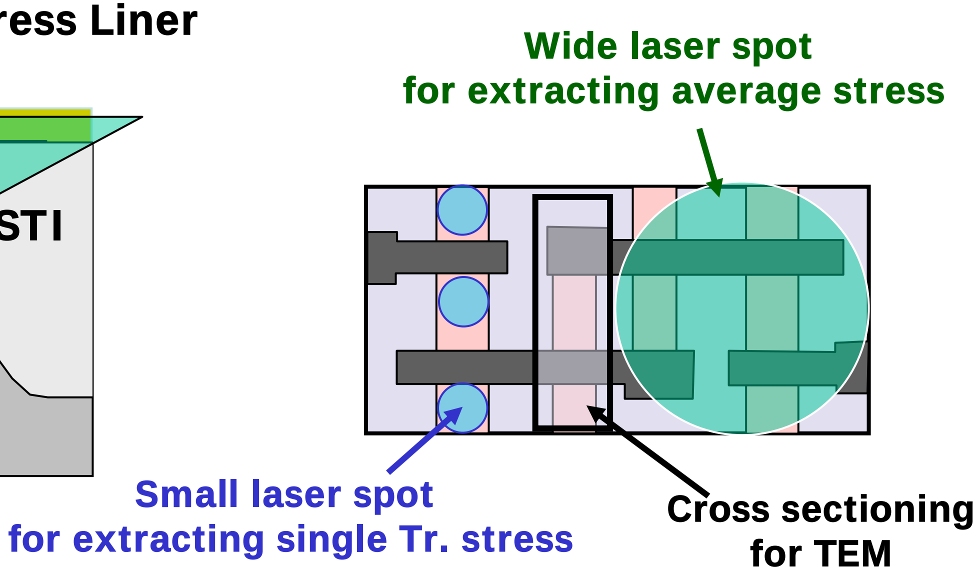
(J. Jang, Samsung)

Local Strain/Stress Measurement

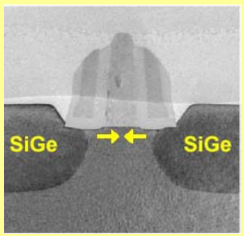
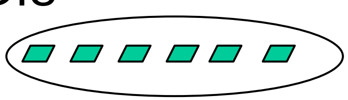




Ghani, et al (Intel)



Local Stress/Strain Measurement Method

Area of Interest	Measurement Method	Sensitivity		Measurement Area	Sample Thickness	
		Stress	Strain			
Transistor Level 	- CBED	20 MPa	0.02%	10-20nm	<100nm	Destructive
	- NBD	100 MPa	0.1%	~10nm	<300nm	Destructive
	- TERS	50 MPa	0.05%	<50nm		Destructive Non-Destructive
Micro-Area Level 	- Confocal Raman	20 MPa	0.02%	~150nm		Non-Destructive
	- XRD	10 MPa	0.01%	100um		
	- Photo reflectance Spectroscopy	<20MPa	<0.02%	1um		***Handling Area of ITRS***
Die 	- Die level flatness - Laser Interferometry - Coherent Gradient Sensing					Non-Destructive
Wafer 	- Laser Interferometry - Coherent Gradient Sensing					Non-Destructive

* Stress – Strain relation : need to be clarified

TERS (Tip Enhanced Raman Scattering)
CBED (Convergent Beam Electron Diffraction)
NBD (Nano Beam Electron Diffraction)
XRD (X-ray Diffraction)

New table for Local Stress/Strain Measurement

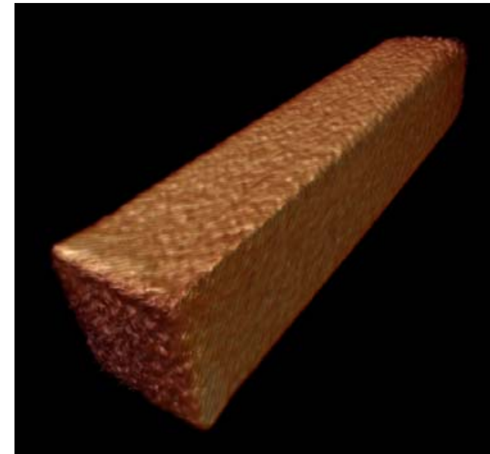
need inputs from FEP and PIDS

Front End Processes Metrology Technology Requirements—Near-term Years

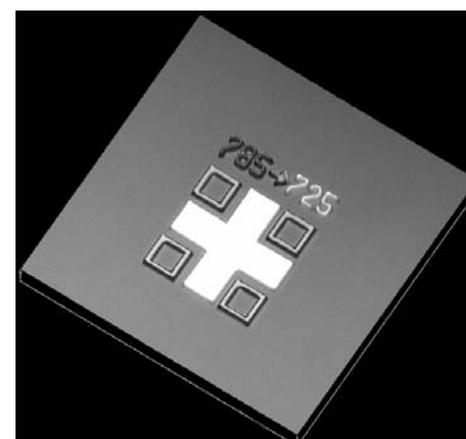
Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Stress measurement with 50MPa resolution									
Spatial resolution (Offline, destructive, single	5	4.4	4	3.6	3.2	2.8	2.6	2.2	2
Spatial resolution (Inline, non-destructive, Test pattern for average stress measurement)	Same size with HP								
	65	57	50	45	40	36	32	28	25
	Using test pad of 100um X 100um								
	100	100	100	100	100	100	100	100	100
Throughput (wafers/hour) (Inline, non-destructive, Test pattern)	25 sites per wafer								
	2	2	2	2	2	2	2	2	2

Need to modify according to ORTC modification

2009 Interconnect Metrology



- Existing Challenges
  - Measurement Gap - Sidewall barrier thickness and sidewall damage (compositional changes in low k)
  - New - Porous low k is projected for 32 nm ½ Pitch
  - Detection of Voids after electroplating
  - Monolayer interface for new barrier-low k
- Air Gap sacrificial layer does not require unique metrology
- Metrology is needed for 3D Integration
  - TSV Depth and Profile through multiple layers
  - Alignment of chips for stacking – wafer level integration
  - Bond strength
  - Defects in bonding
  - Damage to metal layers
  - Defects in vias between wafers
  - Through Si via is high aspect ratio CD issue
  - Wafer thickness and TTV after thinning
  - Defects after thinning including wafer edge



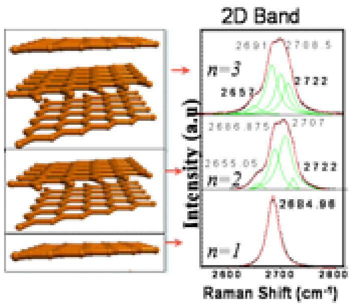
Questions for Interconnect

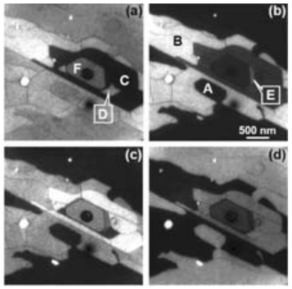
- Describe the new copper contact process and metrology issues
- In addition to TSV, what issues face 3d Interconnect for metrology

Metrology for ERM/ERD

High carrier mobility and structural robustness have driven a considerable effort in Graphene research

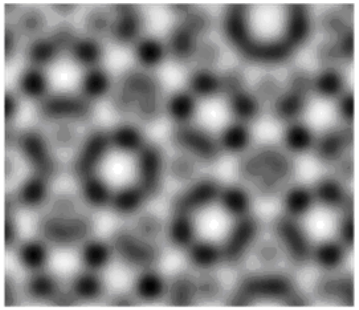
How many Layers? Raman and LEEM



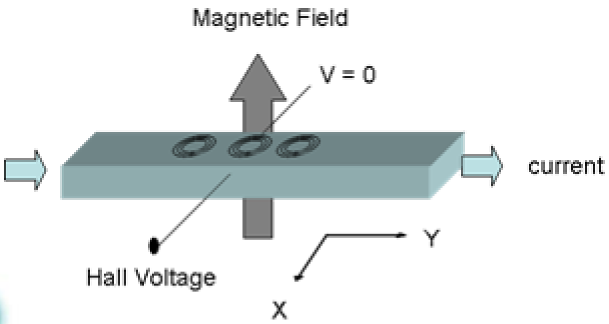


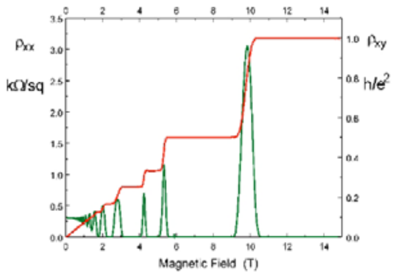
Measurement of Bi-layer misorientation

Aberration corrected TEM



Quantum Hall Effect observes the Berry Phase

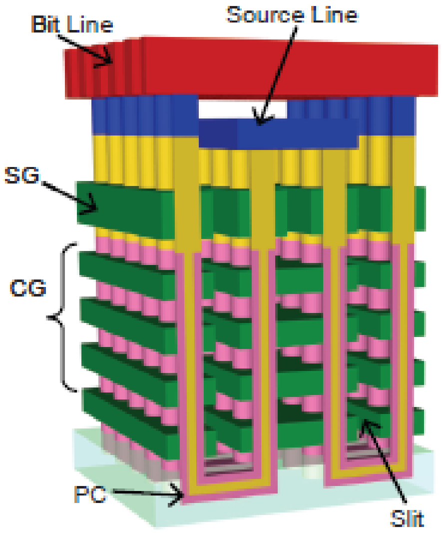




Metrology Summary

- **FEP-Interconnect-Litho**
  - PC and SST RAM - New materials for Metrology
  - Dual Patterning
  - 3D Metrology – Confirm Geometry Requirements e.g. film thickness & properties on sidewall
  - Reference Methods for 3D
  - Composition & Stress – e.g. buried channels
  - EUV metrology requirements
- **ERD-ERM**
  - Properties of low Dimensional Materials
  - Microscopy and feature size/function
  - Time resolved magnetic measurements
  - Ability to perform real time measurements, e.g. phase transitions

3D Metrology for Advanced Memory



Graphene – C. Kisielowski