2009 ITRS ORTC

Public Presentation 07/15/2009

A. Allan - Rev 9, 07/14/09

7/15 2009 ITRS ORTC Pre-Summary

1) ORTC Model Completed and delivered to TWGs for San Francisco TWG Interdependency Preparation
   1) MPU Model completed based upon Design TWG model proposals
   2) Dimensional trend “Node” “Score Card” updated to include Foundry positioning
   3) Memory Chip Size and density models complete based on Brussels proposal presentation by PIDS
   4) “Frozen” ORTC tables delivered to the TWGs for their preparation work
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   1) 2yr cycle trend through 2013
   2) Cross-over DRAM M1 2010/45nm
   3) Plus Smaller 60f^2 Design TWG SRAM 6t cell Design Factor
   4) Plus Smaller 175f^2 still proposed Logic Gate 4t Design Factor
3) DRAM M1
   1) Unchanged from 2007/08 ITRS
   2) However, new 4f2 Design factor begins 2011
4) Flash Un-contacted Poly – extend 2yr cycle trend to 2010/32nm (1-year pull-in); then 3yr cycle
   1) Inserted 3bits/cell MLC 2009-11; and
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6) MPU GLph – 1-yr delay; Low operating and standby line items track changes
7) MPU Functions/Chip and Chip Size Models
   1) Utilized Design TWG Model for Chip Size and Density Model trends – tied to technology cycle timing trends and updated cell design factors
   2) High Performance MPU Transistors/chip crosses DRAM bits/chip in 2009 at 2Bt/2Gbits!
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8) DRAM Bits/Chip and Chip Size Model
   1) 1-yr push-out, 3yr generation "Moore's Law" doubling cycle;
   2) smaller Chip Sizes (<60mm2) with 4f2 design factor included
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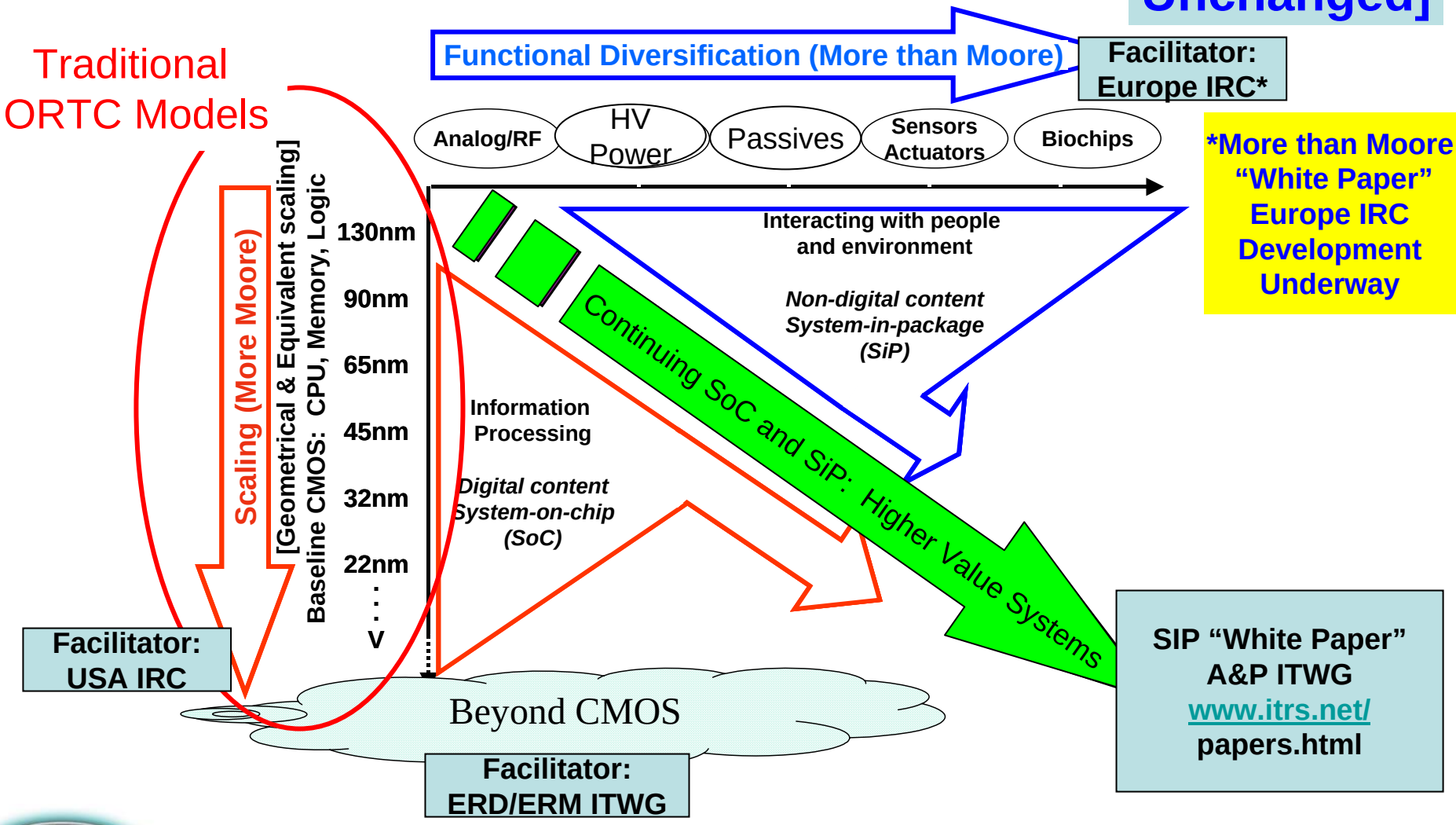
   1) 1-yr pull-in; 2yr generation "Moore's Law" doubling cycle;
   2) growing Chip Sizes after return to 3-year technology cycle
   3) PIDS Scenario option proposal (for 2010 Update work): "mix and match" 2yr and 3yr doubling cycles across SLC and MLC products
10) New IRC 450mm Position: 32nm Pilot lines/2012; 22nm Production/2014

2007 ITRS Executive Summary Fig 5

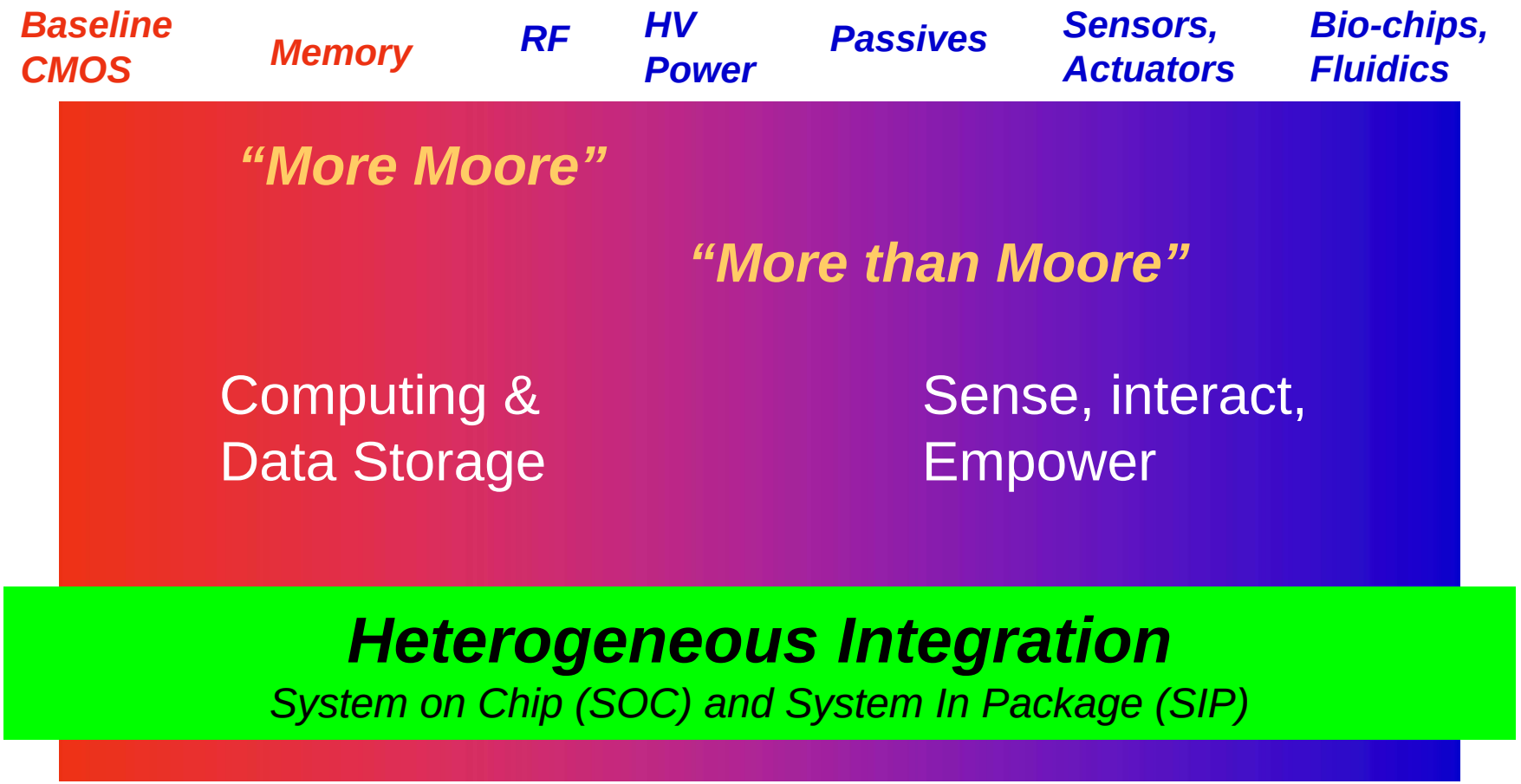
Moore's Law & More

[2009 – Unchanged]



[2009 – Unchanged]

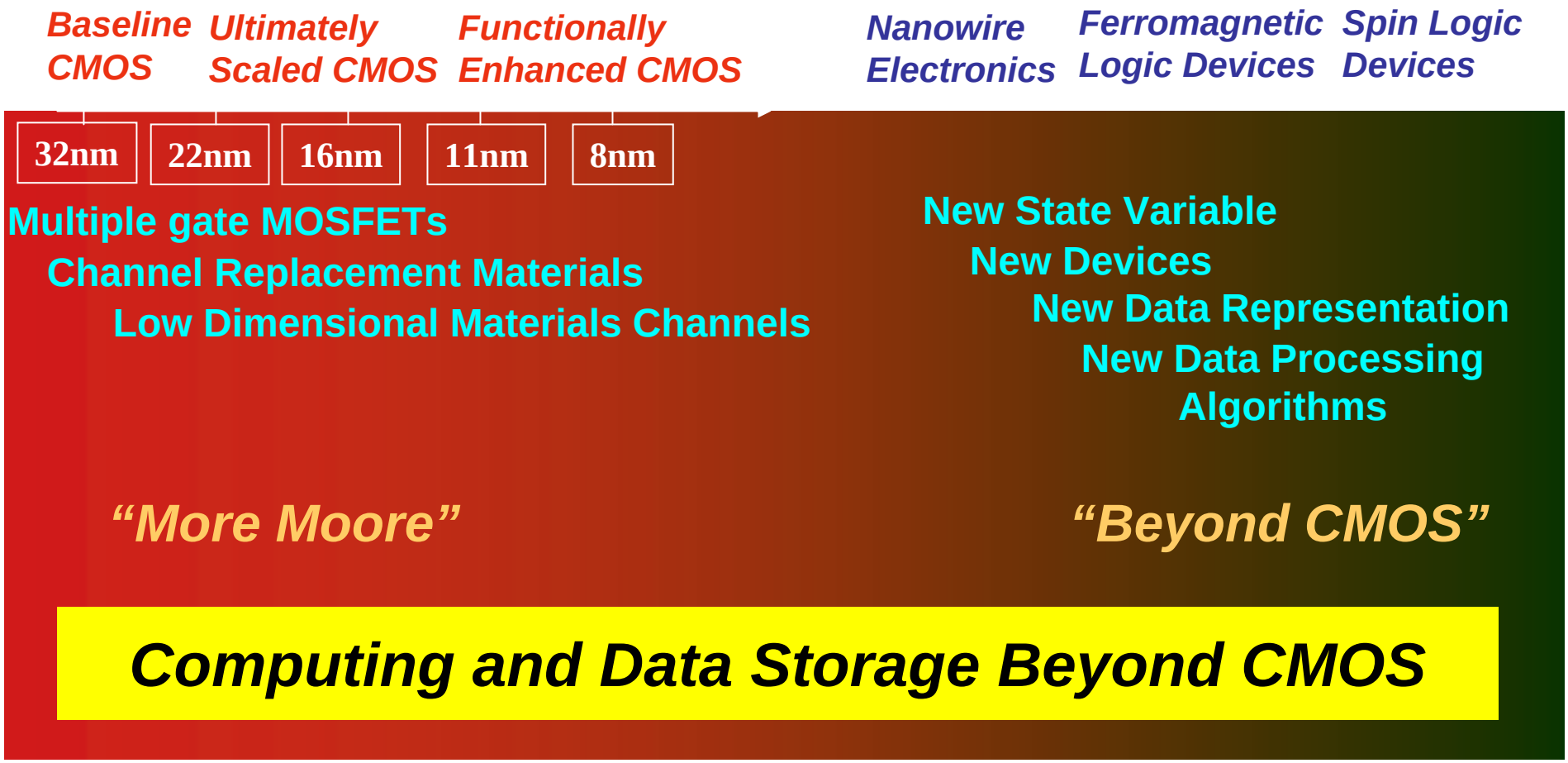
2007/08 ITRS "Moore's Law and More" Alternative Definition Graphic



Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

[2009 – Unchanged]

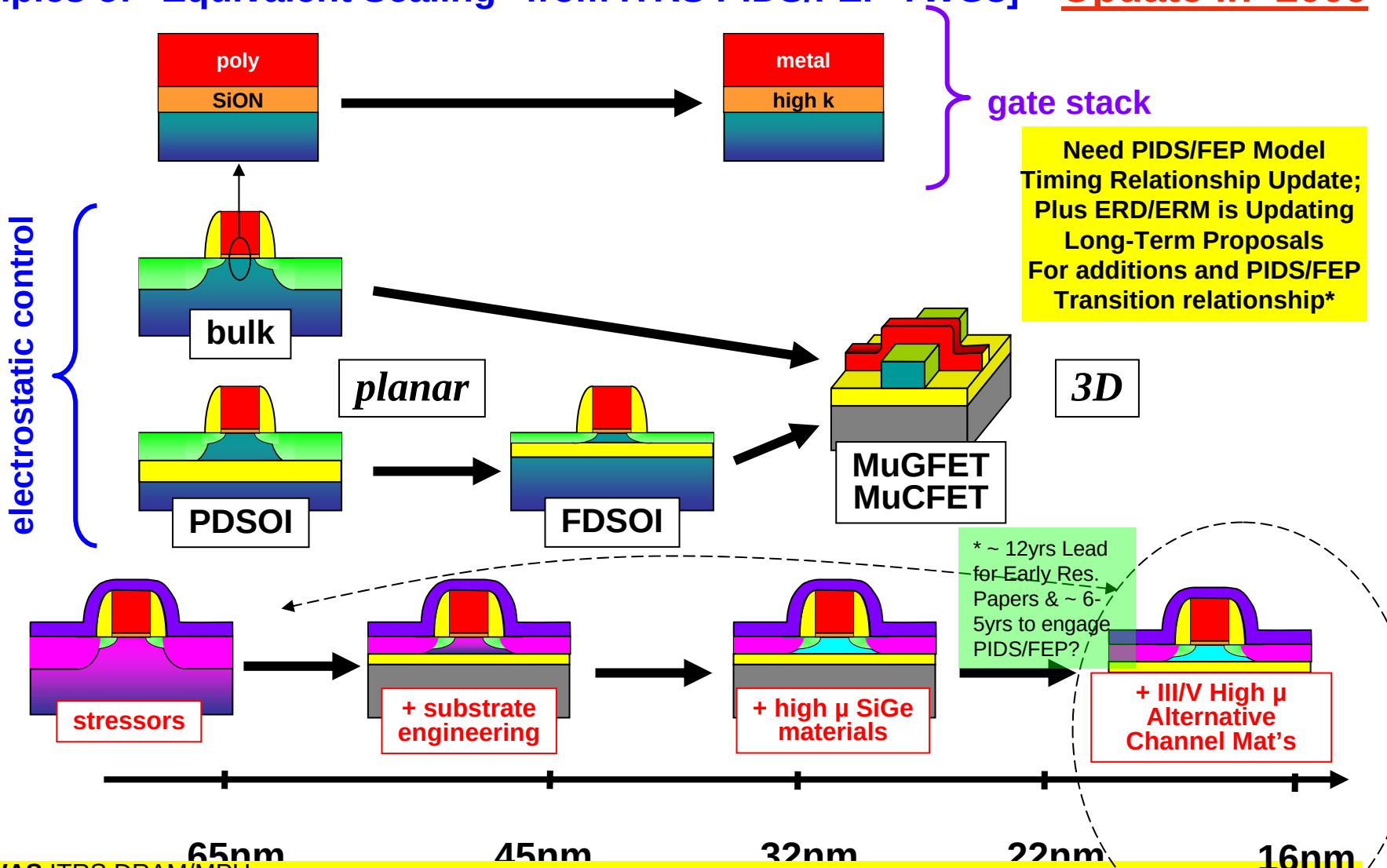
2008 ITRS "Beyond CMOS" Definition Graphic



Source: Emerging Research Device Working Group

2007/08 - PIDS/FEP - Simplified Transistor Roadmap

[Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs] – Update in 2009



[**2008 WAS** ITRS DRAM/MPU Half-Pitch Timing: 2007[7.5] 2010 2013 2016 2019]

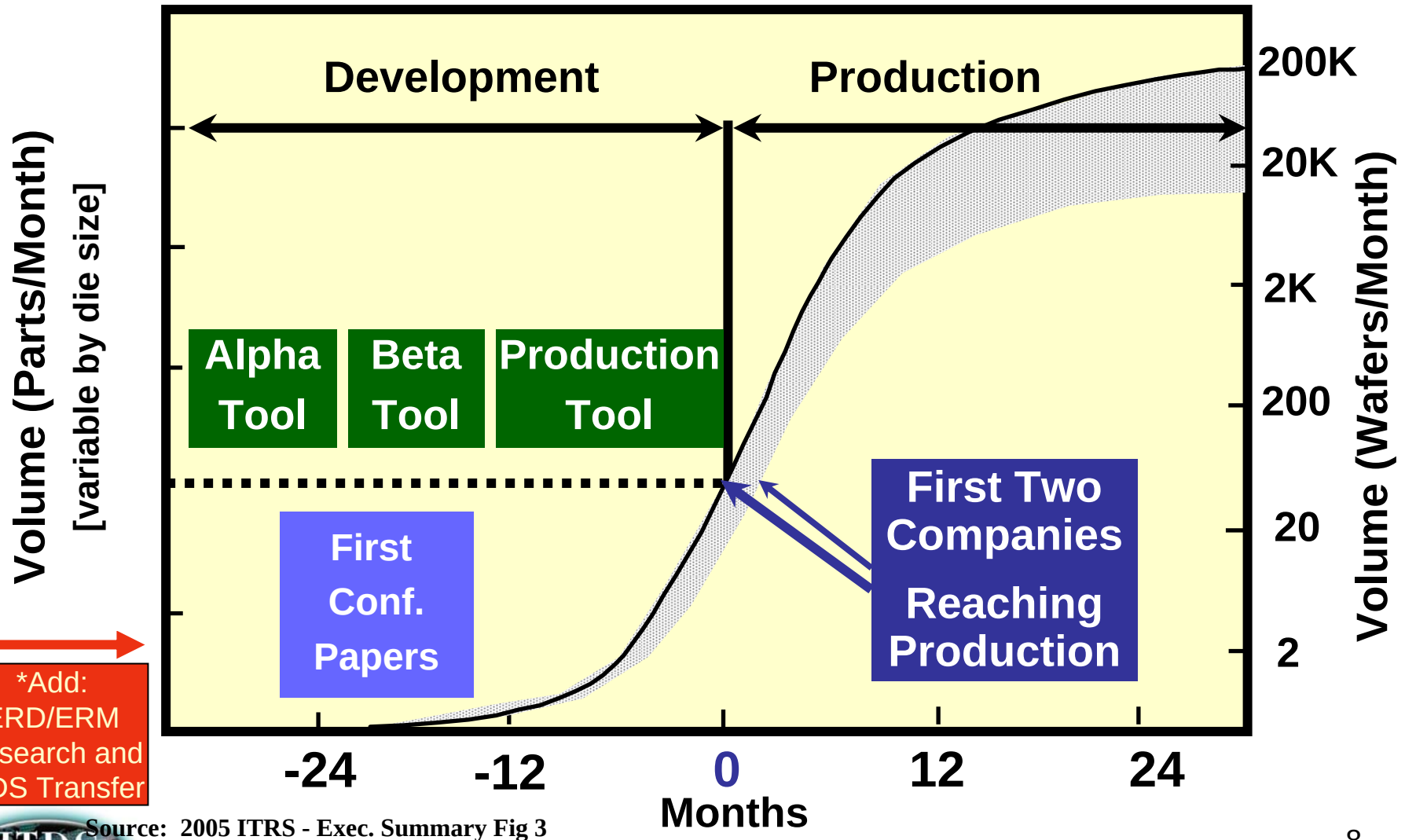
Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

[*2009 ITRS ERD/ERM Proposal Feb'09]

Fig 3

2009 – Updated (no Parts/Month scale); and add ERD/ERM Research and PIDS Transfer *

Production Ramp-up Model and Technology Cycle Timing



Source: 2005 ITRS - Exec. Summary Fig 3

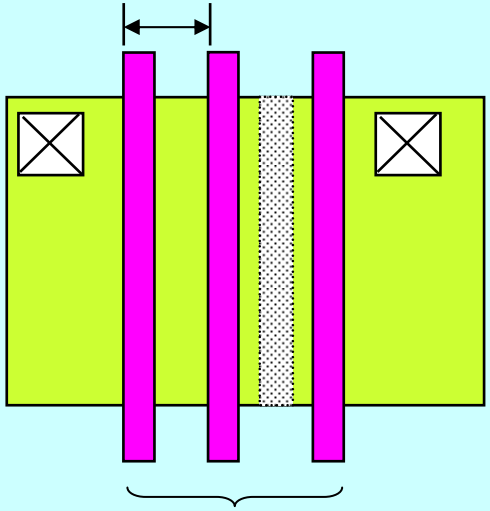
2007 Definition of the Half Pitch – 2008 unchanged

[No single-product "node" designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2

Poly

Pitch



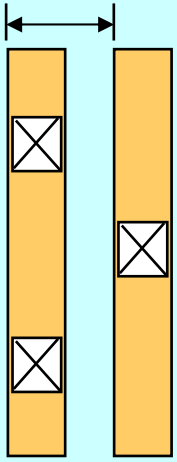
8-16 Lines

Typical flash
Un-contacted Poly

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

Metal

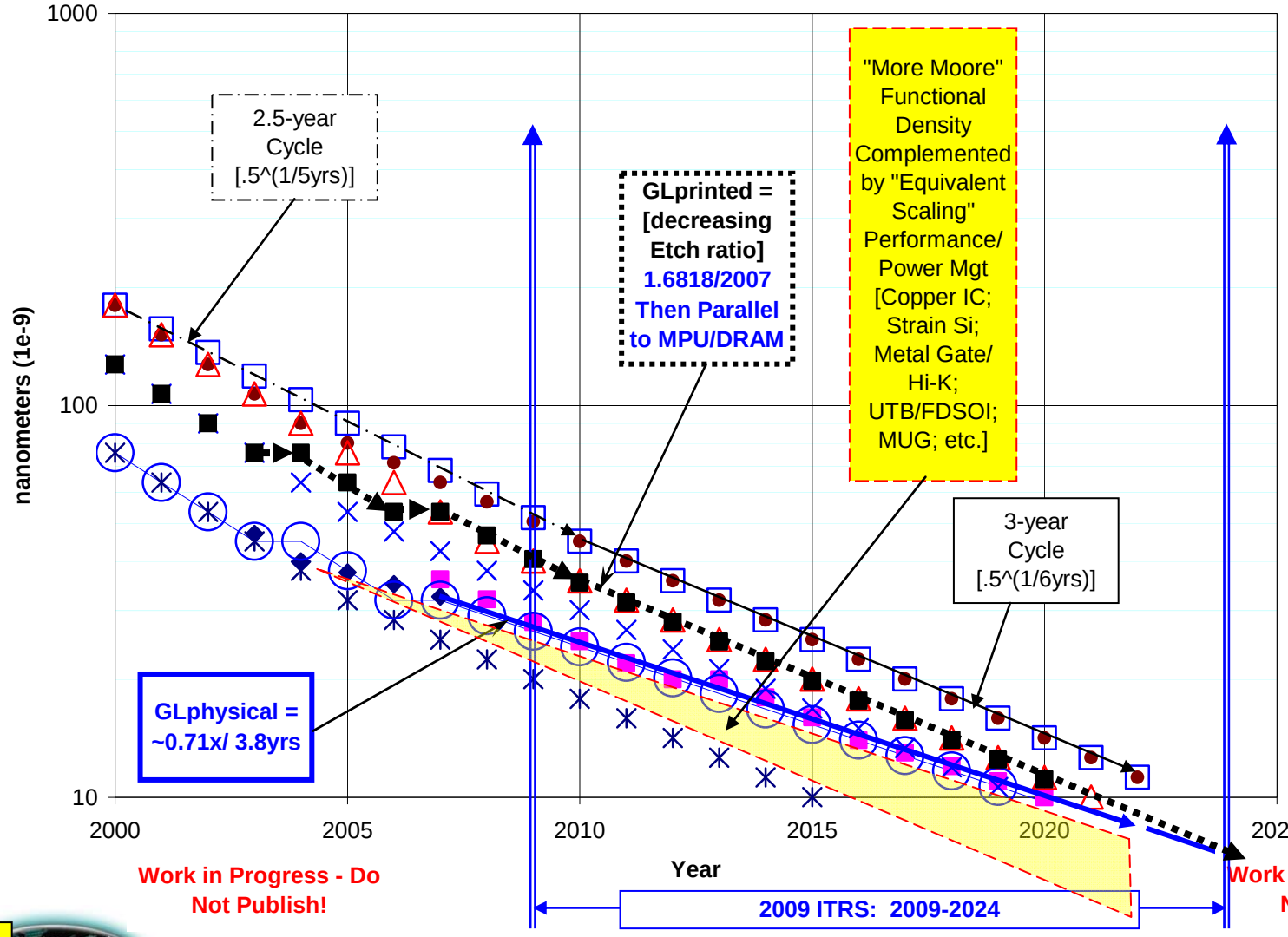
Pitch



Typical DRAM/MPU/ASIC
Metal Bit Line

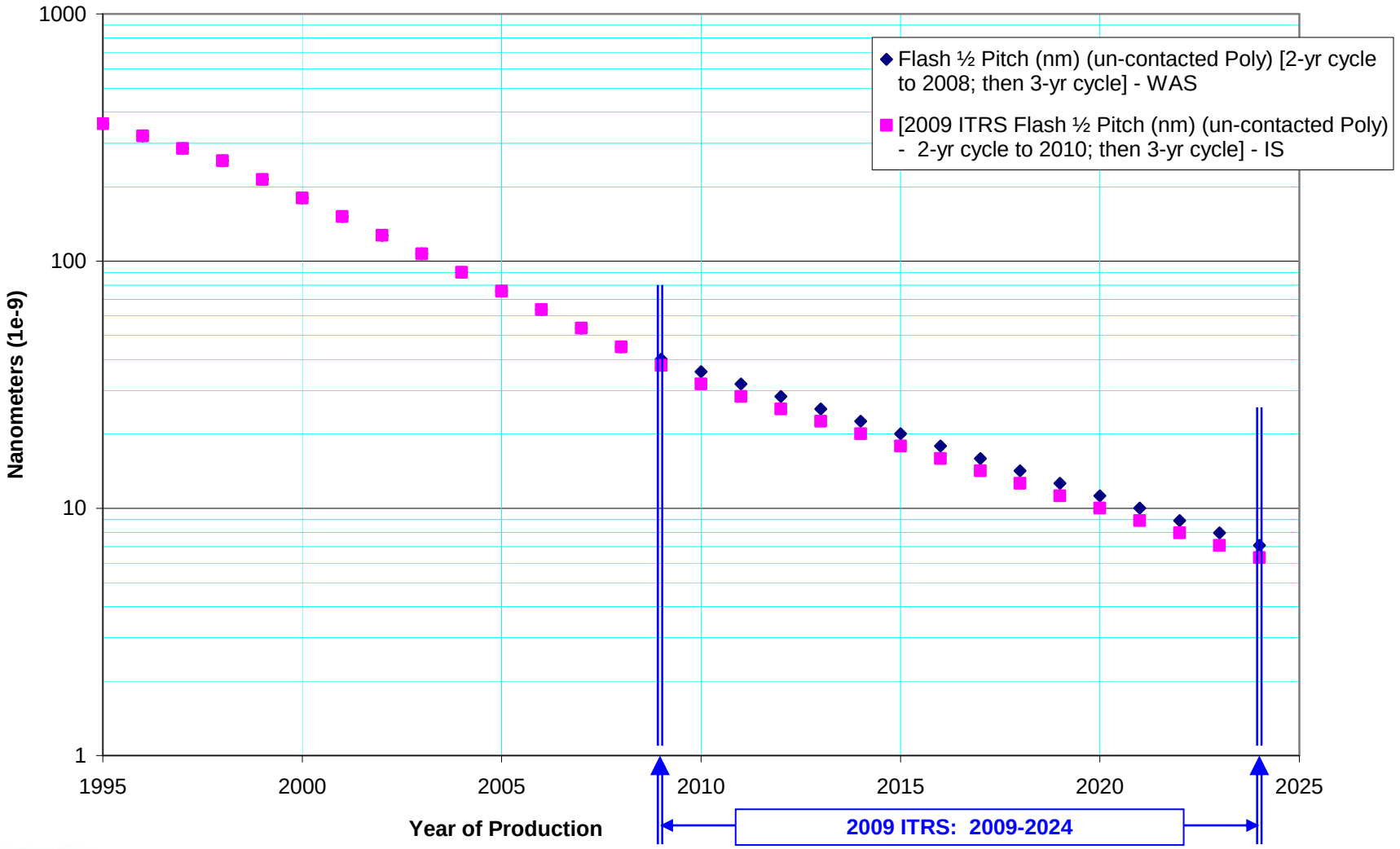
Source: 2005 ITRS - Exec. Summary Fig 2

2008 ITRS Update - Technology Trends vs Actuals and Survey [including Final Litho Printed Gate Length Proposal]

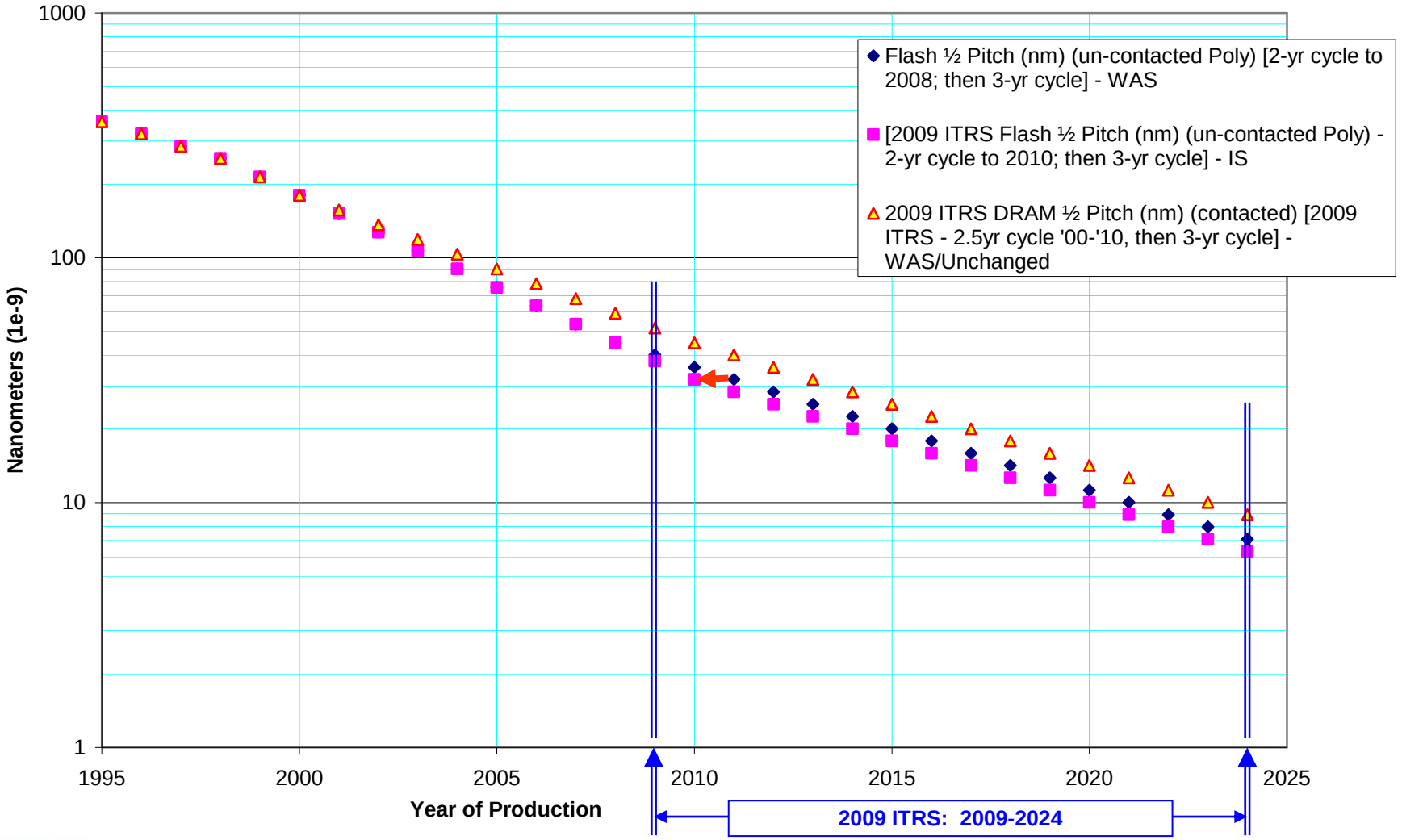


- Jeff Butterbaugh/FEP GLphys Actuals (leading):
- Kwok Ng/PIDS GLphys Survey (leading):
- Glpr(nm) MPU (ITRS 05-07) → 2008 Update
- Glph(nm) MPU (ITRS 05-07) → 2008 Update
- M1 Half Pitch(nm) MPU (ITRS 05-07) [also DRAM M1 in 2008 Update]
- M1 Half Pitch(nm) DRAM (ITRS 05-07)
- Poly Half Pitch(nm) Flash (ITRS 07) [Litho Driver after 2007]
- GLph Proposal 2008 Update Final
- GLpr(nm) MPU HP Proposal4 [FINAL - Litho Jul'08]

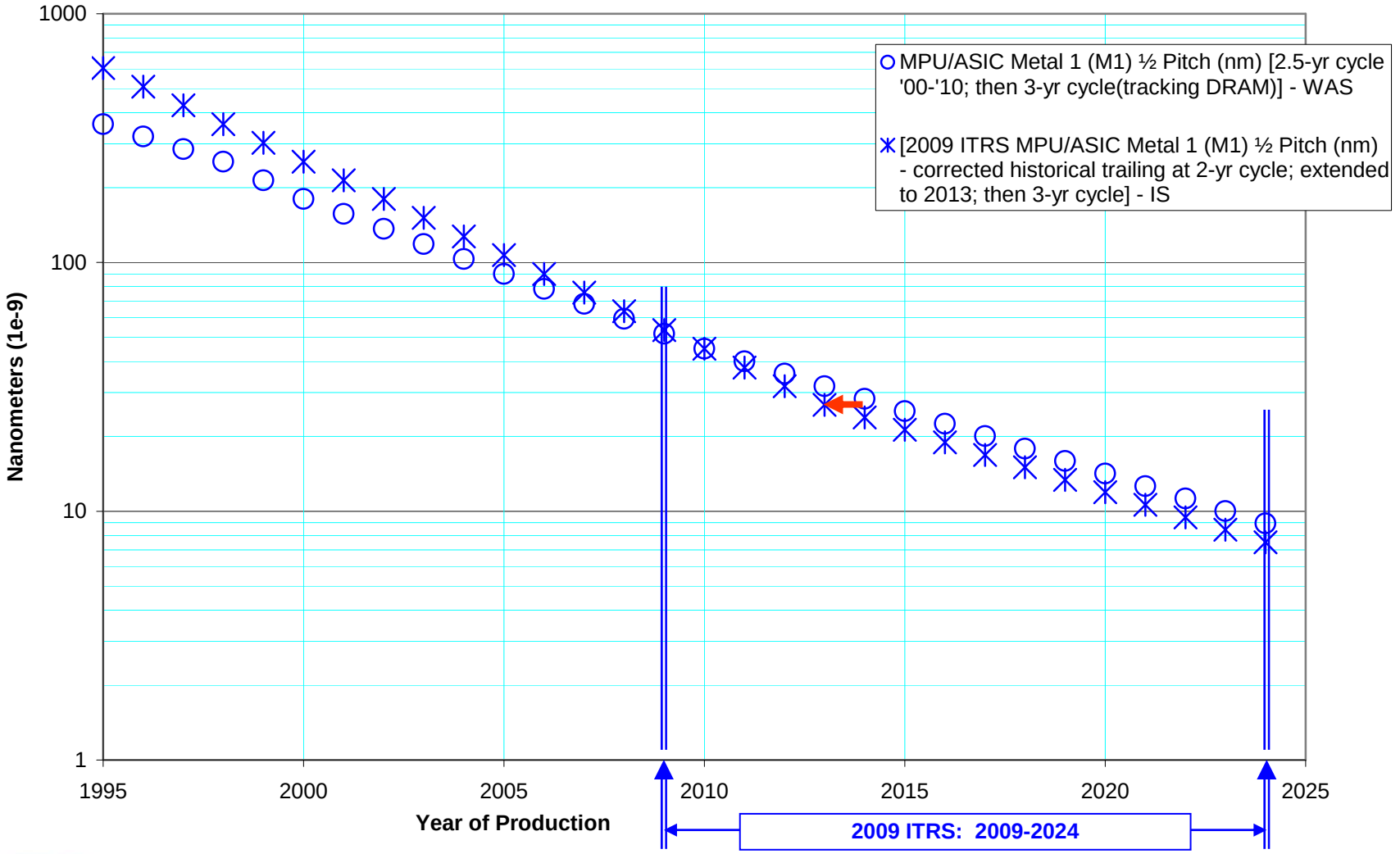
2009 ITRS - Technology Trends



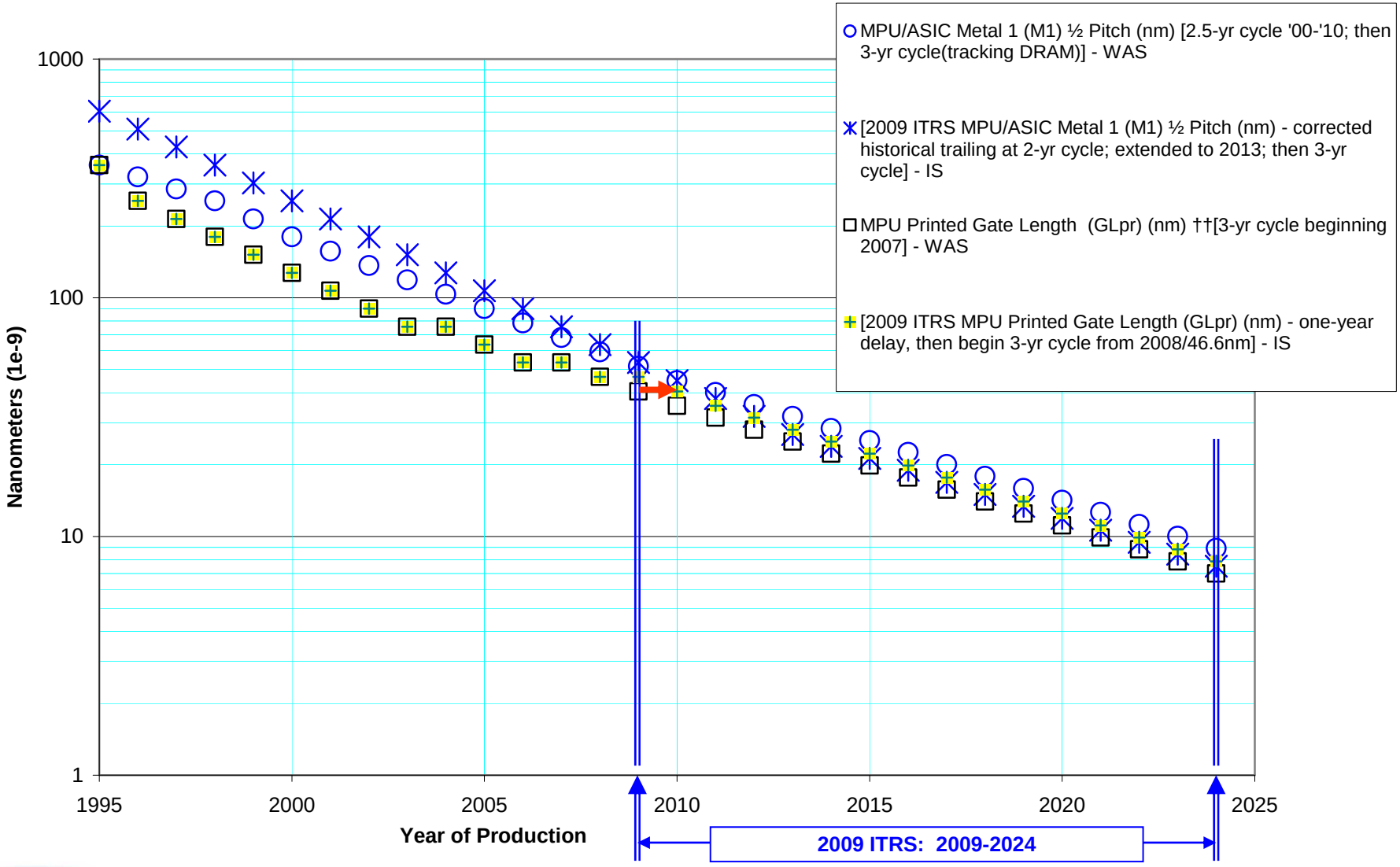
2009 ITRS - Technology Trends



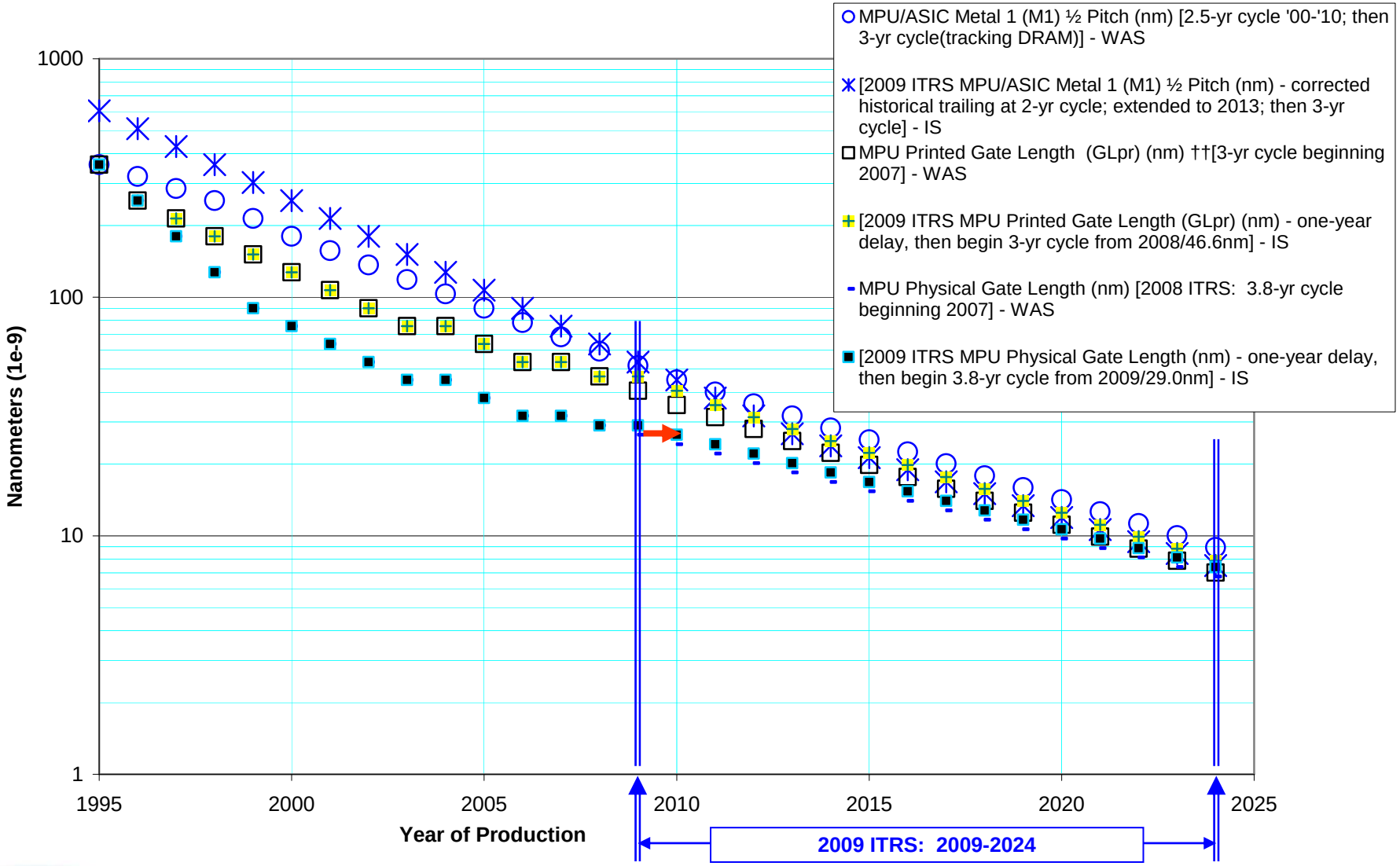
2009 ITRS - Technology Trends



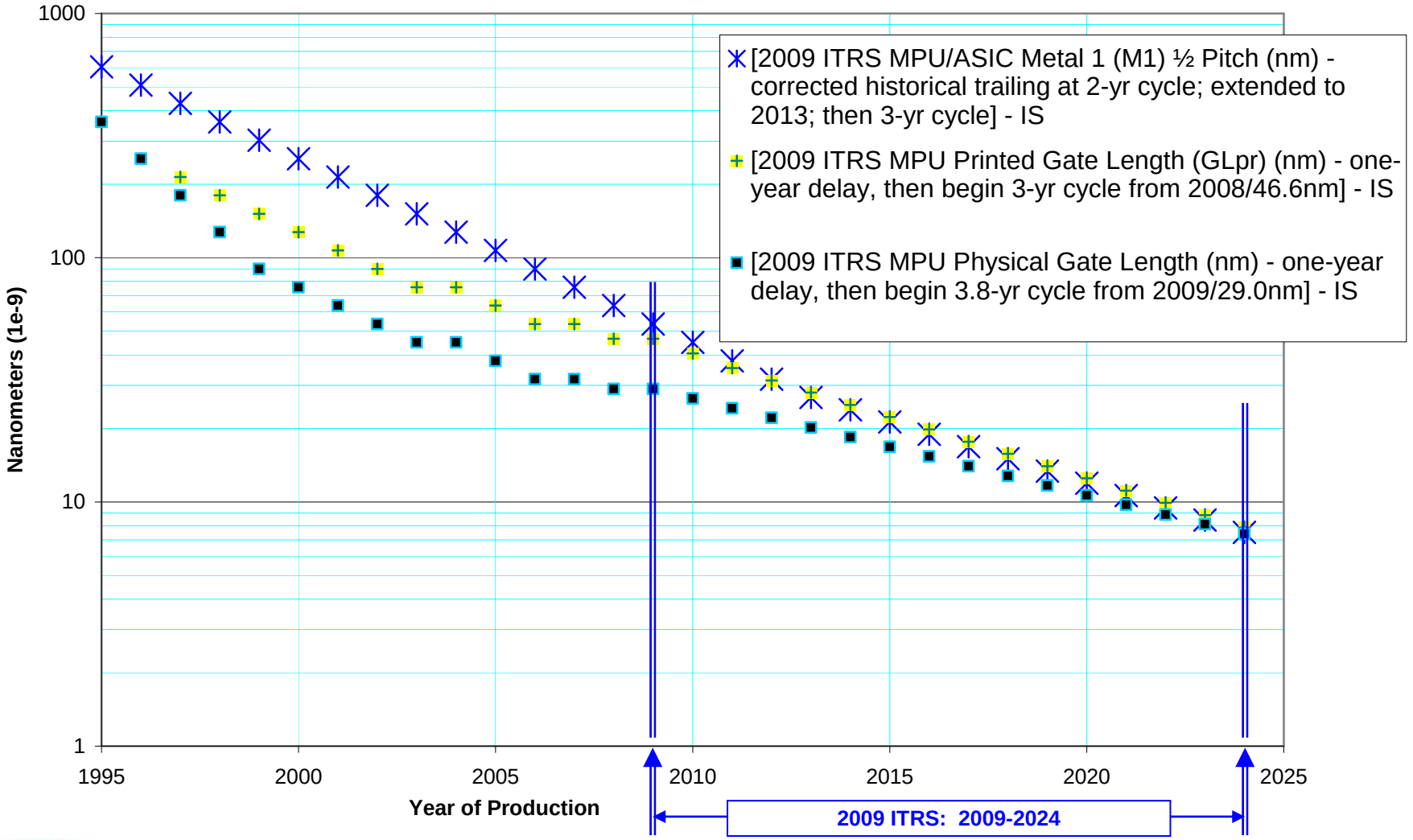
2009 ITRS - Technology Trends



2009 ITRS - Technology Trends



2009 ITRS - Technology Trends



2009 ITRS - Technology Trends

Industry MPU [also Hi-Performance (hp) ASIC] "Node"* Alignment w/ITRS

DRAM Density "Equiv. Scaling":	$8f^2$	$8f^2$	$6f^2$	$4f^2$	TBD	TBD	TBD
Flash Density MLC "Equiv. Scaling":	16/11/8/5.5/4f2: 2b/cell	$2.0f^2$: 2b/cell	$1.5f^2$: 3b/cell	$1.0f^2$:4b/cell	TBD	TBD	TBD
MPU Perform/Power "Equiv. Scaling":	Copper	Strain	HiK/MG	TBD	TBD	TBD	TBD

Dimensional Half Pitch Scaling (EOT not shown):

Past ↔ Future

Note: TSMC uses "40nm"(no HiK/MG) and "28nm" (SiON Lo-K + ?? Gate Hi-K) As their "node labels" and actual M1 ****

Year	'99	'00	'01	'02	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20	'21	'22	'23	'24	'25
~ Mark Bohr Tutorial**; +extrapolation: "Node"	"180"	"160"	"130"	"110"	"90"	"80"	"65"	"55"	"45"	"40"	"32"	"28"	"22"	"20"	"16"		->	"11"			"8.0"			"5.6"			"4.0"
~Actual	303	255	214	180	151	127	107	90	76	64	54	45	38	32	27	24	21	19									
EETimes, Xbit TSMC**** +extrapolation: calculated	277.6	233.4	196.3	165.1	138.8	116.7	98.1	82.5	69.4	58.3	49.1	41.3	34.7	29.2													
~Actual	270	226	190	160	135	113	95	80	67	57	48	40	34	28													
WAS DRAM (unch.) / ITRS M1 WAS		180		127			90			64		45			32			22			16			11			7.9
WAS MPU/(& hp ASIC) / 2008 ITRS Contacted MPU M1: [2.5yr Cyc thru '10, then 3yr]											52	45	40	36	32	28	25	22	20	18	16	14	13	11	10	8.9	7.9
IS MPU/(& hp ASIC) / 2009 ITRS Proposal MPU M1: [2yr Cyc thru '13, then 3yr]											54	45	38	32	27	24	21	19	17	15	13	12	11	9.5	8.4	7.5	6.7
IS MPU/(& hp ASIC) / 2009 ITRS Proposal MPU GLpr: [3yr Cycle >'10]											47	41	35	31	28	25	22	20	18	16	16	14	12	9.9	8.8	7.8	7.0
IS MPU/(& hp ASIC) / 2009 ITRS Proposal MPU GLph: [3.8yr Cycle >'09]											29	27	24	22	20	18	17	15	14	13	12	11	9.7	8.9	8.1	7.4	6.8
WAS Flash / 2008 ITRS Proposal Flash Poly: [3yr Cycle >'08]											40	36	32	28	25	22	20	18	16	14	13	11	10	8.9	8.0	7.1	6.3
IS Flash / 2009 ITRS Proposal Flash Poly: [2yr Cyc thru '10, then 3yr]											38	32	28	25	22	20	18	16	14	13	11	10	8.9	8.0	7.1	6.3	5.6

MPU & hp ASIC Same ~actual targets; Odd, Even "node" yrs

2010 45nm "Hinge" Year

2013 32nm 2nd "Hinge" Year: (MPU M1 turns to a 3-year Cycle)

~1.5yr pull-in of the M1 function size and density driver => ~3-4yr pull-in of Function Size And Density Timing due to square relationship

2009 ITRS: 2009-2024

*Notes:
1) DRAM industry "Node" typically = Contacted M1 half-pitch***;
2) Flash "Node" typically = Uncontacted Poly half-pitch, which Is approx. equivalent (i.e.,using same lithography technology) to a 2-year lead of DRAM contacted M1 DRAM.
3) Litho TWG estimates Flash driving Lithography since 2007.
4) At 2-year behind the Flash Uncontacted-Poly, the 2012/32nm Contacted M1 MPU/hp-ASIC will be a co-driver of Lithography, and will lead DRAM M1 by 1 year.

**Mark Bohr Tutorial, 3/5/08, #19 "Transistor [half] Pitch" and #5 "Minimum Feature Size"

* http://intel_im.edgesuite.net/2008/123085/IM2008_Bohr.pdf

***However, Inoue-san presentation has Samsung Using "40nm-class" announcement in 2009 (52nm?)

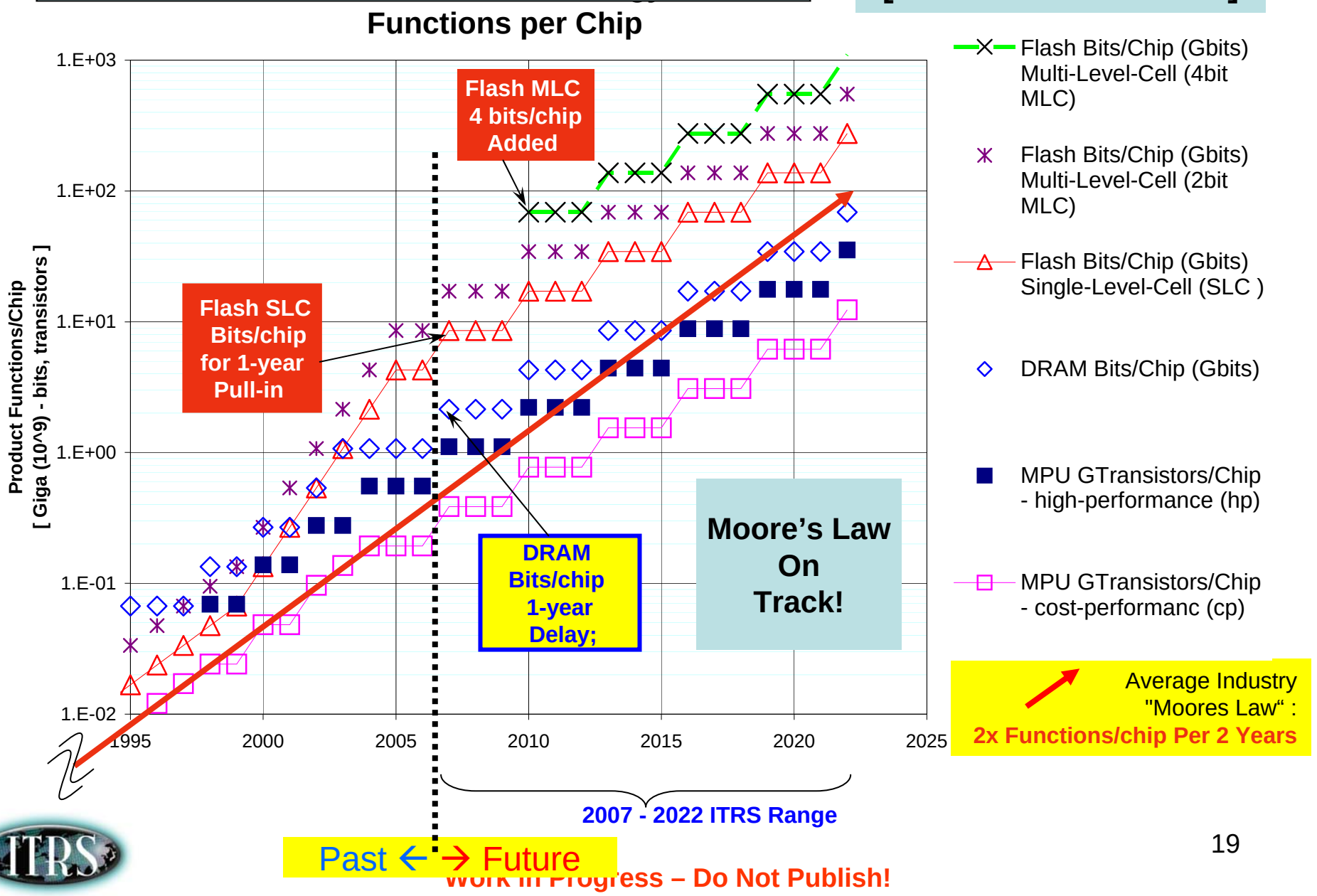
****TSMC "Nodes" Articles @: http://www.xbitlabs.com/news/other/display/20080930205529_TSMC_Unveils_32nm_28nm_Process_Technologies_Roadmap.html ; http://www.eetimes.com/news/semi/showArticle.jhtml?articleID=177100620

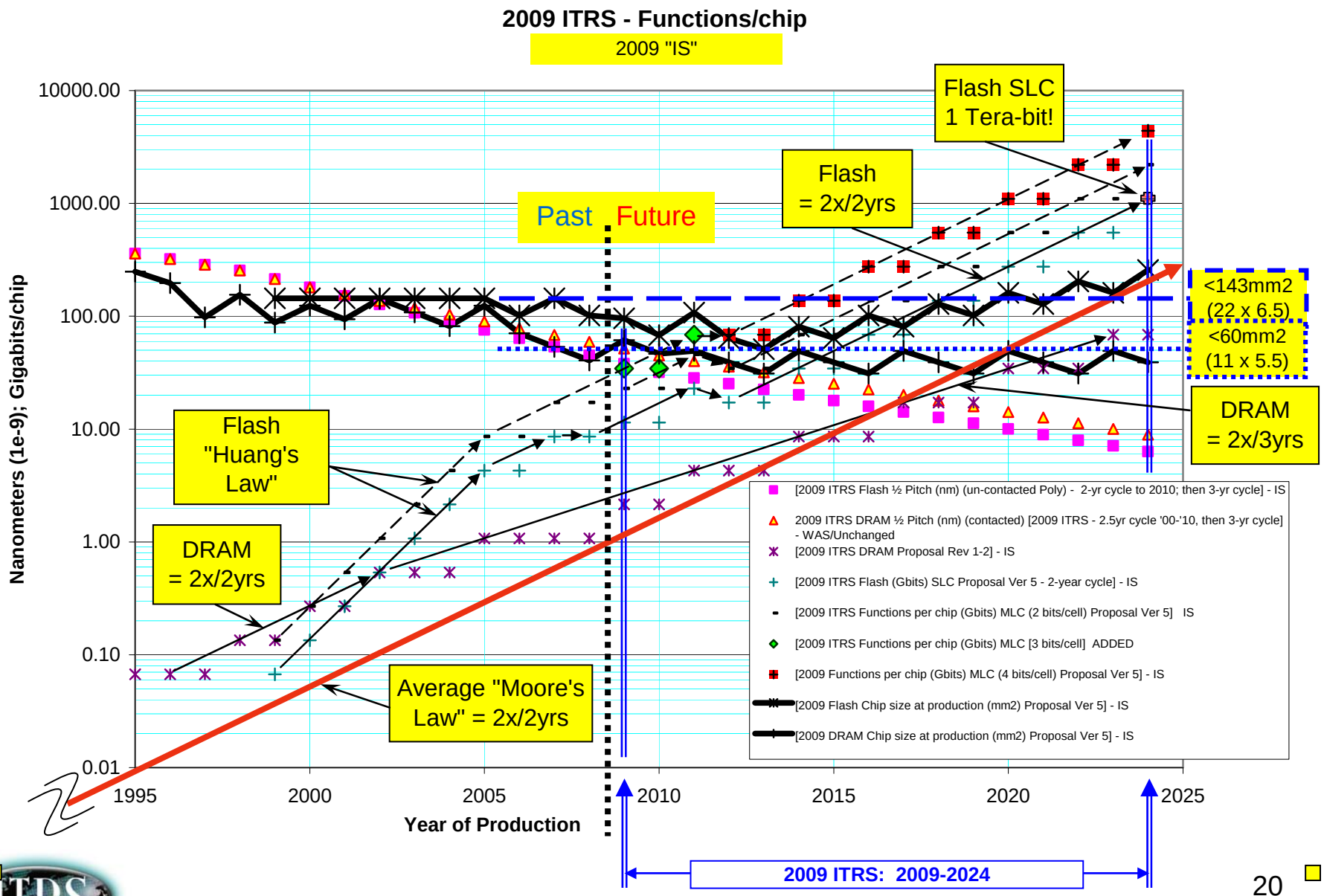
Work in Progress – Do Not Publish!

Figure 10 ITRS Product Functions per Chip

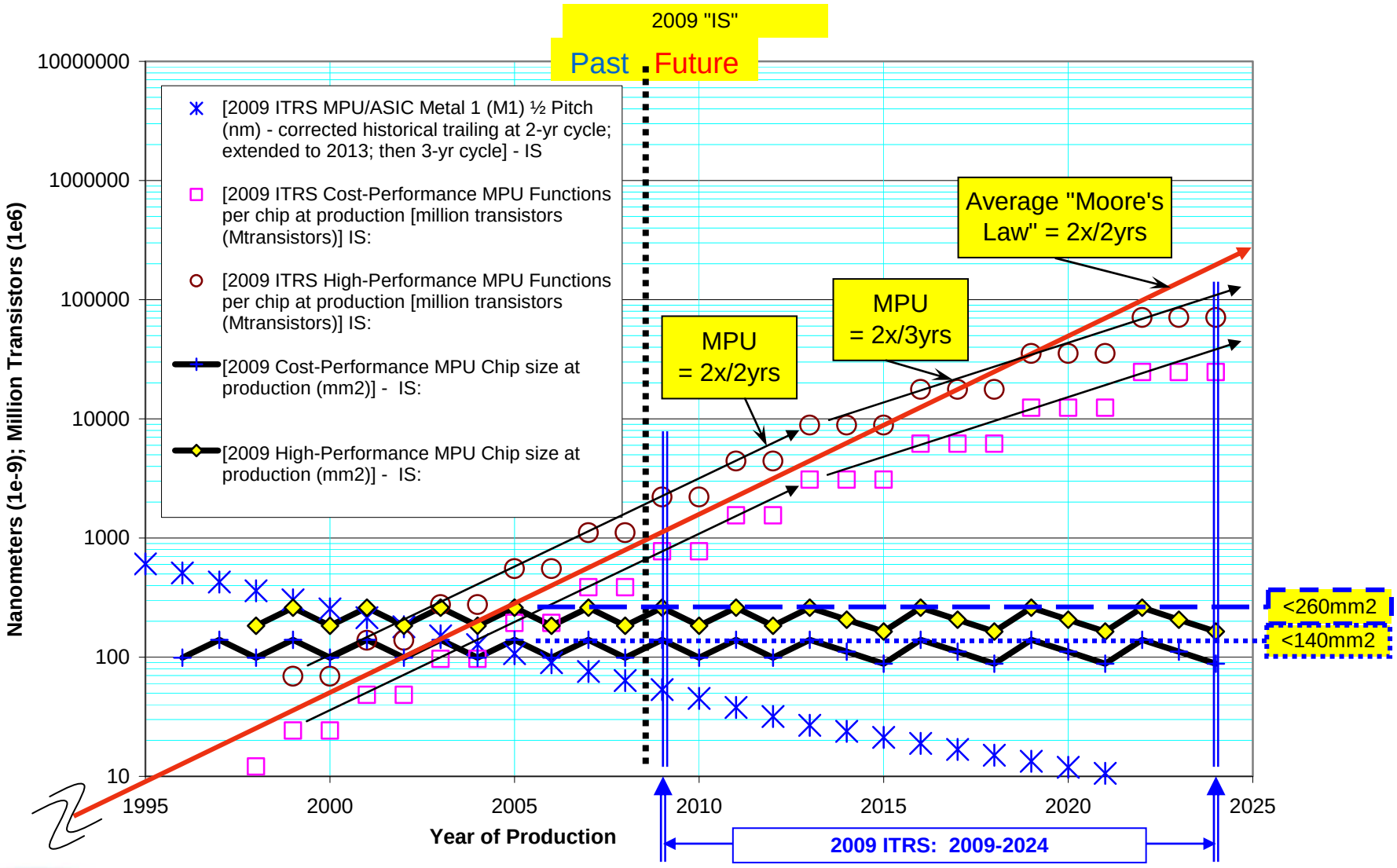
[MIT "Moore's Law" Article: http://www.technologyreview.com/computing/21901/?a=f]

[2007/08 ITRS "WAS"]

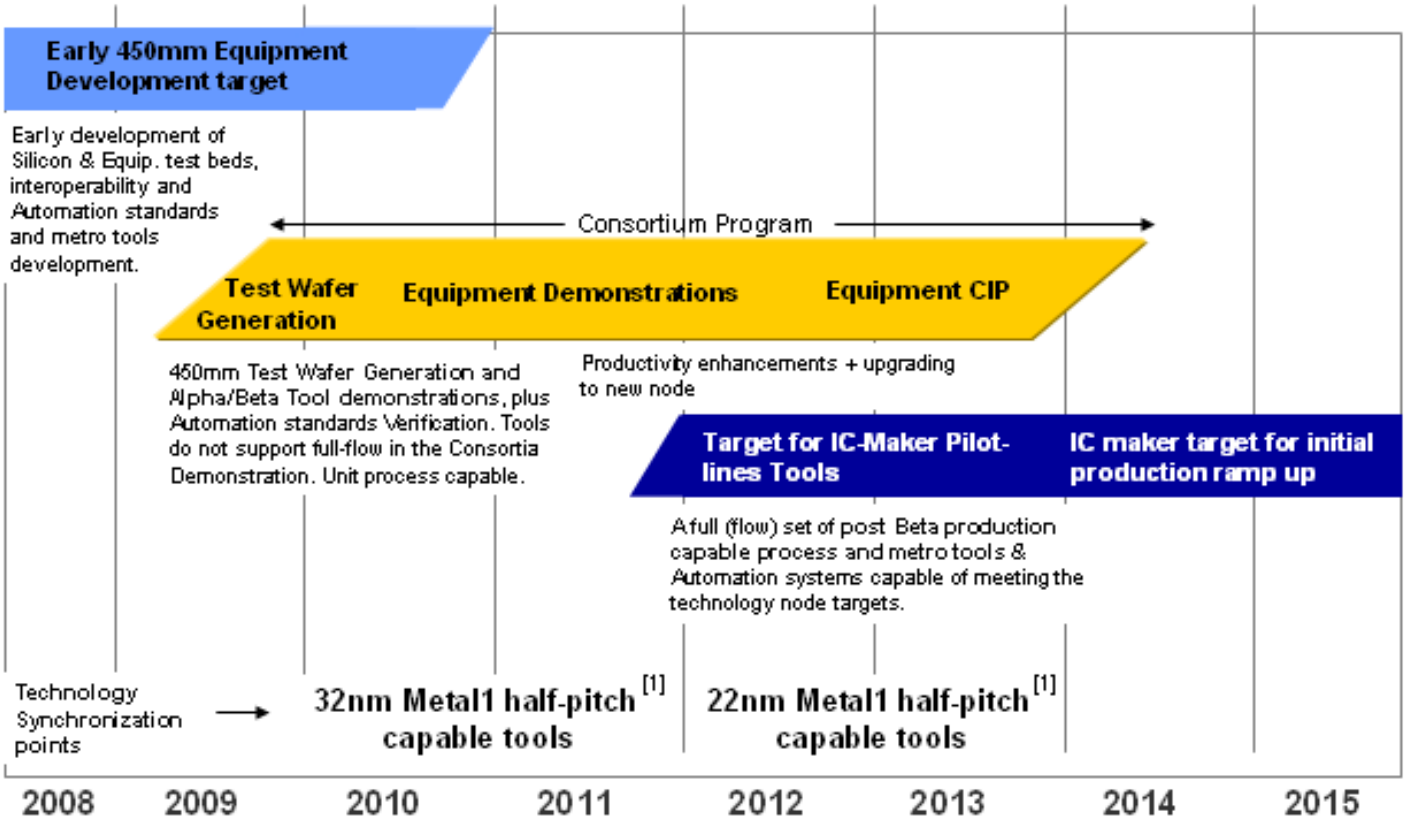




2009 ITRS - Technology Trends



Development & Technology Intercept Targets for 450mm



Note: Detailed technology goals will be defined by individual company business requirements

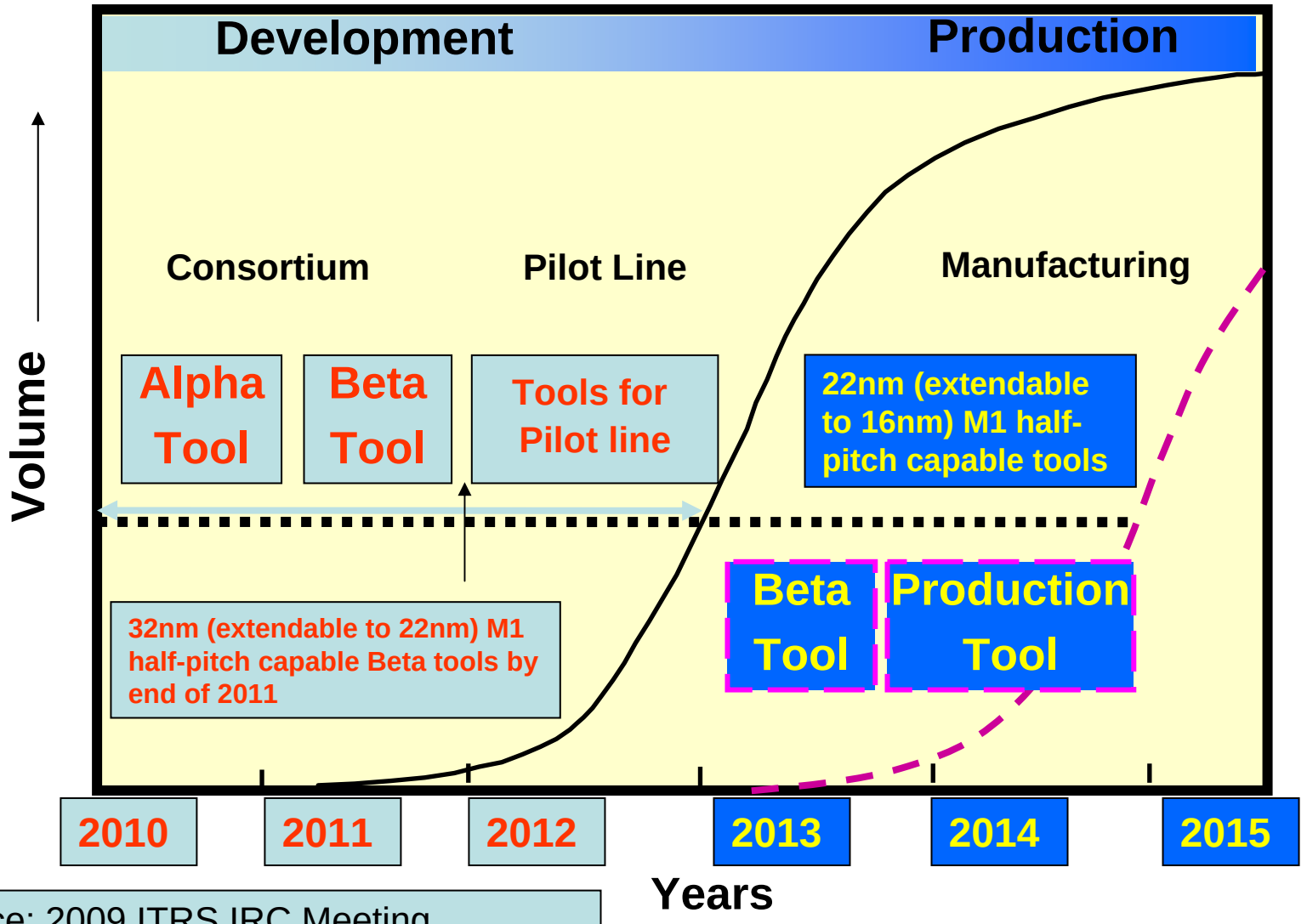
[1]: Reference is DRAM stagger-contacted Metal 1 half-pitch in nanometers

Intel, Samsung, and TSMC (IST) announced in May'08 that they will work together with suppliers, other semiconductor players and ISMI to develop 450mm with a goal of a pilot line in 2012. Full production may be 2-3 years after that. – "May 2008"/ "Oct 2008 ISMI symposium"/Dec'08 ISMI 450mm Transition Program Status Update for ITRS IRC, Seoul, Korea

ITRS IRC Position 7/13/09:

1) Wafer diameter should not be tied to technology generations.
2) The Public IST(Intel, Samsung, TSMC)/ISMI announcement and assessment may be subject to revision based on future statements; but it is the statement of record by these three companies and ISMI.
3) The ITRS/IRC expects manufacturing tools to be available between 2012 to 2014 for pilot lines; with possible production manufacturing ramp from 2014-2016 and beyond.

450mm Production Ramp-up Model



Source: 2009 ITRS IRC Meeting, 7/14/09; interpretation of 2008 ISMI Timing

2009 ITRS IRC 450mm Timing Update
"The Bottom Line"

Table ORTC-3 Lithographic-Field and Wafer Size Trends

	Year of Production	2007	2008	2009	2010	2011	2012	2013	2014
ADD	***Flash ½ Pitch (nm) (un-contacted Poly)(f)***	54	45	40	36	32	28	25	23
IS		54	45	38	32	28	25	23	20
WAS	***DRAM ½ Pitch (nm) (contacted)***	68	59	52	45	40	36	32	28
IS		68	59	52	45	40	36	32	28
WAS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	68	59	52	45	40	36	32	28
IS		76	64	54	45	38	32	27	24
ADD	***MPU Printed Gate Length (GLpr) (nm) ††***	54	47	41	35	31	28	25	22
IS		54	47	47	41	35	31	28	25
WAS	***MPU Physical Gate Length (GLph) (nm)***	32	29	27	24	22	20	18	17
IS		32	29	29	27	24	22	20	18
WAS	*Lithography Field Size*								
IS									
WAS	*Maximum Lithography Field Size—area (mm^2)*	858	858	858	858	858	858	858	858
IS		858	858	858	858	858	858	858	858
WAS	*Maximum Lithography Field Size—length (mm)*	33	33	33	33	33	33	33	33
IS		33	33	33	33	33	33	33	33
WAS	*Maximum Lithography Field Size—width (mm)*	26	26	26	26	26	26	26	26
IS		26	26	26	26	26	26	26	26
WAS	*Maximum Substrate Diameter (mm)—High-volume Production (>20K **parts** starts per month)*								
IS									
WAS	*Bulk or epitaxial or SOI wafer*	300	300	300	300	300	450	450	450
IS		300	300	300	300	300	300	300	450

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   3) ORTC line item added to deal with OverHead (OH) area model changes to deal with non-active area
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10) New IRC 450mm Position: 32nm Pilot lines/2012; 22nm Production/2014

Backup

- 2009 ITRS/ORTC Technology Trend tables
- Frequency Targets (Unch. From 2008)

2009 ITRS

Table ORTC-1 ITRS Technology Trend Targets

	Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
WAS	*Flash ½ Pitch (nm) (un-contacted Poly)(f)*	54	45	40	36	32	28	25	23	20
IS		54	45	38	**32**	**28**	**25**	**23**	**20**	**18**
WAS	*DRAM ½ Pitch (nm) (contacted)*	68	59	52	45	40	36	32	28	25
IS		68	59	52	45	40	36	32	28	25
WAS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	68	59	52	45	40	36	32	28	25
IS		**76**	**64**	**54**	**45**	**38**	**32**	**27**	**24**	**21**
WAS	*MPU Printed Gate Length (GLpr) (nm) ††*	54	47	41	35	31	28	25	22	20
IS		54	47	**47**	**41**	**35**	**31**	**28**	**25**	**22**
WAS	*MPU Physical Gate Length (GLph) (nm)*	32	29	27	24	22	20	18	17	15
IS		**32**	**29**	**29**	**27**	**24**	**22**	**20**	**18**	**17**

Table ORTC-1 ITRS Technology Trend Targets

	Year of Production	2016	2017	2018	2019	2020	2021	2022	2023	2024
WAS	*Flash ½ Pitch (nm) (un-contacted Poly)(f)*	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1
IS		**15.9**	**14.2**	**12.6**	**11.3**	**10.0**	**8.9**	**8.0**	**7.1**	**6.3**
WAS	*DRAM ½ Pitch (nm) (contacted)*	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
IS		22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
WAS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
IS		**18.9**	**16.9**	**15.0**	**13.4**	**11.9**	**10.6**	**9.5**	**8.4**	**7.5**
WAS	*MPU Printed Gate Length (GLpr) (nm) ††*	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9	7.0
IS		**19.8**	**17.7**	**15.7**	**14.0**	**12.5**	**11.1**	**9.9**	**8.8**	**7.9**
WAS	*MPU Physical Gate Length (GLph) (nm)*	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	6.8
IS		**15.3**	**14.0**	**12.8**	**11.7**	**10.7**	**9.7**	**8.9**	**8.1**	**7.4**

2009 ITRS

Table ORTC-1 ITRS Technology Trend Targets

	Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
WAS	Flash ½ Pitch (nm) (un-contacted Poly)(f)	54	45	40	36	32	28	25	23	20
IS		54	45	38	**32**	**28**	**25**	**23**	**20**	**18**
WAS	DRAM ½ Pitch (nm) (contacted)	68	59	52	45	40	36	32	28	25
IS		68	59	52	45	40	36	32	28	25
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	68	59	52	45	40	36	32	28	25
IS		**76**	**64**	**54**	**45**	**38**	**32**	**27**	**24**	**21**
WAS	MPU Printed Gate Length (GLpr) (nm) ††	54	47	41	35	31	28	25	22	20
IS		54	47	**47**	**41**	**35**	**31**	**28**	**25**	**22**
WAS	MPU Physical Gate Length (GLph) (nm)	32	29	27	24	22	20	18	17	15
IS		**32**	**29**	**29**	**27**	**24**	**22**	**20**	**18**	**17**
WAS	ASIC/Low Operating Power Printed Gate Length (nm) ††	64	54	47	41	35	31	25	22	20
IS		64	54	**54**	**47**	**41**	**35**	**31**	**25**	**22**
WAS	ASIC/Low Operating Power Physical Gate Length (nm)	38	32	29	27	24	22	18	17	15
IS		38	32	**32**	**29**	**27**	**24**	**22**	**18**	**17**
WAS	ASIC/Low Standby Power Physical Gate Length (nm)	45	38	32	29	27	22	18	17	15
IS		45	38	**38**	**32**	**29**	**27**	**22**	**18**	**17**
WAS	MPU Etch Ratio GLpr/GLph (nm)	1.6818	1.6039	1.5296	1.4588	1.4237	1.3895	1.3561	1.3235	1.2917
IS		1.6818	1.6039	**1.6039**	**1.5296**	**1.4588**	**1.4237**	**1.3895**	**1.3561**	**1.3235**

Table ORTC-1 ITRS Technology Trend Targets

	Year of Production	2016	2017	2018	2019	2020	2021	2022	2023	2024
WAS	Flash ½ Pitch (nm) (un-contacted Poly)(f)	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1
IS		**15.9**	**14.2**	**12.6**	**11.3**	**10.0**	**8.9**	**8.0**	**7.1**	**6.3**
WAS	DRAM ½ Pitch (nm) (contacted)	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
IS		22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
IS		**18.9**	**16.9**	**15.0**	**13.4**	**11.9**	**10.6**	**9.5**	**8.4**	**7.5**
WAS	MPU Printed Gate Length (GLpr) (nm) ††	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9	7.0
IS		**19.8**	**17.7**	**15.7**	**14.0**	**12.5**	**11.1**	**9.9**	**8.8**	**7.9**
WAS	MPU Physical Gate Length (GLph) (nm)	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	6.8
IS		**15.3**	**14.0**	**12.8**	**11.7**	**10.7**	**9.7**	**8.9**	**8.1**	**7.4**
WAS	ASIC/Low Operating Power Printed Gate Length (nm) ††	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9	7.0
IS		**19.8**	**17.7**	**15.7**	**14.0**	**12.5**	**11.1**	**9.9**	**8.8**	**7.9**
WAS	ASIC/Low Operating Power Physical Gate Length (nm)	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	6.8
IS		**15.3**	**14.0**	**12.8**	**11.7**	**10.7**	**9.7**	**8.9**	**8.1**	**7.4**
WAS	ASIC/Low Standby Power Physical Gate Length (nm)	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	6.8
IS		**15.3**	**14.0**	**12.8**	**11.7**	**10.7**	**9.7**	**8.9**	**8.1**	**7.4**
WAS	MPU Etch Ratio GLpr/GLph (nm)	1.2607	1.2304	1.2008	1.1720	1.1438	1.1163	1.0895	1.0609	1.0329
IS		**1.2917**	**1.2607**	**1.2304**	**1.2008**	**1.1720**	**1.1438**	**1.1163**	**1.0895**	**1.0633**

Performance and Power Management Enabled by "Equivalent Scaling"