Front End Processes
2009 ITRS

ITRS Public Conference
July 15, 2009
Marriott Hotel, San Francisco

2009 Summer Meeting FEP ITWG Participants:
J. Butterbaugh, R. Jammy, M. Walden, M. Goldstein, M. Watanabe, L. Chang, G. Celler, M. Beebe, P. Majhi, Y. Le Tiec
[by conference call: L. Larson, T. Lii, J. Barnett, M. Alessandri]

2009 FEP Sub-TWGs and Chairs

NEW STRUCTURE FOR FEP CHAPTER in 2009

DEVICE METRICS

- Logic Devices [HP, LOP, LSTP]: Prashant Majhi (US)
- DRAM Devices: Deoksin Kil (KR)
- Flash Devices: Mauro Alessandri (EU)
- PCM Devices: Mauro Alessandri (EU)
- FeRAM Devices: Yoshimasa Horii (JP)

PROCESS METRICS

- Starting Materials: Mike Walden (US), Mike Goldstein (US)
- Surface Preparation: Joel Barnett (US)
- Thermal/Thin Films/Doping: Prashant Majhi (US)
- Etch: Tom Lii (US)
- CMP: Darryl Peters (US)

Logic Devices

- **New Table Structure**
  - Individual tables to focus on device metrics for HP, LOP, and LSTP
- **New scaling approach coordinated with PIDS**
  - reset CV/I benchmark in 2009
  - CV/I improvement factor changed to 13% per year
- **New Model Assumptions and New Rows; Parasitic Resistance Constraint**

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU Printed Gate Length (nm)	47	41	35	31	28	25	22
MPU Physical Gate Length (nm)	29	27	24	22	20	18	17
Supply voltage of operatin (voltage scaling to ensure total active power cnsumption not to exceed heat removal rate)	**0.95**	**0.95**	**0.85**	**0.85**	**0.75**	**0.75**	**0.65**
Threshold voltage under linear drain bias conidition (V)	**0.32**	**0.32**	**0.27**	**0.27**	**0.22**	**0.22**	**0.22**
Saturation drive current (mA/um)	**1.68**	**1.80**	**1.80**	**1.80**	**1.75**	**1.75**	**1.7**
Off-state current under high drain bias (nA/um)at room temperature	**100**	**100**	**100**	**100**	**100**	**100**	**100**

- **LOP and LSTP still need to be addressed**
- **Introduction of FDSOI and Multigate still under consideration → next slide**

Timing of CMOS Innovations

ongoing FEP/PIDS discussions . . .

2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021

HP bulk CMOS (ITRS 2008) ???

HP UTB/FDSOI (ITRS 2008)

??? HP Multi-Gate (ITRS 2008)

LOP bulk CMOS (ITRS 2008) ???

LOP UTB/FDSOI (ITRS 2008)

??? LOP Multi-Gate (ITRS 2008)

LSTP bulk CMOS (ITRS 2008) ???

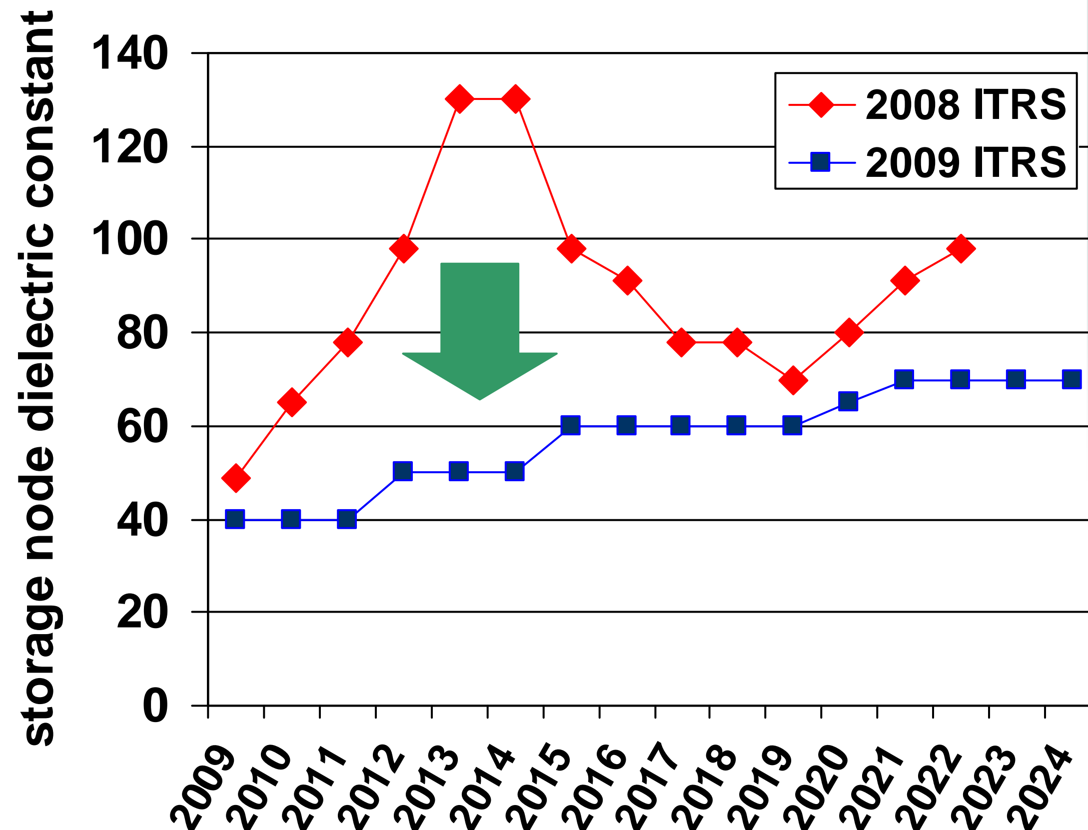
LSTP UTB/FDSOI (ITRS 2008)

LSTP Multi-Gate (ITRS 2008)

ongoing discussions . . .

DRAM

- a factor drops from 6 to 4 in 2011, driving smaller cell size and smaller storage node size → colored yellow
- capacitance per cell reduced from 25 to 20 pF in 2011 due to introduction of buried word line
- capacitor dielectric constant reduced and no longer peaks at 130
- capacitor dielectric constant physical thickness reduced → no longer red
- A/R yellow in 2010 and red in 2013



Flash

- Floating Gate Flash will require only minor adjustments
- New Table added for the Charge-Trapping Flash,
- CT Table is still under construction, but will include:
  1. EOT thickness for the tunnel oxide
     → including the material/structure to be used
  2. Max leakage current for the tunnel oxide (for retention purpose)
     → measured @ 3 MV/cm for write and -1.5 MV/cm for erase
  3. Minimum trap density for the charge trap layer (cm^{-3})
  4. Properties of the Charge Trapping layer
     → minimum band offset vs conduction band of the tunnel dielectric and the blocking dielectric (eV)
  5. Minimum dielectric constant of the blocking dielectric
  6. Max leakage current for the blocking dielectric (for ritention purpose)
     →measured @ 1 MV/cm for write and -1 MV/cm for erase
  7. Work function of the gate material
  8. Program - Erase window (based on PIDS)
  9. Retention (based on PIDS)

PCRAM

- **Added conformality of the PCM cell sealing dielectric.**
- **The challenge in this case is to achieve conformality within a very low thermal budget compatible with the phase change material**

Grey cells indicate the requirements projected for years before it reaches volume production.

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*
PCM ½ Pitch (nm) (contacted)	50	45	40	35	32
Phase change material min. conformality (%) [A]	70	90	90	90	98
PCRAM phase change material minimum operating temperature (°C) [B]	100	100	100	100	125
Heater max resistivity change during reset cycle and after 1E12 cycles (%)	5	5	5	5	5
Maximum Reset Current Density (A/ μm^2)	0.3-0.8	0.4-1.0	0.4-1.0	0.4-1.0	0.5-1.3
Cell Sealing Dielectric min. conformality (%)[E]	90	95	95	95	98

FeRAM

- **Table parameters, general trend are unchanged**
- **Trends in 4-year blocks**

Year of Production	*2009-2012*	*2013-2016*	*2017-2020*	*2021-2024*
FeRAM technology – F (nm) [A]	**180**	**130**	**90**	**65**
FeRAM cell size – area factor a *in multiples of F2* [B]	**22**	**16**	**14**	**12**
FeRAM cell size (μm^2) [C]	**0.713**	**0.27**	**0.113**	**0.051**
FeRAM cell structure [D]	**1T1C**	**1T1C**	**1T1C**	**1T1C**
FeRAM capacitor structure [E]	**stack**	**stack**	**3D**	**3D**
FeRAM capacitor footprint (μm^2) [F]	**0.33**	**0.106**	**0.041**	**0.016**
FeRAM capacitor active area (μm^2) [G]	**0.33**	**0.106**	**0.1**	**0.069**
FeRAM cap active area/footprint ratio	**1**	**1**	**2.46**	**4.25**
Ferro capacitor voltage (V) [I]	**1.5**	**1.2**	**1**	**0.7**
FeRAM minimum switching charge density ($\mu C/cm^2$) [J]	**13.5**	**34**	**30**	**30**
FeRAM endurance (read/write cycles) [K]	**1.00E+14**	**1.00E+15**	**>1.0E16**	**>1.0E16**
FeRAM nonvolatile data retention (years) [L]	**10 Years**	**10 Years**	**10 Years**	**10 Years**

Starting Materials

- New ORTC and related chip size / gate length models have been utilized
- Pull-in of 45nm particle size from 2012 to 2010
- Defect densities are no longer allowed to increase from the previous generations' values based upon industry realities
- Near-term improvement in SOI BOX and layer thickness capabilities noted – Partially depleted SOI removed from table beginning with 15nm MPU technology generation
- Continuing to monitor industry activities related to 450mm development and assessing impact on the Starting Materials content
- The Emerging Materials Team (of Starting Materials) will likely add Silicon on Lattice Engineered Substrates (SOLES), a derivative of SOI technology capable of supporting III-V compound integration, as a new emerging material topic in this year's FEP chapter.

Surface Preparation

- Particle metrics updated for changes in DRAM models
- Material loss metrics colorization removed for DRAM
- Achieving material loss goals for advanced logic remains a challenge

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*52*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*54*	*45*	*38*	*32*	*27*
MPU Physical Gate Length (nm)	*29*	*27*	*24*	*22*	*20*
Front surface particles					
Killer defect density, D_pR_p (#/cm^2) [A]	0.033	0.043	0.033	0.042	0.053
Critical particle diameter, d_c (nm) [B]	◆ 25.8	◆ 22.5	◆ 20.0	◆ 17.9	◆ 15.9
Critical particle count, D_{pw} (#/wafer) [C]	◆ 113.3	◆ 113.3	◆ 113.3	◆ 327.2	◆ 327.2
Silicon and oxide loss (Å) on polysilicon blanket test wafers per LDD clean step—DRAM [K]	1.2	0.9	0.9	0.9	0.6
Silicon and oxide loss (Å) on polysilicon blanket test wafers per LDD clean step—Microprocessor/SoC/Analog [L]	0.4	◆ 0.3	◆ 0.3	◆0.3	◆0.2

Thermal/Thin Films/Doping

- New process metrics table
- Split from device metrics table
- Still being edited → expect only minor adjustments

Etch

- **New Methodology to address gate length variation**
  - contributions from lithography and etch cannot be treated separately
  - advanced process control allows lithography tools to make field-to-field adjustments to account for both lithography and etch variations across the wafer
- **Still need to include Physical Gate Length 1-year push**

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*
MPU Printed Gate Length (nm)	41	35	31	28	25	22
MPU Physical Gate Length (nm)	27	24	22	20	18	17
L_{gate} 3 σ variation (nm) [Z]	3.18	2.9	2.65	2.42	2.21	2.02
Lgate line edge roughness 3 σ (nm) [AA]	2	1.86	1.66	1.52	1.4	1.27
Through pitch Lgate variation 3 σ (nm)	1.4	1.3	1.16	1.06	0.97	0.88
Across chip Lgate variation 3 σ (nm)	1.4	1.3	1.16	1.06	0.97	0.89
Across wafer Lgate variation 3 σ (nm)	1	0.93	0.83	0.76	0.7	0.64
Wafer to wafer within lot Lgate 3 σ (nm)	0.8	0.74	0.66	0.62	0.56	0.51
Lot to lot Lgate 3 σ (nm)	0.8	0.74	0.66	0.62	0.56	0.51

CMP

- New Table for 2009 ITRS FEP Chapter
- Initially addressing Allowable Scratches and Uniformity
- Need to clean up colorization

Year of Production	*2009*	*2010*	*2011*	*2012*
DRAM ½ Pitch (nm) (contacted)	52	45	40	36
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	54	45	38	36
MPU Physical Gate Length (nm)	29	27	24	22
Wafer diameter (mm)	**300**	**300**	**300**	**450**
Scratches				
Critical scratch length, s_c (nm) [F]	**25.8**	**22.5**	**20.0**	**17.9**
Critical scratch count, S_{pw} (#/wafer) [F]	**40.1**	**40.1**	**40.1**	**166.2**
Uniformity				
CMP total uniformity (3σ) for removal (%) [F]	**8**	**8**	**8**	**8**
CMP uniformity (3σ) within wafer (%) [F]	**6**	**6**	**6**	**6**

2009 FEP - Highlights

- **Logic Devices:**
  - Separate tables for HP, LOP, LSTP; CV/I pacing set at 13%; Ioff set at 100nA/um
  - Incorporate new Lg pacing
- **DRAM Devices:**
  - Node capacitance adjusted for buried wordline; Capacitor dielectric requirement eased/smoothed
- **Non-volatile memories**
  - Flash – New Charge Trapping Flash Table to be added
  - PCRAM – Conformality of Sealing Dielectric added
  - FeRAM – minor changes; pacing captured in 4-year blocks
- **Starting Materials:**
  - Incorporated new ORTC scaling and recalculated allowable defects
  - Near-term improvement in SOI BOX and layer thickness capabilities noted (color changed)
- **Surface Preparation:**
  - Incorporated new ORTC scaling and recalculated allowable defects
  - Metrology not capable of monitoring killer defect size
- **Thermal/Thin Films/Doping:**
  - New table which is split from previous logic device tables
  - Still under editing; expect no major changes
- **Etch:**
  - New methodology for tracking gate length variation requirements accounting for currently used Advanced Process Control capabilities in lithography.
- **CMP:**
  - New table for 2009; scratches and uniformity requirements are projected